Structured Electronics Design

EE4109
Design exercise 1
A hearing loop system in CMOS18 technology

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Application diagram

Mechanical noise

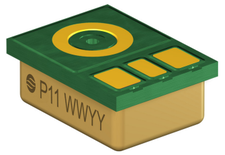
Thermal noise

Electro-magnetic noise

Acoustic signal

30 - 110 dBSPL
20Hz - 6kHz

Microphone



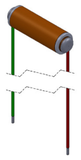
-35.5 dBV @ 1Pa
noise: 25dBSPL

Electrical signal

Magnetic signal

70dB SPL = 0.1 A/m
600Hz - 6kHz

Pick-up coil



-59.4 dBV/(A/m) @ 1 kHz

Electrical signal

Electronic information processing system

source select switch

microphone
hearing loop

A1

pick-up coil
pre-amplifier

ADC driver

A2

ADC input impedance
10 pF

ADC

R2R input

DSP

DAC output impedance
10 kOhm

DAC

R2R output

LSP driver

A3

0.9V Supply
A1, A2,
ADC

Supply regulator

Supply
DAC, A3

Electrical power

Battery

Size 675 Hearing Aid Battery
1.4V 600mAh

30 - 110 dBSPL
20Hz - 6kHz

600Hz - 6kHz

HEARING LOOP INSTALLED
Switch hearing aid to T-coil

1.4V 600mAh
100hrs

max 110 dBSPL
20Hz - 6kHz

Electrical signal

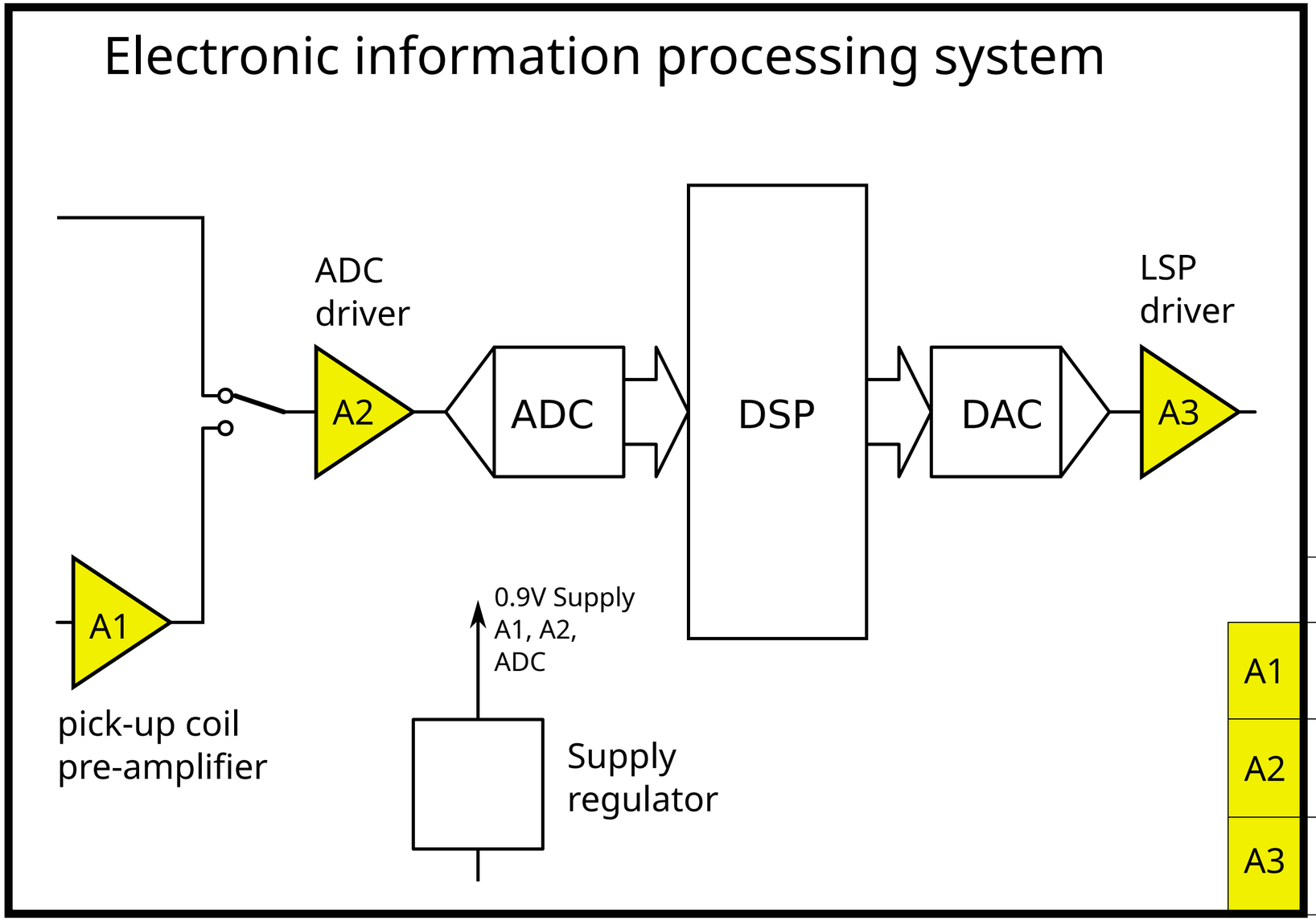
Loudspeaker

101.5 dBSPL
@1kHz, 0.18V_{RMS}

Acoustic signal

max 110 dBSPL
20Hz - 6kHz

Design Exercise 1



Audio signal properties:

crest factor =3
Maximum full-power frequency = 5kHz
0 dBSPL = 20 uPa

System requirements

noise level 30 dBSPL
Peak power level 110 dBSPL
frequency range microphone input : 20 Hz - 6 kHz
frequency range hearing loop: 600 Hz - 6 kHz

Electrical requirements

ADC input signal: max. 0.9Vpp
A1 output signal approximates microphone output
DAC pp. output voltage approximates battery voltage

Design the gain distribution

	Amplifier Type	Desired transfer (Laplace expression)
A1		
A2		
A3		