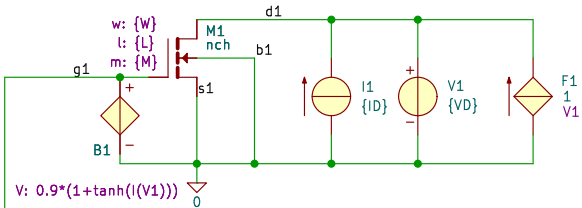
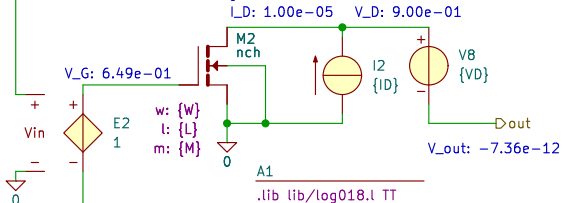


Biasing circuit determines VGS at VD, and ID setpoint



Biased CS stage



A1

```
.lib lib/log018.l TT
```

A2

```
.param ID=10u VD=0.9 W=220n L=180n M=1
```

