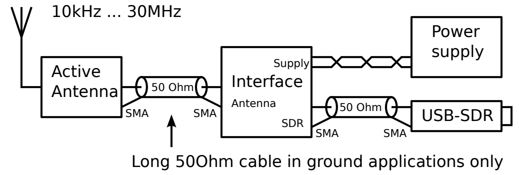
Design of a LF-HF Active Antenna in CMOS18 technology

Radio astronomy antenna for space applications

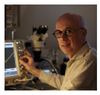


Antenna length: max 0.5m
E-field antenna-referred noise:

10kHz	: 100n	$\left[\frac{\mathrm{V}}{\mathrm{m}\sqrt{\mathrm{Hz}}}\right]$
100KHz	: 10n	
1MHz	: 5n	
30MHz	: 5n	

Output 1dB compression level:
0dBm in 50Ohm
Antenna gain (-3dB: 10kHz-30MHz)
0dB

Features
ESD discharge protected
Low-power 1.8V CMOS technology



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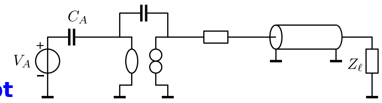
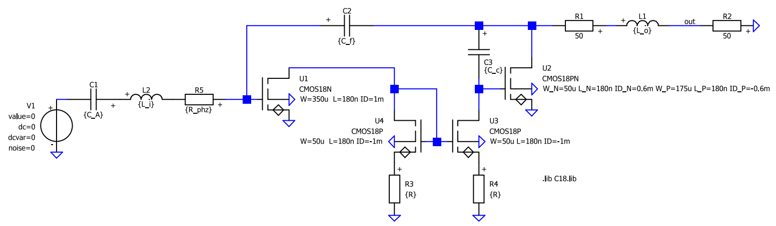


Amplifier concept

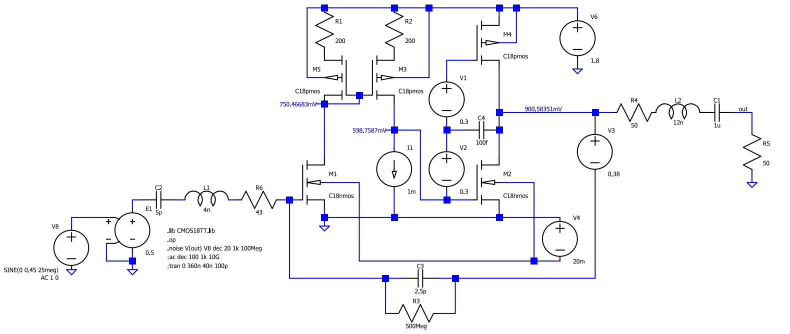
DualStageMirrorResComp1BondWires.asc



SLiCAP

Signal path design of the antenna amplifier
SLiCAP model
- C_iss of the first stage minimized for more effective phantom-zero compensation, I_DS increased for low noise floor. This is possible because there was a significant design margin for noise.
- Output phantom zero with bondwire + trace inductance
- Input complex phantom zeros with bond wire and series resistor
- Current mirror with high cut-off frequency and noise governed by feedback resistors
- Bandwidth limitaion with phantom zeros is not implemented
- Out-of-band interference has not been specified
- More elaborated model of the antenna is available but not implemented.

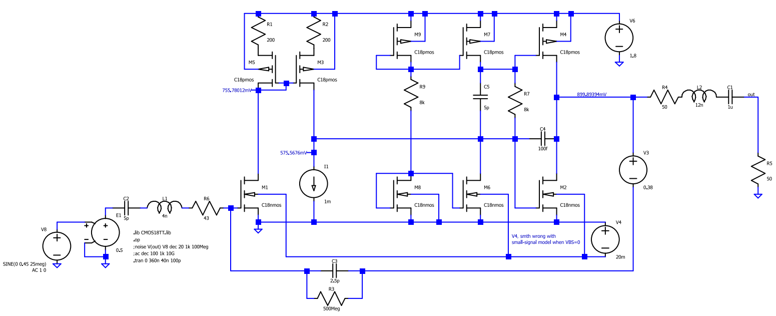
DualStageMirrorRes_Check.asc



From SLiCAP to LTspice

First step biasing:
- LT spice equivalent of signal path
- Aside from R3, only ideal voltage and current sources added
- Check for:
  - Small-signal dynamic response
  - Noise performance
  - Drive capability
  - Weak nonlinearity

DualStageMirrorRes_BiasedEndStage.asc



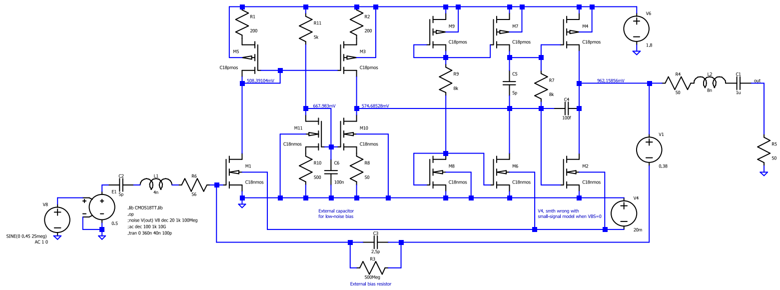
LTspice

Second step biasing:
- Model-based biasing of the output stage (Book Figure 15.32)
  - Use a low reference current (smaller than quiescent current of end stage
  - Short R7 with C5 (should be voltage source = 0 Ohm) Check for distortion and make C5 as small as possible
- Check for:
  - Small-signal dynamic response (no significant change)
  - Noise performance (no significant change)
  - Drive capability (no significant change)
  - Weak nonlinearity (C5)

SLiCAP

Budgets for the (finite) output impedance of the current sources M6, M7, as well as budgets for C5 and R7 can be obtained with SLiCAP.

DualStageMirrorRes_Complete.asc



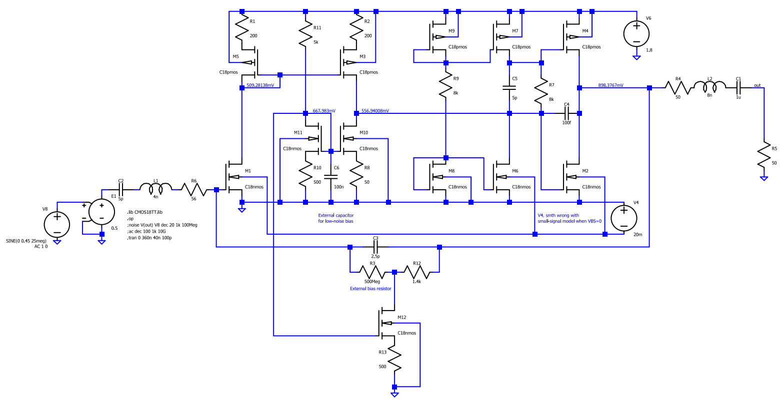
LTspice

Third step biasing:
- Implementation of the current source
  - Adjustment of current input stage (noise performance)
  - Minimization of noise addition current source and improvement PSRR often an external capacitor is required for a low-noise reference (C6).
- Check for:
  - Small-signal dynamic response (no significant change)
  - Noise performance (may require adjustements if budgets were to tight)
  - Drive capability (no significant change)
  - Weak nonlinearity (may be increased if M10 is driven into the linear region in that case the output stage can be driven on a tap of R7, C5)

SLiCAP

Budgets for the (finite) output impedance of the current source (R//C) M10 can be obtained with SLiCAP.

DualStageMirrorRes_MoreComplete



LTspice

Fourth step biasing:
- Implementation of the output voltage source level shift
  - Implemented with a current through a resistor (M12, R12)
  - Take a small current compared to the quiescent current of the output stage
- Check for:
  - Small-signal dynamic response (no significant change)
  - Noise performance (may require adjustements if budgets were to tight)
  - Drive capability (no significant change)
  - Weak nonlinearity (no significant change)

ToDo

- Influence of temperature and device tolerances on all relevant performance parameters
- Adding parasitics after lay-out
- Final optimization