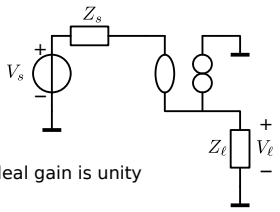
The CD stage

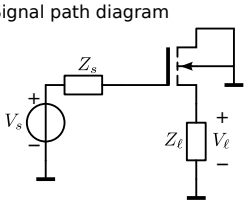
Negative feedback voltage follower

Circuit with ideal controller



Ideal gain is unity

Circuit with CS stage controller
Biasing is omitted:
Signal path diagram



Behavioral modifications negative feedback

Load drive capabilityy

The CD stage is a non-energic feedback stage.
- The feedback network does not deteriorate the load drive capability
- The load drive capability of the CD stage equals that of its controller, which is the biased CS stage.

Power efficiency

The CD stage is a non-energic feedback stage.
- The feedback network does not consume power or store energy
- The power efficiency of the CD stage equals that of its controller, which is the biased CS stage.

Noise performance

The CD stage is a non-energic feedback stage.
- The feedback network does not add any noise, nor increase the noise contributions of its controller's noise sources
- The equivalent input noise sources of the CD stage equals those of its controller, which is the biased CS stage.

Offset and drift

The CD stage is a non-energic feedback stage.
- The feedback network that consists of a short in series with the signal path and an open circuit in parallel with the signal path does not contribute any offset or drift and it does not enlarge the offset and drift of the controller.
- The equivalent input offset sources of the CD stage equals those of its controller, which is the biased CS stage.

High loop gain drive and termination conditions

The CD stage is a feedback stage. If effective, output voltage sensing and input voltage comparison give this stage a relatively higher input impedance and lower output impedance than its controller: the CS stage.

Behavioral changes listed below are significant if the CD stage is driven from a low impedance and terminated with a high impedance.

Gain inaccuracy

The gain inaccuracy is reduced by (effective) negative feedback: it is smaller than that of its controller: the biased CS stage.

Weak nonlinearity

The weak nonlinearity is reduced by (effective) negative feedback: it is smaller than that of its controller: the biased CS stage.

Bandwidth

The bandwidth is enlarged by (effective) negative feedback: it is larger than that of its controller: the biased CS stage.

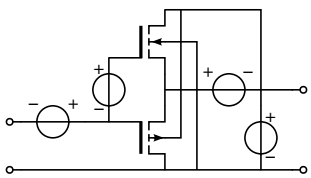
Conclusions for other drive and termination conditions

If shorted (terminated with a relatively low impedance) or current driven (driven from a relatively high impedance), the loop gain becomes very low and the feedback is not effective.

Combine multiple error-reduction techniques

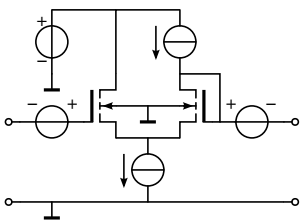
Negative feedback and balancing

Complementary parallel CD stage:
A voltage follower with a high current drive capability at a low quiescent current:



Balancing and negative feedback

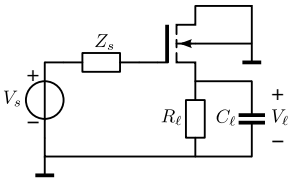
An anti-series CS stage as controller:
A voltage follower with a low offset:



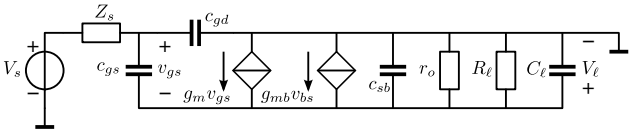
Note

Use isolated bulk transistors with bulk-source connected for improved low-frequency performance.

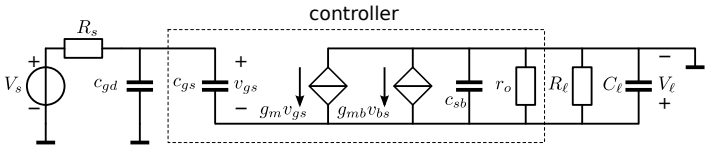
Negative feedback voltage follower with RC load



Signal path diagram
and
small-signal equivalent circuit.



Study of dynamic behavior using the asymptotic-gain feedback model



Ideal gain and asymptotic gain

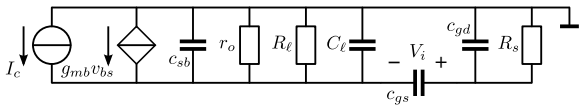
Placing the drain-gate capacitance outside the cortroller changes the ideal gain.

$$A_i = \left.\frac{V_\ell}{V_s}\right|_{\text{controller=nullor}} = \frac{1}{1+sR_s c_{gd}} \text{ [-]}.$$

Selection of the transconductance of the MOS as loop gain reference makes the asymptotic-gain equal to the modified ideal gain

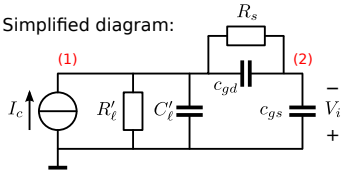
$$A_{f\infty} = \left.\frac{V_\ell}{V_s}\right|_{A\to\infty} = \frac{1}{1+sR_s c_{gd}} \text{ [-]}.$$

Loop gain



$$L = A\lambda\beta\kappa = -g_m\lambda\beta\kappa \qquad \lambda\beta\kappa = \left.\frac{V_i}{I_c}\right|_{V_s=0}$$

Simplified diagram:



$$\frac{1}{R'_\ell} = g_{mb} + \frac{1}{r_o} + \frac{1}{R_\ell}$$

$$C'_\ell = C_\ell + c_{sb}$$

DC loop gain

$$L_{DC\,\max} = -\frac{g_m}{g_{mb}+g_o} = -\frac{1}{n-1+\frac{1}{\mu}}$$

The substrate effect (backgate effect) introduces a strong reduction of the loop gain

Poles and zeros of the loop gain

$$L = -\frac{R'_\ell g_m (1+sR_s c_{gd})}{1+s\left(R_s(c_{gd}+c_{gs})+R'_\ell\left(C'_\ell+c_{gs}\right)\right)+s^2 R'_\ell R_s\left(c_{gd}c_{gs}+C'_\ell c_{gd}+C'_\ell c_{gs}\right)}$$

Study the influence of the drain-gaite capacitance seperately:

assume: $c_{gd} \ll c_{gs}$ and $c_{gd} \ll C'_\ell$

Calculate the two poles from their product and from their sum:

$$p_1 p_2 = \frac{1}{R'_\ell R_s C'_\ell c_{gs}} \qquad p_1 + p_2 = -\frac{1}{R'_\ell C'_\ell} - \frac{C'_\ell + c_{gs}}{R_s C'_\ell c_{gs}}$$

Both poles are dominant if their squared sum is smaller than four times their product.
Both poles are in MFM positions if their squared sum equals two times their product.
Compensation for MFM is possible if their squared sum is smaller than two times their product.

Achievable bandwidth

$$B = \sqrt{(1-L_{DC})\,p_1 p_2} \approx \sqrt{\frac{2\pi n f_T}{R_s C'_\ell}} \text{ [rad/s]}$$

Frequency compensation

The drain-gate capacitance introduces a left half-plane phantom-zero.
It can be increased with an external capacitor for frequency compensation or bandwidth limitation.