Structured Electronics Design

A systems engineering approach
to the design of electronic circuits

Solidly based on

- Systems Engineering
- Device physics
- Signal processing
- Network theory
- Control theory

History

1980: Ernst H. Nordholt:
Design of High-Performance
Negative-Feedback Amplifiers

1989: Catena Micro Electronics Delft,
Product Partners Delft, TU Delft, IMS
Stuttgart: Analog Electronics Design
Course, COMETT program EU.

2003: C.J.M Verhoeven, A. van Staveren,
G.L.E. Monna, M.H.L. Kouwenhoven, E. Yildiz:
Structured Electronic Design

2018: A.J.M. Montagne: Structured Electronics
Design

Benefits

- Straightforward top-down design
- Specification driven
- Early identification of design risks
- Solid basis for analog design education
- Solid basis for algorithmic design automation

Characteristics

- Hierarchically structured design process
- Identical process flow at each level
- Circuit design put in the perspective of information processing
- Clear relation between application, requirement specification and design
- Clear distinction between theoretical concepts and their technology-specific implementation
- Takes concepts and their technology-specific implementation, rather than known circuit topologies as starting point for the design.
- Puts circuit analysis in the perspective of design synthesis.
- Provides clear goals for circuit optimization.

Design tools SLiCAP

Symbolic **Li**near **C**ircuit **A**nalysis **P**rogram

A python application for deriving and solving design equations of electronic circuits.

Symbolic and numeric determination of design equations, show-stopper values, and design budgets for:

- DC variance and temperature dependency of component values
- Noise contributions of transistors, resistors, current and voltage sources
- Bandwidth / settling time
- Frequency response

Includes MOS (EKV) model and BJT (Gummel-Poon) model.

Symbolic and numeric pole-zero analysis.

Root-locus plots

Design education tools

Currently under development at the TU Delft.

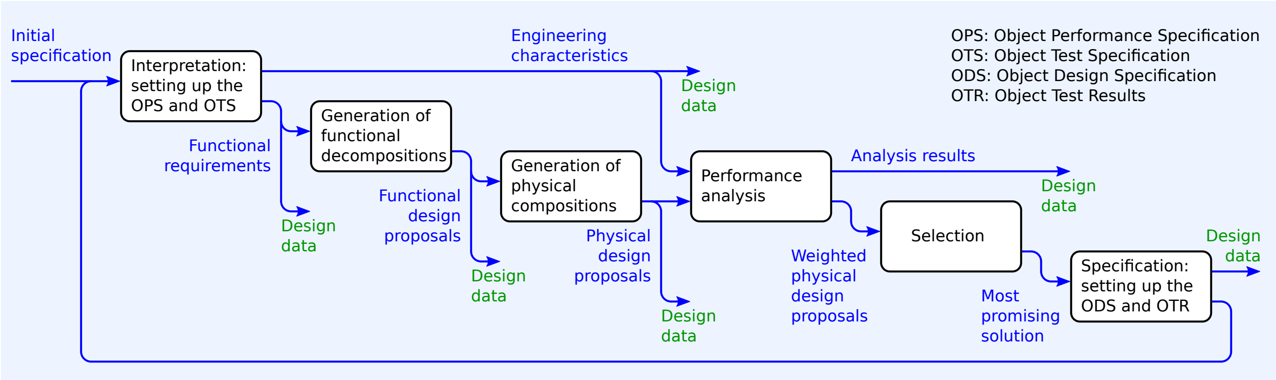
A computer-based learning system for analog circuit design.

Hierarchical design process

Identical structure at each level

Input:
Initial specification of object to be designed
At highest level:
Application description

Output:
Design data
Initial specification of next level objects
At lowest level:
Final specification of object(s)



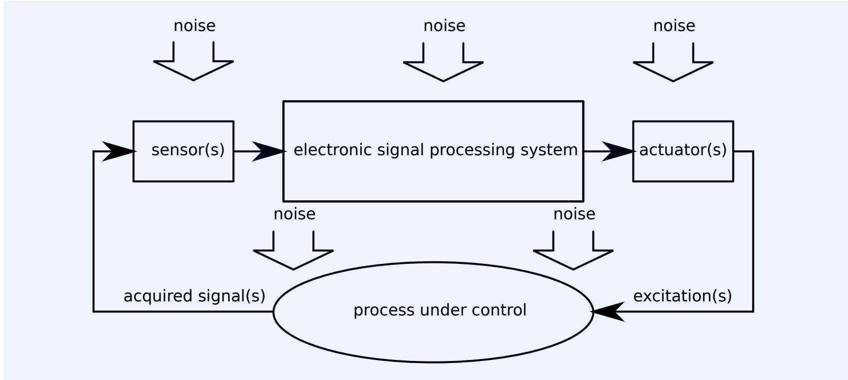
Requirement specification

- Functions
- Performance
- Environment
- Costs
  - time
  - space
  - matter
  - energy

Figure Of Merit

$$\mathrm{FOM} = \frac{\text{Weighted product of performance measures}}{\text{Weighted product of cost factors}}$$

Put the design of electronic circuits in the perspective of information processing



Electronic information processing systems can be constructed from a limited number of:

Basic references and processing functions / objects

Function	Materialization	Object
Reference in V-I domain		Voltage of current source
Reference in frequency domain	Physical operating principle in technology	Harmonic oscillator
Reference in time domain		Timer
Impedance matching		Transformer / matching network
Increase of available signal power		Amplifier
Selection in V-I domain		Comparator / limiter
Selection in frequency domain		Filter
Selection in time domain		Switch
Memorize		Memory

Materialization: create objects that perform functions

G.P. Box:
All models are wrong,
but some are useful.

Model the desired functional (ideal) behavior.

Find an operating mechanism that can be used for the materialization of this function in an available technology.

A. Einstein:
Models should be as simple as possible, but not simpler!

Model the physical (nonideal) behavior.

Evaluate performance limitations and cost factor limitations.

Evaluate interaction between performance aspects and between performance aspects ans cost factors.

A model should provide an answer to a question.

Evaluate the application of design techniques (see below) for improvement of the performance-cost ratio.

The amount of information that can be processed by an object is limited

Channel capacity Shannon (1948) $C = B\log_2\frac{P+N}{N}\left[\frac{\mathrm{bit}}{\mathrm{s}}\right]$

Fundamental limitations

The information processing capacity [bits/s] of physical systems is limited

- addition of noise
- power limitation
- speed (bandwidth, rate of change) limitation

Technological limitations

Imperfect, incomplete, or unavailable materialization of the desired function

- insufficient performance
- high costs

Design techniques

A collection of techniques that can be applied to
- improve performance
- reduce the costs

Types of design techniques
- optimization of physical implementation
  - scaling of dimensions
  - changing of operating point
- modification of physical implementation
  - changing of device
- modification of functional decomposition
  - application of design techniques

Examples
- isolation
- compensation
- balancing
- feedback
- auto-zeroing
- modulation
- sampling
- quantization

Design risk management

Show stopper

A performance aspect or cost factor that cannot be realized under the given constaints.

Identify at earliest possible stage

Impact on the predictability of the design process increases each stage

No propagation of design risks

Design risks identified at a hierarchical level must be resolved at that level

No design loops

Only take design decisions if necessary

Orthogonalize design techniques - performance requirements

Seminar Program Structured Electronics Design

Structured Design of Negative Feedback Amplifiers

1. Introduction
2. Specification and design of amplifier type
3. Specification and design of drive capability and noise performance
4. Specification and design of accuracy, bandwidth and weak nonlinearity
5. Specification and design of small-signal dynamic response
6. SLiCAP a design tool that supports Structured Electronics Design
7. Example design in PCA technology: Audio Hearing Loop
8. Structured Electronics Design in CMOS technology
9. Structured Electronics Design in CMOS technology
10. Example design in CMOS technology: CMOS active receiver antenna (0.1-30 MHz)
    Conclusions: Analog Design education and automation

Design the design process

Requirements

- Identical structure at each hierarchical level
- Show stoppers appear at the earliest possible stage
- No risk propagation, no design loops

Orthogonalization

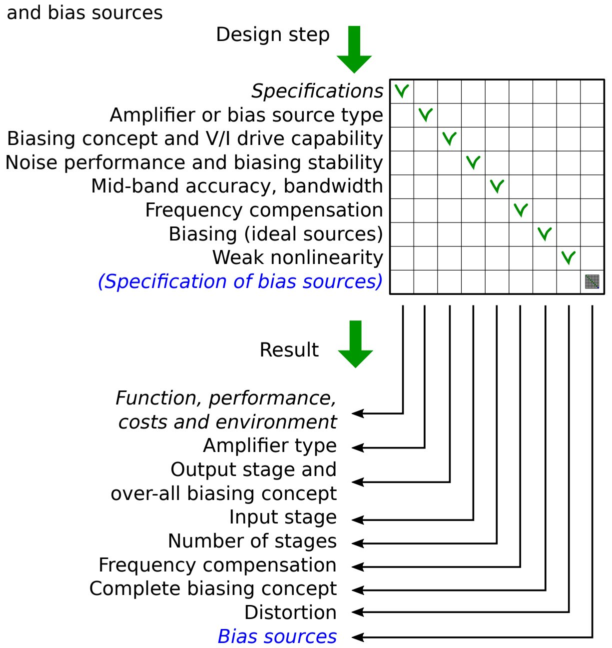
- Create degrees of freedom for realizing functions and their characteristic performance aspects.
- Separate them in:
  - parameters - frequency range
  - time - location

Sequencing of activities

The sequence of the design activitie should be such that
- Show stoppers appear at the earliest possible stage:
  - Materialization of a function in the desired technology is not available
  - The required performance-cost ratio cannot be achieved within the required constraints:
    There is no design technique capable of
    - improving a performance aspect to a sufficient quality level
    - reducing a cost factor to an acceptable level
- Design decisions taken at one stage need not to be reconsidered at a later stage

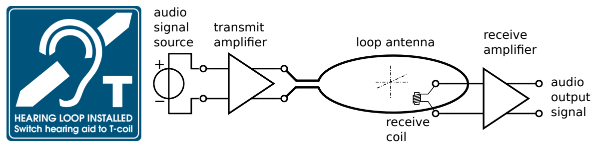
IC Amplifier Design Process

Stepwise approach to the design of negative feedback amplifiers and bias sources



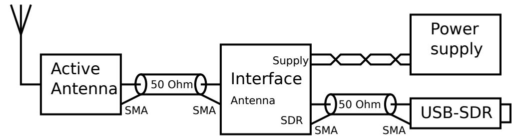
Example Designs

TU Delft BSc course EE3C11



Specification, design, build, and test of an audio hearing loop system in PCA technology.

TU Delft MSc course



Specification, design, and verification by simulation of an active antenna for receivers with a frequency range of 0.1 - 30 MHz..