EE4109 Structured Electronics Design

Design of application-specific amplifiers in CMOS technology

1. Application Description

The design starts with a study of the application description.
The result of this study is the designer's interpretation of this description in the form of a performance and test specification

2. Performance and Test Specification

The performance specification gives measurable quantities for

1. Performance aspects of the amplifier, such as,
   - Noise performance
   - Drive capability
   - Bandwidth and frequency response
   - Weak nonlinearity
2. Environmental conditions under which this performance must be achieved
   - Signal source specification
   - Load specification
   - Temperature range
   - EMI and ESD conditions
3. Available resources for the amplifier
   - Power supply specification
   - Chip area and available packages
   - PCB area and external components
4. More:
   - Interaction with environment (emitted radiation, temperature rise)
   - Safety
   - Reliability

The test specification describes the test methods and tools, or applicable standards for the quantities described above.

3. Feedback configuration and biasing concept of the amplifier

1. Which electrical quantities can be used at the input and at the output of the amplifier?
2. Which combinations of (zero, non-zero) transmission-1 matrix parameters can be used?
3. In which way can these parameters be fixed with negative feedback?
4. Is there, on grounds of the performance requirements a preference for a specific solution?

4. Technology noise (offset) performance

The equivalent input noise sources and the equivalent-input offset and offset drift of a negative feedback amplifier can at best equal those of its controller. If the feedback networks are not non-energic, these equivalent input sources of the feedback amplifier will be larger than those of the controller. This effect can be studied with simple models.
If the controller is designed with cascaded nullor-like stages (CS or balanced CS) these equivalent input sources can at best equal those of the input stage of the controller.
Application of transformers or noise matching networks may be considered.
Considering noise and offset, the technology may introduce show stoppers and set limits to the device geometry, the operating conditions, and the use of transformers or matching networks.

5. Technology drive capability

The drive capability of a feedback amplifier at best equals that of its controller. If the feedback networks are not non-energic, the drive capability of the feedback amplifier will be lower than that of the controller. This effect can be studied with simple models.
If the controller is designed with cascaded nullor-like stages (CS or balanced CS) the drive capability of the controller at best equals that of its output stage.
Application of transformers or power matching networks may be considered.
Considering the drive capability, the technology may introduce show stoppers and set limits to the device geometry, the operating conditions, and the use of transformers or matching networks.

6. Number of controller stages

In negative feedback amplifiers:

1. The mid-band gain accuracy can be increased by increasing the mid-band value of the loop gain
2. The bandwidth can be increased by increasing the product of the mid-band loop gain and the dominant poles
3. The weak nonlinearity can be decreased by decreasing the diferential-error-to-gain ratio

This all can be done by increasing the number of stages and by:

1. Maximizing the contribution of each stage to the mid-band value of the loop gain
2. Maximizing the contribution of each stage to the product of the mid-band loop gain and the poles
3. Minimizing the contribution of each stage to the differential-error-to-gain ratio of the loop gain

This all can be achieved by:

1. Not inserting impedances in series or in parallel with the signal path
2. Use cascoded CS or balanced cascoded CS stages.

If the bandwidth is too close to the process cut-off frequency, a feedback amplifier is not feasible.
If the number of dominant poles exceeds four, frequency compensation may become too difficult and the amplifier may be designes as two cascaded feedback amplifiers

7. Structure of controller and feedback network

The stages in the controller must be cascaded properly:
- The input of subsequent stages is connected to the output port of preceeding stages.
Four-terminal controllers can be connected in two different ways to their environment.

8. Frequency compensation of the amplifier

The following frequency compensation techniques can be applied (order of preference)

1. Phantom zero compensation
2. Pole-splitting by increasing the interaction between two poles
3. Pole-splitting by pole-zero canceling
4. Resistive broadbanding
5. Manipulatie dominant pole(s) out of the dominant group (bandwidth reduction)
   - Reduction of the mid-band loop gain (resistive broadbanding or local feedback)
   - Exessive pole-splitting
   - Increasing the time constant of a more dominant pole

9. Biasing concept of the controller

1. Add ideal bias sources (LTspice) to the signal path of the controller and use the over-all biasing concept from step (3).
2. Optimize the concept: minimize the number of floating voltage sources, and combine current sources.
3. Check the performance and compare it with that of the signal path (SLiCAP, step (8))
4. Make adjustments if necessary.

10. Weak nonlinearity check

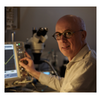
Check the weak nonlinearity (differential-gain, differential phase, IMD, THD) if not within spec:

1. Check signal excursions and if necessary, adjust bias voltages and currents.
2. If the above does not give the desired results:
   - Try to compensate for nonlinearity
   - Increase the loop gain, it may be necessary to add another stage (see step(6))

11. Step-by step implementation of bias sources

For all bias sources:

1. Find budgets for biasing parasitics, biasing errors and added noise of bias sources (SLiCAP)
2. Find budgets for requires voltage swing across current sources and current excursions through bias voltage sources (LTspice, step (10))
3. Performance specification of bias source
4. Design voltage or current bias source according to this specification
5. Verify the behavior of the bias source
6. Add it to the controller
7. Verify the amplifier performance, and if necessary, make adjustments.

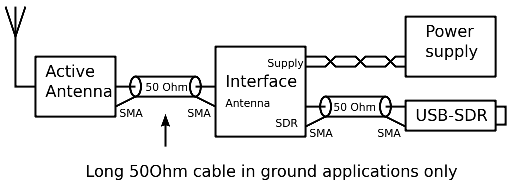


(c) 2021 Anton Montagne
anton@montagne.nl
https://www.analog-electronics.eu

Design Active Antenna for radio astronomy in CMOS18 technology

1. Application Description

10kHz ... 30MHz



Long 50Ohm cable in ground applications only

2. Performance specification

Antenna length: max 0.5m
E-field antenna-referred noise:

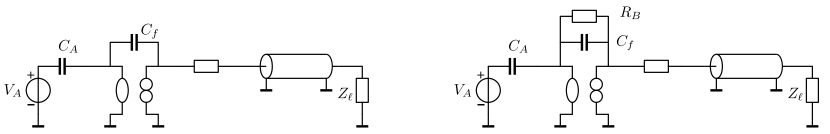
10kHz	: 100n	$\left[\frac{\mathrm{V}}{\mathrm{m}\sqrt{\mathrm{Hz}}}\right]$
100KHz	: 10n	
1MHz	: 5n	
30MHz	: 5n	

Antenna gain (-3dB: 10kHz-30MHz)
0dB

IM distortion:
-50dB: 10kHz-30MHz
Output 1dB compression level:
0dBm in 50Ohm
Temperature range:
-25 ... +70 deg Celsius

Power supply:
1.8V
Power dissipation:
< 30mW
ESD discharge protected

3. Feedback configuration and biasing concept of the amplifier

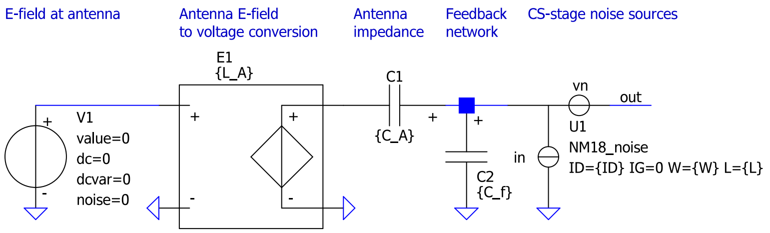


$C_A = 5\mathrm{pF}$

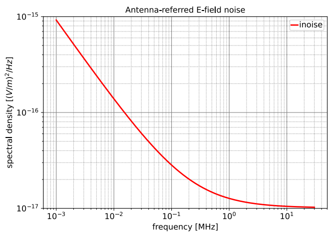
$C_f = \frac{1}{2}C_A$

$R_B > \frac{1}{2\pi 10^4 C_f}$

4. Technology noise (offset) performance



```
.include C18.lib
.param C_A={L_A*C_0} L_A=0.5 C_0=10p C_f={C_A/2}
```

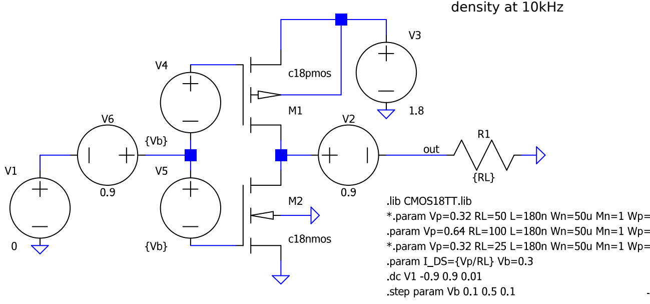


$$S_E = \left(5\cdot 10^{-9}\right)^2\left(1+\left(\frac{2\cdot 10^5}{f}\right)^2\right) \qquad R_B > \frac{4kT}{S_E\left(L_A 2\pi 10^4 C_A\right)^2} = 67\mathrm{M}\Omega$$

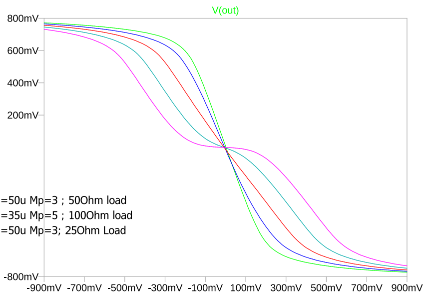
antenna-referred spectral density at 10kHz

ID=600u, W=350u, L=180n

5. Technology drive capability



```
.lib CMOS18TT.lib
*.param Vp=0.32 RL=50 L=180n Wn=50u Mn=1 Wp=50u Mp=3 ; 50Ohm load
.param Vp=0.64 RL=100 L=180n Wn=50u Mn=1 Wp=35u Mp=5 ; 100Ohm load
*.param Vp=0.32 RL=25 L=180n Wn=50u Mn=1 Wp=50u Mp=3; 25Ohm Load
.param I_DS={Vp/RL} Vb=0.3
.dc V1 -0.9 0.9 0.01
.step param Vb 0.1 0.5 0.1
```



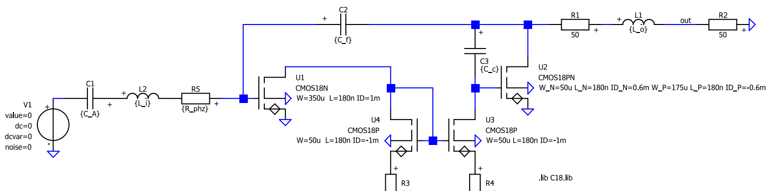
6. Number of controller stages

1. Single-stage controller, push-pull stage (complementary parallel CS stage)
   - Noise: OK
   - Drive capability: OK
   - Bandwidth: OK
   - Weak nonlinearity NOT OK
2. Two-stage controller with larger mid-band loop gain for improved accuracy and linearity

7. Structure of controller and feedback network

1. CS input stage
2. Complementary parallel CS output stage
3. Unity gain inverting current amplifier intermediate stage (not counted as stage because it does not contribute a dominant pole and not increase the mid-band loop gain)

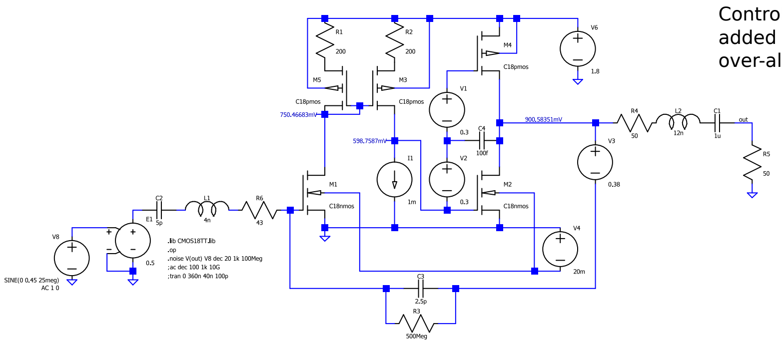
8. Frequency compensation of the amplifier



```
.lib C18.lib
```

1. Bandwidth about 1 GHz
2. Input and output phantom zeros
3. Pole splitting in output stage

9. Biasing concept of the controller



```
.lib CMOS18TT.lib
.op
.noise V(out) V8 dec 20 1k 100Meg
;ac dec 100 1k 10G
;tran 0 360n 40n 100p
```

Controller biased with ideal sources added to feedback configuration with over-all feedback biasing.

10. Weak nonlinearity check

In-band IMD of the above cofiguration OK!

11. Step-by step implementation of bias sources

Complete circuit
step-by-step on separate poster.