

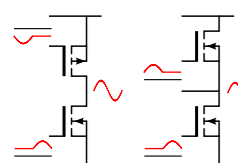
# Class AB amplifiers with OpAmps and discrete transistors

## Class AB output stage

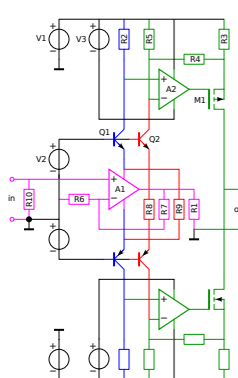
### Rail to rail output

- Complementary output
- Source P devices
- Sink N devices

Quasi complementary output  
- All N devices with isolated source drive

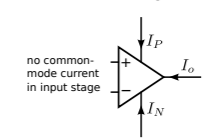


### Class AB power current driver



### Stable bias

- Copy biasing from opamp
- Measure and control the bias (feedback biasing)

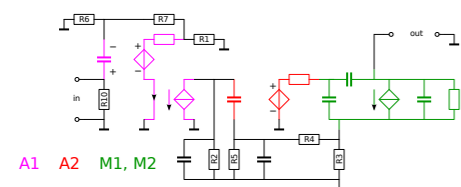


$$I_P + I_N + I_o = 0$$

$$I_P \approx \frac{1}{2} (\text{sgn} I_o + 1) I_o + I_Q$$

$$I_N \approx \frac{1}{2} (\text{sgn} I_o - 1) I_o - I_Q$$

### Small-signal equivalent circuit



### Modeling aspects

Bandwidth limitation of BJT can be modeled in the CCCS  
Output capacitances Q1 and Q2 added to CM input capacitance of A2  
Dynamic behavior can be investigated for different values of source, sink, or quiescent current:

Parameterize component values of small-signal MOS model  
Use different parameter sets for source, sink or quiescent behavior  
Model the current dependency of the MOS transconductance

### Reduction of offset and even-order distortion

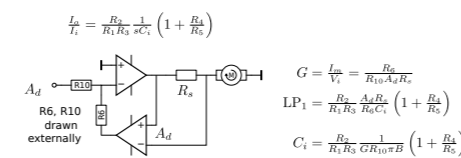
Apply over-all feedback

Convert power current driver into integrator

Replace R7 with integration capacitor

Create feedback path with current sense resistor and difference amplifier

$C_i$  Integration capacitance  
 $R_a$  Resistance of current-sense resistor  
 $A_d$  Voltage gain of difference amplifier

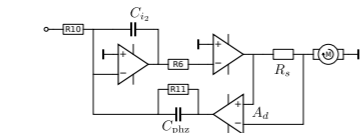


The loop gain in the main amplifier of the power current driver is proportional with the integration capacitance

A large bandwidth can be obtained using an extra integrator. Use a dual integrator with phantom zero for a low-distortion, wide-band class AB driver.

Design the circuit such that all other poles are non-dominant. Frequency compensation in the power transconductance stages can be accomplished with a phantom zero:

- Capacitor across R4
- Inductor in series with R3



$$G = \frac{I_{cm}}{V_i} = \frac{R_{11}}{R_{10} A_d R_a}$$

$$LP_2 = \frac{R_2}{R_1 R_3} \frac{A_d R_a}{4\pi^2 R_{10} C_i} \left(1 + \frac{R_a}{R_5}\right) \quad B = \frac{1}{2\pi} \sqrt{LP_2}$$

$$C_{i2} = \frac{R_2}{R_1 R_3} \frac{R_a}{4\pi^2 R_{10} C_i} \left(1 + \frac{R_a}{R_5}\right) \quad C_{phz} = \frac{1}{\sqrt{2\pi} B R_{11}}$$

### Design sequence

- Select the power transistors; consider drive capability, dissipation and cooling.
- Select current sense resistor and divergence amplifier; consider noise and offset (drift) for the amplifier and power dissipation and temperature coefficient for the sense resistor.
- Assume reasonable budgets for quiescent current and current drive capability for the main opamp and design R2 and the power transmittance with a bandwidth at least five times larger than the required bandwidth of the total circuit.
- Design the main amplifier consider the drive requirements for R1 (no voltage or current clipping or slow-rate limitation) for R1 (no voltage or current clipping or slow-rate limitation)
- Design R6 and the integration capacitance such that the integrator bandwidth (servo function) is at least five times the required bandwidth for the complete circuit.
- Select the BJTs (power dissipation)
- Design the first integrator.

### High-voltage class AB output stages

- High-voltage Si or SiC transistors
- Stacked transistors
- Isolated drivers

### CRETE

#### C2M1000170D

#### Silicon Carbide Power MOSFET

#### C2M™ MOSFET Technology

#### N-Channel Enhancement Mode

- High Speed Switching with Low Capacitance
- High Blocking Voltage with Low Field
- Easy to Parallel and Series to Drive
- High Voltage Capacitor Compatible
- Energy Free, Rugged Construct

- Higher Switch Efficiency
- Resonant System Switching Frequency
- Reduced Ringing Phenomena
- Increased System Reliability

- Auxiliary Power Supplies
- Brush Motor Power Supplies
- High-End Drive Controller

Maximum Ratings (V, +25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V <sub>DS</sub>	Drain-Source Voltage	1700	V	V <sub>GS</sub> =0V, I <sub>D</sub> =0A	
V <sub>DS</sub>	Drain-Source Voltage	>+10V	V	Absolute maximum value	
V <sub>DS</sub>	Drain-Source Voltage	>+10V	V	Recommended maximum value	Fig. 14
I <sub>D</sub>	Continuous Drain Current	3.5	A	V <sub>GS</sub> =20V, V <sub>CE</sub> =10V	Fig. 23
I <sub>D</sub>	Peak Drain Current	6.0	A	Pulse with I <sub>D</sub> limited by T <sub>DM</sub>	Fig. 23
P <sub>tot</sub>	Power Dissipation	60	mW	T <sub>case</sub> =25°C, V <sub>GS</sub> =10V	Fig. 20
T <sub>j</sub>	Operating Junction and Storage Temperature	-40 to 150	°C		
T <sub>stg</sub>	Storage Temperature	-55 to 175	°C		
M <sub>t</sub>	Mounting Torque	0.8	Nm	M3 in M3 screw	

### CRETE

#### C2M1000170A

#### Silicon Carbide Power MOSFET

#### C2M™ MOSFET Technology

#### N-Channel Enhancement Mode

- High Speed Switching with Low Capacitance
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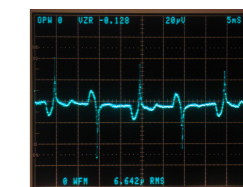
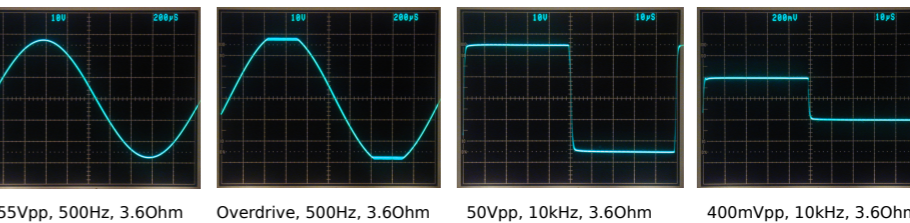
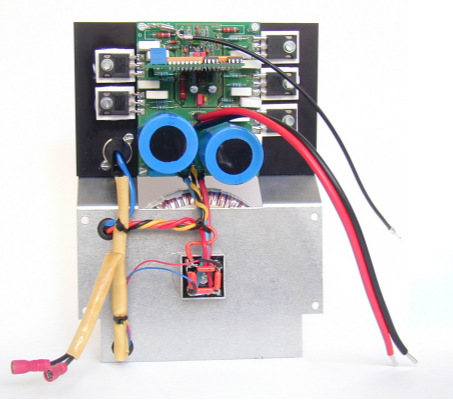
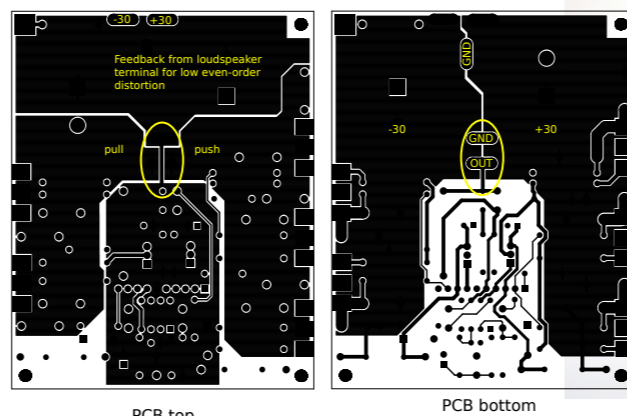
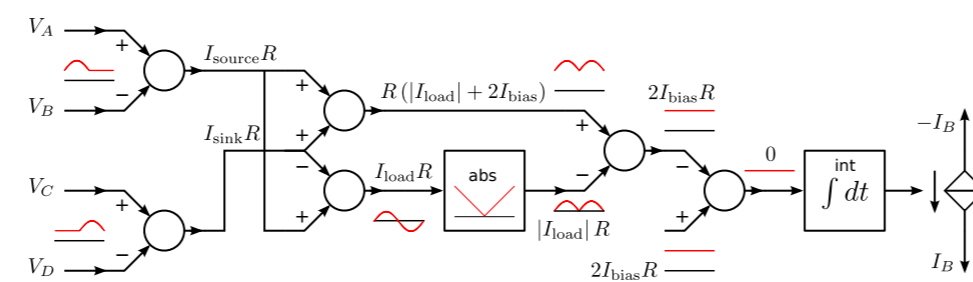
Maximum Ratings (V, +25°C unless otherwise specified)

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V <sub>DS</sub>	Drain-Source Voltage	>+10V	V	Recommended maximum value	Fig. 14
I <sub>D</sub>	Continuous Drain Current	3.5	A	V <sub>GS</sub> =20V, V <sub>CE</sub> =10V	Fig. 23
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T <sub>j</sub>	Operating Junction and Storage Temperature	-40 to 150	°C		
T <sub>stg</sub>	Storage Temperature	-55 to 175	°C		
M <sub>t</sub>	Mounting Torque	0.8	Nm	M3 in M3 screw	

#### Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V <sub>SD</sub>	Drain-Source Voltage	0.8	1.8	V	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =25°C	
I <sub>S</sub>	Static Drain Current	0.1	1.0	mA	V <sub>GS</sub> =0V, V <sub>SD</sub> =0.8V, T <sub>j</sub> =25°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =25°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =100°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =150°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =175°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =200°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =225°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =250°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =275°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =300°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =325°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =350°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =375°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =400°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =425°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =450°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =475°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =500°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =525°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =550°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =575°C	Fig. 5, 6
r <sub>SD</sub>	Drain-Source Resistance	0.1	0.2	Ω	V <sub>GS</sub> =0V, I <sub>D</sub> =0A, T <sub>j</sub> =600°C	Fig. 5, 6

### Analog Bias Computation and Control



#### Technical specifications

Voltage amplification factor	≥ 22 V/V
Charge time (voltage controlled)	< 20 μs @ 10V
Output noise level (DIN A weighted)	< 150 dBu
DC output voltage (input shorted)	< 20 dBu
SMV small-signal bandwidth	0.200 MHz
Nominal output voltage for 40W RMS at 1 Ohm	< 1 Vrms
Total Harmonic Distortion (A, B, C, W, F, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z)	< 50 dB (0.01%)
Output impedance at 1 kHz	43 mΩ
Damping factor at 1 kHz	60 dB
Power bandwidth (1 kHz)	40 kHz
Peak output current (source and sink)	> 40 A
Main voltage (factory selected)	110/220 Vrms
Main frequency	50/60 Hz
Power consumption (no signal)	2 A
Main fuse 230V version (low loss IEC127)	1 A
Main fuse 115V version (low loss IEC127)	2 A
Humank temperature for mains switch-off	70 °C
Humank temperature for mains recovery	25 °C
Humank temperature recovery time (typical)	600 s
Dimensions (WxDxH)	165 x 130 x 231 mm
Weight	1 kg

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