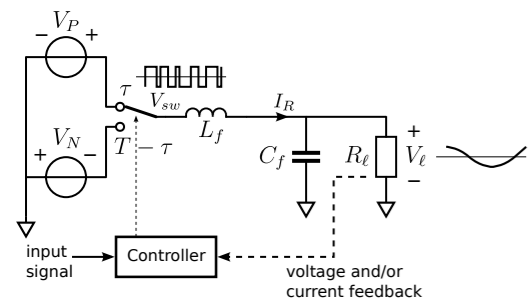
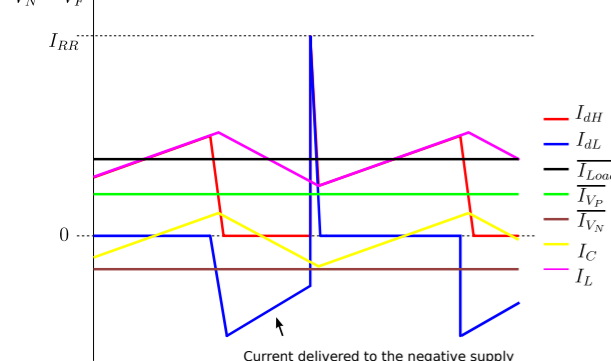
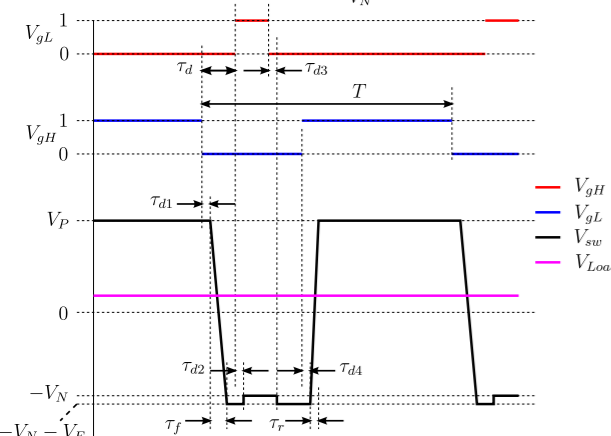
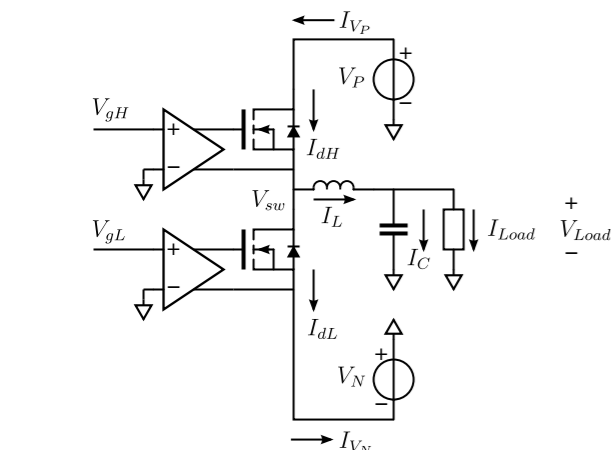


# Class D amplifier design

## Half-bridge operating principle



## Half-bridge switching behavior and power losses



**VISHAY** **Si7454FDP**  
Vishay Siliconix

### N-Channel 100 V (D-S) MOSFET

**FEATURES**

- TrenchFET™ Gen IV power MOSFET
- Very low  $R_{DS(on)}$  x  $Q_g$  figure-of-merit (FOM)
- Tuned for the lowest  $R_{DS(on)}$  x  $Q_{oss}$  FOM
- 100%  $R_{\theta(jc)}$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc298912](http://www.vishay.com/doc298912)

**APPLICATIONS**

- Synchronous rectification
- Primary side switch
- DC/DC converters
- Power supplies
- Motor drive control

PRODUCT SUMMARY	
$V_{DS}$ (V)	100
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0295
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.034
$Q_g$ typ. (nC)	8
$I_D$ (A)	23.5
Configuration	Single

## Output voltage and ripple current

$$V_L = \frac{\tau}{T} (V_P + V_N) - V_N$$

$$V_S = V_P = V_N$$

$$\delta = \frac{\tau}{T}$$

$$V_L = V_S (2\delta - 1)$$

$$I_R = \frac{2V_S \delta (1 - \delta) T}{L}$$

$$I_R = \text{peak-to-peak value of the ripple current.}$$

Expressions for peak ripple current much smaller than load current

## MOS conduction losses

$$P_{CM} \approx I_{load}^2 R_{dsOn} \frac{T - 2\tau_d}{T} \quad R_{dsOn} = \text{MOS on resistance}$$

## Body diode conduction losses

$$P_{CD} \approx I_{load} V_F \frac{2\tau_d}{T} \quad V_F = \text{MOS body diode forward voltage at load current}$$

## Output charge losses

$$P_{OQ} \approx \frac{2}{T} Q_o (V_P + V_N)$$

or

$$P_{OQ} \approx \frac{2}{T} C_o (V_P + V_N)^2$$

$Q_o$  = MOS output charge

$C_o$  = MOS output capacitance

## Reverse recovery losses

$$P_{RR} = \frac{1}{T} Q_{RR} (V_P + V_N) \quad Q_{RR} = \text{MOS body diode reverse recovery charge}$$

## Switching losses

$$P_{sw} = \frac{2}{T} \int_0^{\tau_{sw}} (V_P + V_N) \left(1 - \frac{t}{\tau_{sw}}\right) I_{load} \frac{t}{\tau_{sw}} dt$$

$$= \frac{\tau_{sw} I_{load} (V_P + V_N)}{3T}$$

$C_{gd}$  = MOS gate-drain capacitance

$I_G$  = Gate driver current

$\tau_{sw} \approx \frac{C_{gd}(V_P + V_N)}{I_G}$

## Gate driver losses

$$P_G = \frac{1}{T} V_G^2 C_{iss}$$

or

$$P_G = \frac{1}{T} V_G Q_G$$

$V_G$  = Gate driver voltage

$C_{iss}$  = MOS input capacitance

$Q_G$  = MOS gate charge

## Low losses and low EMI during quiescent operation:

Resonant switching:

$$I_R \tau_d \approx 2 (V_P + V_N) C_{oss} \quad C_{oss} = \text{MOS output capacitance}$$

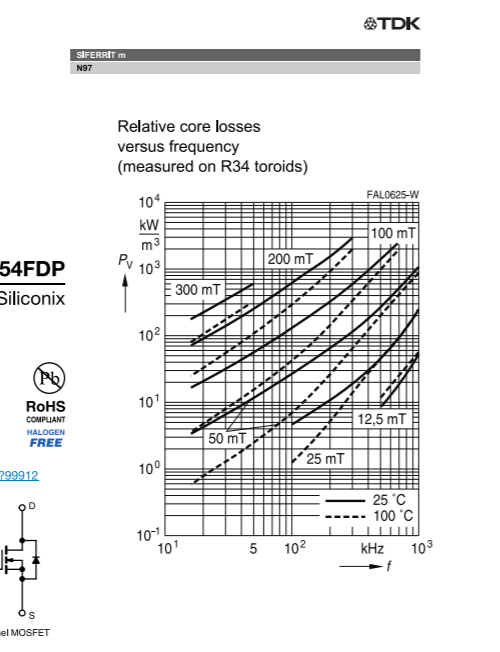
## FOM power devices:

Combine a low charge storage with a low on resistance.

## Core losses

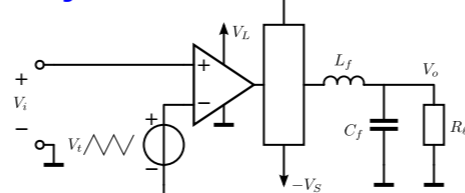
- Manufacturer's calculation tools

- Material specification:



## Fixed frequency PWM

### Voltage driver



$V_i$  = peak-to-peak value of triangular voltage

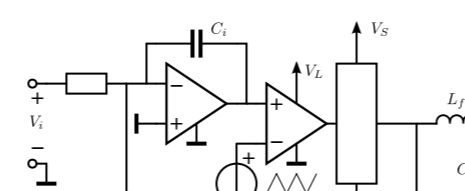
$Q_L$  = Quality factor of the load

$$\frac{V_o}{V_i} = \frac{2V_s}{V_L} \frac{1}{1 + \frac{s}{\omega_f} + \frac{s^2}{\omega_f^2}} \quad \omega_f = \text{Corner frequency of the filter}$$

Nonlinearity caused by:

- dead zone
- signal-dependent delay
- signal-dependent rise and fall times

Can be reduced through application of negative feedback



Small-signal bandwidth: first-order LP product:  $B_f = \frac{2V_s}{2\pi V_L R_i C_i}$

Large-signal stability: Rate of change at the output of the integrator should not exceed that of the triangular signal:  $f_{sw} > \pi B_f$

## Influence of timing noise in the MOS driver of the noise performance

Noisy PWM resulting from timing noise in the MOS driver.

Spectral density:  $S_r \left[ \frac{V^2}{\text{Hz}} \right]$

Equivalent voltage noise density spectrum at the input of the comparator:

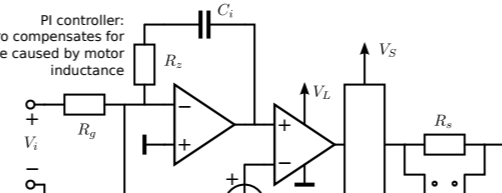
$$S_v = S_r \frac{V_L^2}{T^2} \left[ \frac{V^2}{\text{Hz}} \right]$$

In isolated MOS / IGBT drivers: spurious frequency components may be present.

## Current driver for inductive loads

Without output filter

PI controller: zero compensates for pole caused by motor inductance



High-frequency attenuation and damping of common-mode noise may be required

Compensation of the effect of a small cable capacitance requires two extra (complex) poles in the loop.

## With output filter

An output filter can be applied to:

- Relax the CMRR requirements and/or CM filter requirements for the current sense circuit

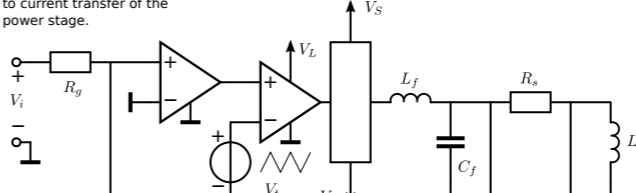
- Reduce the influence of high-frequency through the cable capacitance on the transfer

- Reduce emission levels

The output filter strongly complicates the design of the dynamic performance and the frequency stability of the current driver. An over sampling digital controller with integrated pulse width modulator may be a flexible and attractive alternative for an analog controller.

## Fixed ripple current PWM

### Hysteresis-based self-oscillating class D voltage driver



The effect of the cable capacitance can be reduced using remote sensing.

The effect of the cable capacitance and the motor capacitance can be reduced through application of capacitive voltage feedback at the load, thereby creating a negative output capacitance that compensates for the load capacitance.

$$Z_o = \frac{p}{c} = -\frac{A_d R_i}{s R_i A_v C_{comp}}$$

$C_{out} = -C_{comp} \frac{A_v R_i}{A_d R_o}$

A finite delay limits the gain at low frequencies:

$$V_i(t) = \frac{1}{2} V_H + \frac{V_H - V_L}{L_o} \frac{C_f}{C_f + C_o} R_H \tau_d$$

$$V_i(t) = -\frac{V_L}{L_o} \frac{C_f}{C_f + C_o} R_H \tau_d$$

$$V_i(t) = -\frac{1}{2} V_H - \frac{V_H + V_L}{L_o} \frac{C_f}{C_f + C_o} R_H \tau_d$$

actual operating point

quiescent operating point

output stage switching instants

The reduction of the low-frequency gain can be compensated for by inserting a capacitor in series with

For a low timing noise, construct the Schmitt-trigger with a low noise comparator with positive feedback.

$$\frac{V_a}{V_i} = -\frac{(C_f + C_o)L}{C_f \tau_d} \frac{1}{1 + s \frac{(C_f + C_o)L}{\tau_d}}$$

If the delay in the oscillator equals zero, the mean value of the voltage at the input of the comparator does not depend on the signal and the circuit behaves as an ideal transimpedance integrator:  $I'_R = -\frac{1}{sC_f}$

The output filter does not introduce (observable) complex poles in this transfer.

The DC transfer can be fixed accurately:

- Resistor in parallel with  $C_f$

- Extra feedback loop with non-inverting integrator (with a zero) for lower distortion

First stage: extra loop integrator

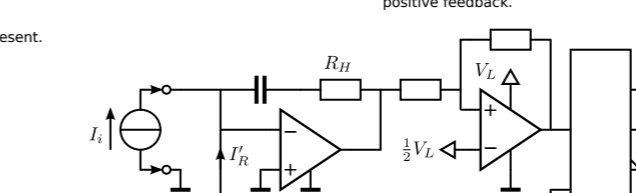
Second stage: Self oscillating class D transimpedance integrator (from figure above)

Simplified diagram

Putting it all together

Further detailing required

Improvement: differential voltage sensing



## Fixed frequency versus fixed ripple current driver

### Fixed frequency

Discrete EMI components with relatively high amplitude at harmonics of the switching frequency

Rail to rail operation limited by minimum pulse width

High efficiency

Difficult to obtain a desired frequency response because the poles of the output filter appear in the loop gain of the current control loop

### Fixed ripple current

Wide spectrum EMI with lower amplitude at unknown frequencies

Ripple voltage increases with voltage excursion

Switching frequency drops below Nyquist at large voltage excursions

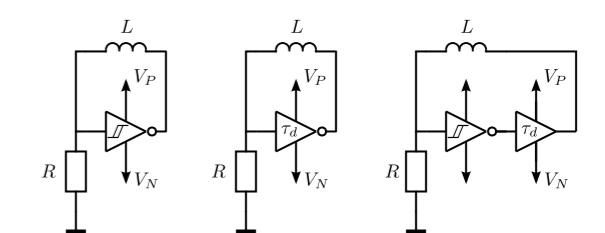
Higher efficiency because switching losses drop at large voltage excursions

Relatively easy to obtain a desired frequency response because the poles of the output filter do not appear in the loop gain of the current control loop.

## Fixed ripple current PWM

### Hysteresis-based self-oscillating class D voltage driver

#### First-order LR oscillators



Comparator with hysteresis

Comparator with delay

Comparator with delay and hysteresis

#### Basic operation

Schmitt-trigger switching levels:  $\pm \frac{1}{2} V_H$

Peak-to-peak value of the ripple current:

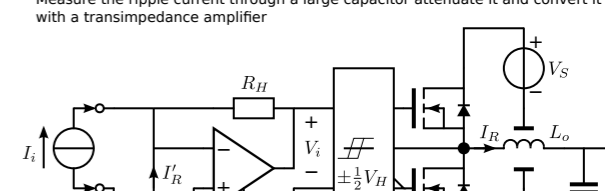
$$I_R = \frac{V_H}{L} + \frac{2V_S}{L} \tau_d$$

Oscillation frequency:

$$f = \frac{1}{T} = \frac{1 - \frac{V_H}{V_S}}{\frac{2LV_H}{RV_S} + 4\tau_d}$$

#### Alternative configuration

Measure the ripple current through a large capacitor attenuate it and convert it into a voltage with a transimpedance amplifier



If the delay in the oscillator equals zero, the mean value of the voltage at the input of the comparator does not depend on the signal and the circuit behaves as an ideal transimpedance integrator:  $I'_R = -\frac{1}{sC_f}$

The output filter does not introduce (observable) complex poles in this transfer.

The DC transfer can be fixed accurately:

- Resistor in parallel with  $C_f$

- Extra feedback loop with non-inverting integrator (with a zero) for lower distortion

First stage: extra loop integrator

Second stage: Self oscillating class D transimpedance integrator (from figure above)