Structured Electronic Design

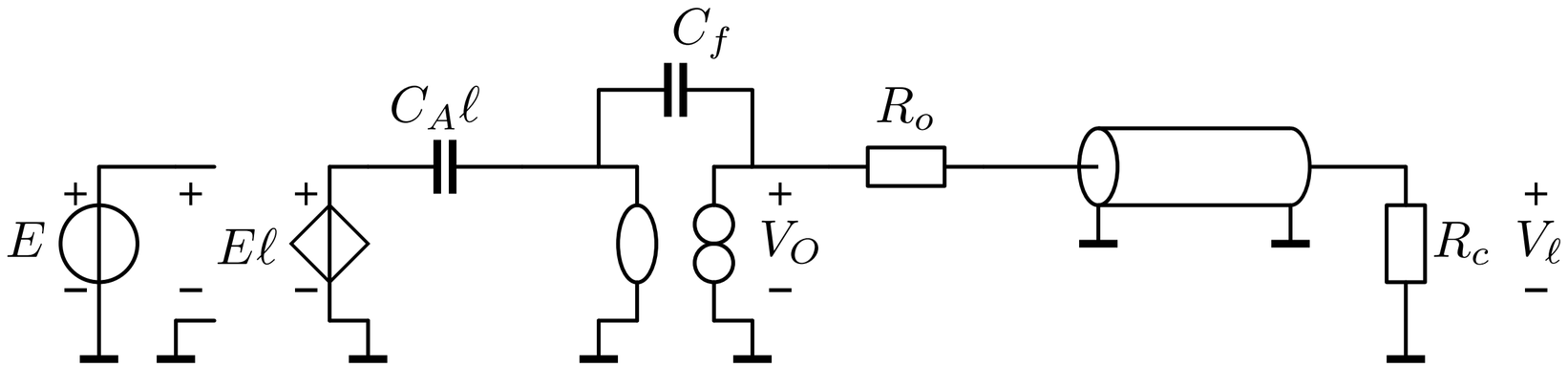
EE4109
Design of the signal path
of the active antenna

Anton J.M. Montagne

Amplifier configuration

Amplifier configuration

Design ideal gain



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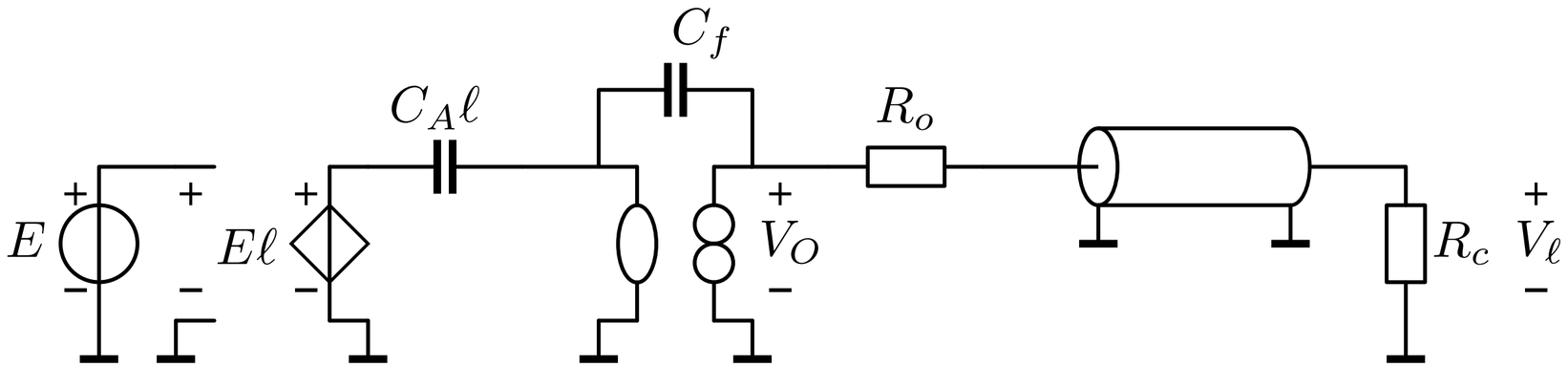

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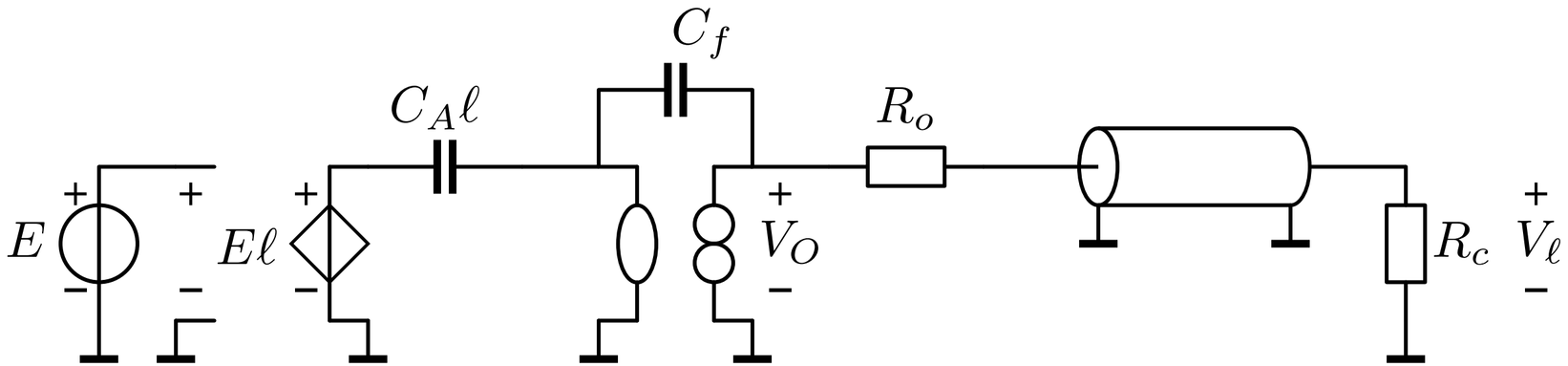

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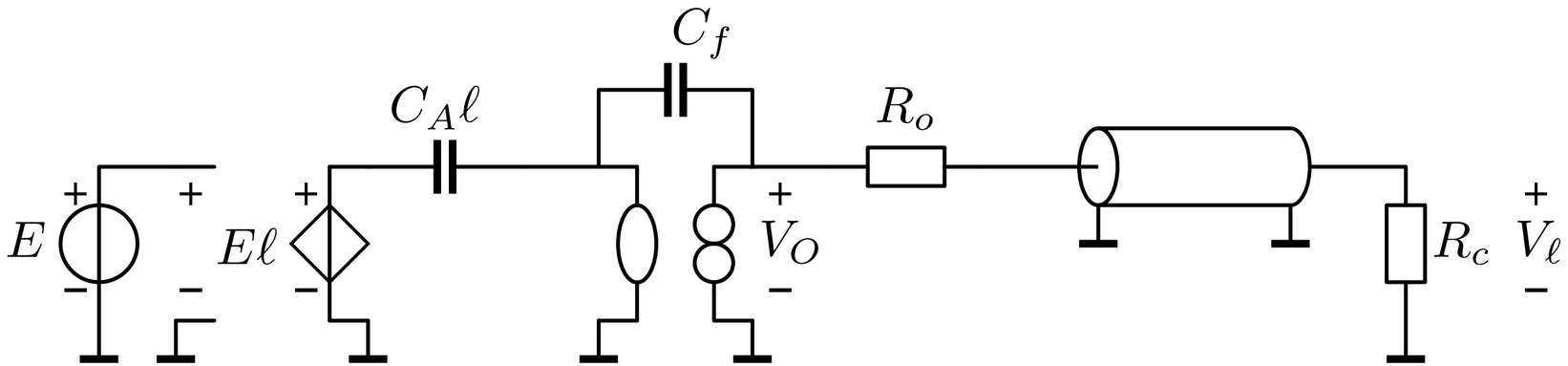

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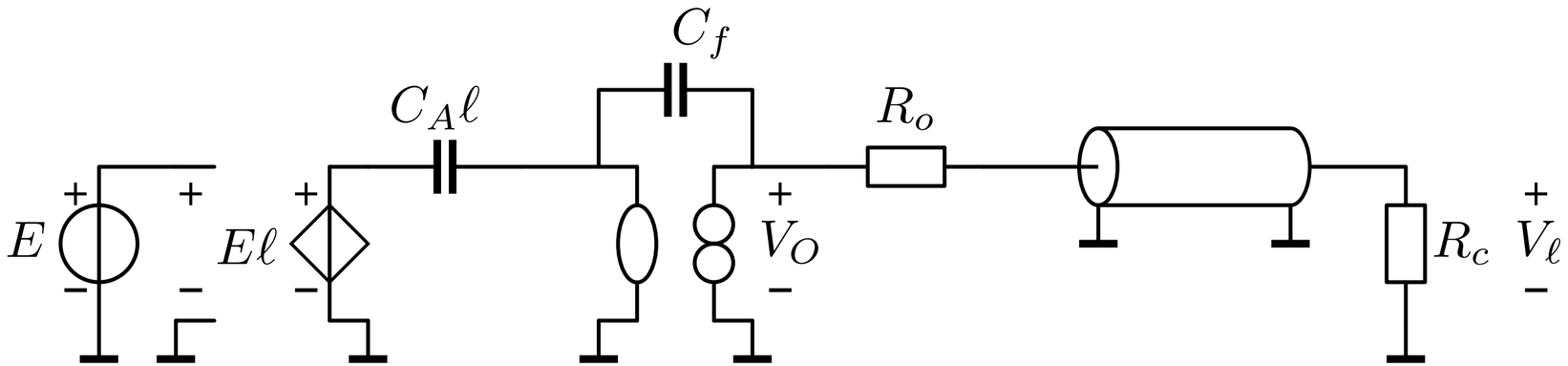

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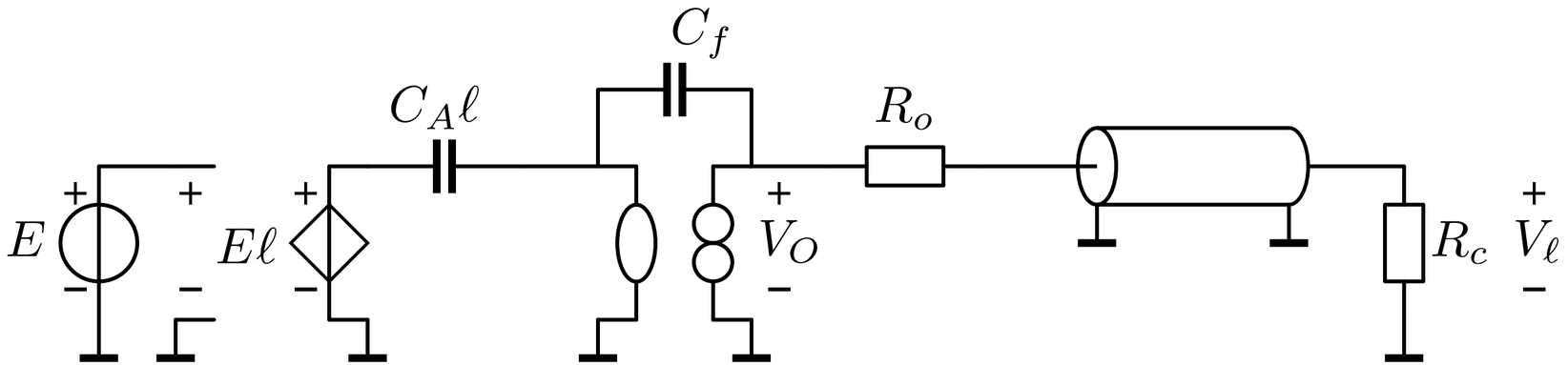

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Structured Electronic Design

EE4109
Design of the input stage
of the active antenna

Anton J.M. Montagne

Input stage

Influence feedback capacitance on the noise performance as if it is in parallel with the source.

Lowest 1/f corner frequency if:

$$C_{iss} = C_A\ell + C_f = C_A\ell\,(1+\ell)$$

SLiCAP_python: W=1200u, L=1.25u, ID=1.4m

Floor E-noise: 5.3nV/m/rt(Hz)

Corner 1/f noise: 34kHz

Floor noise can be reduced by increasing the current.

Other combinations of W, L and ID are also possible.

SLiCAP_python: CS_noise.py

LTspice: CSstageNoise.asc

Input stage SLiCAP

Input stage SLiCAP

CS_noise.py: input stage SLiCAP with antenna model

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Determination of L and ID from W, noise, and antenna specifications

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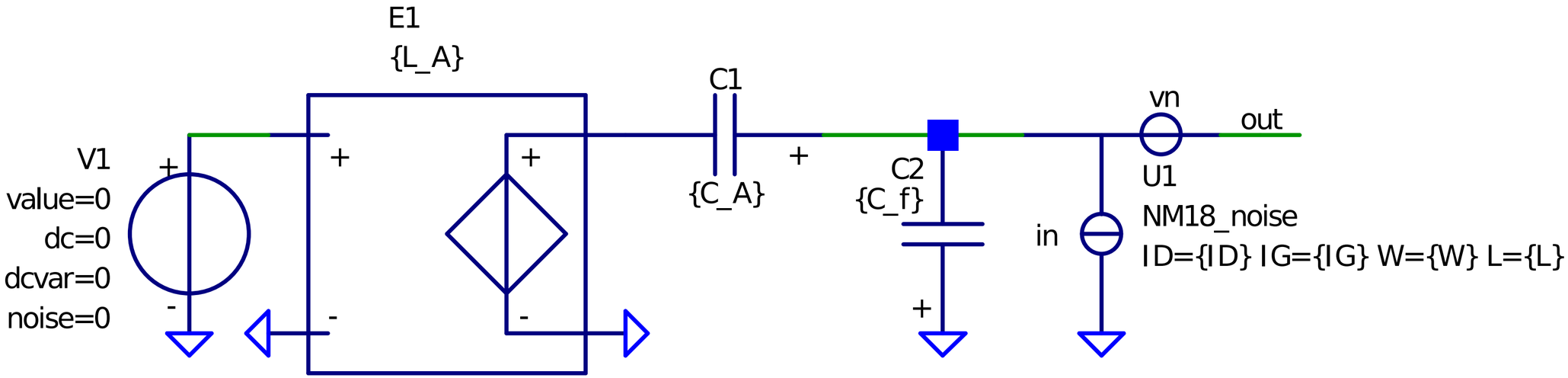

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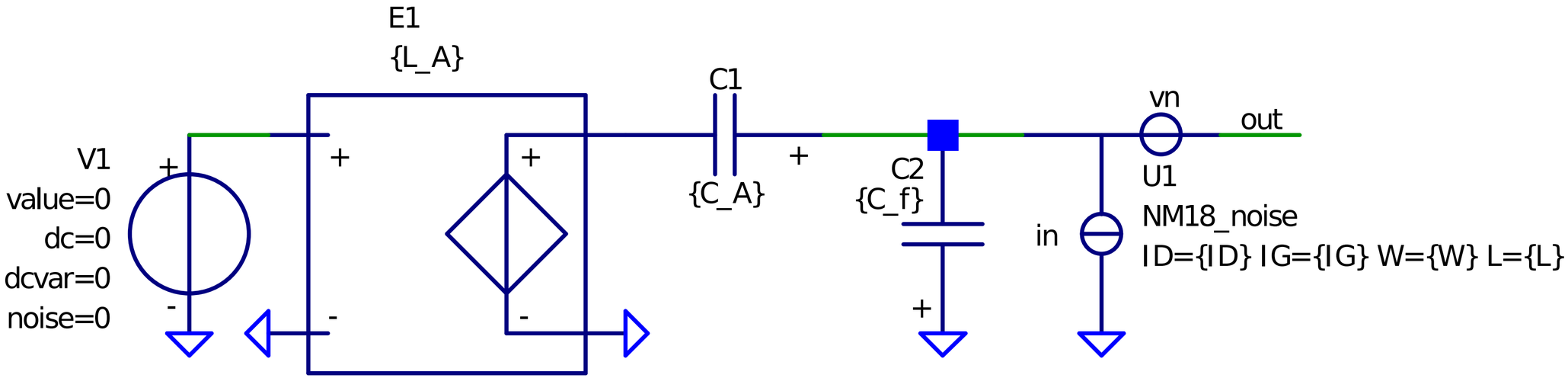

1 : W = 1.20e-3, L = 1.25e-6, ID = 1.39e-03, S_f = 2.81e-17, f_ell = 3.41e+4, Ciss = 1.03e-11, IC=2.27e+0.
2 : W = 9.00e-4, L = 1.71e-6, ID = 2.13e-03, S_f = 2.82e-17, f_ell = 3.34e+4, Ciss = 1.03e-11, IC=6.31e+0.
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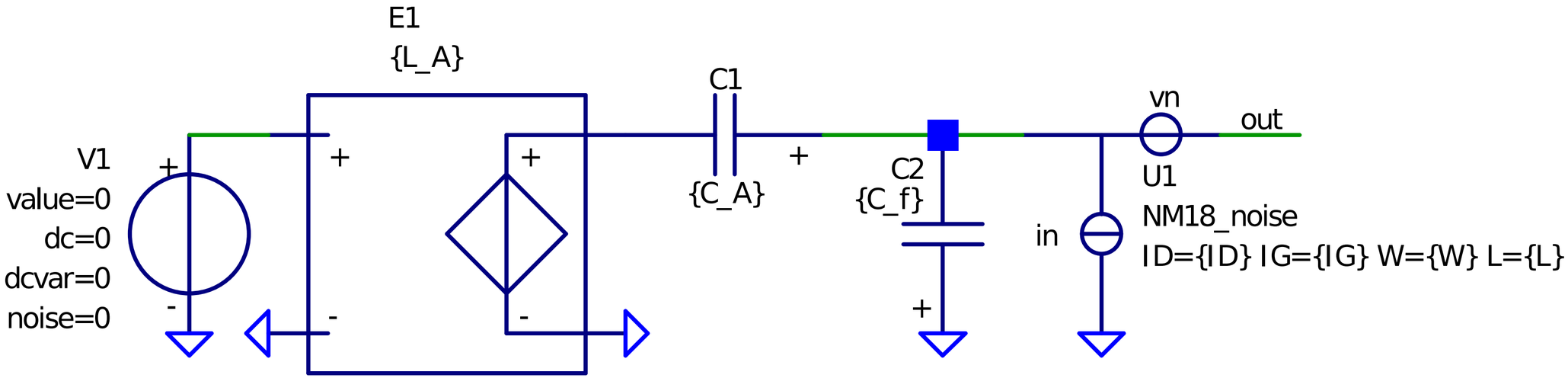

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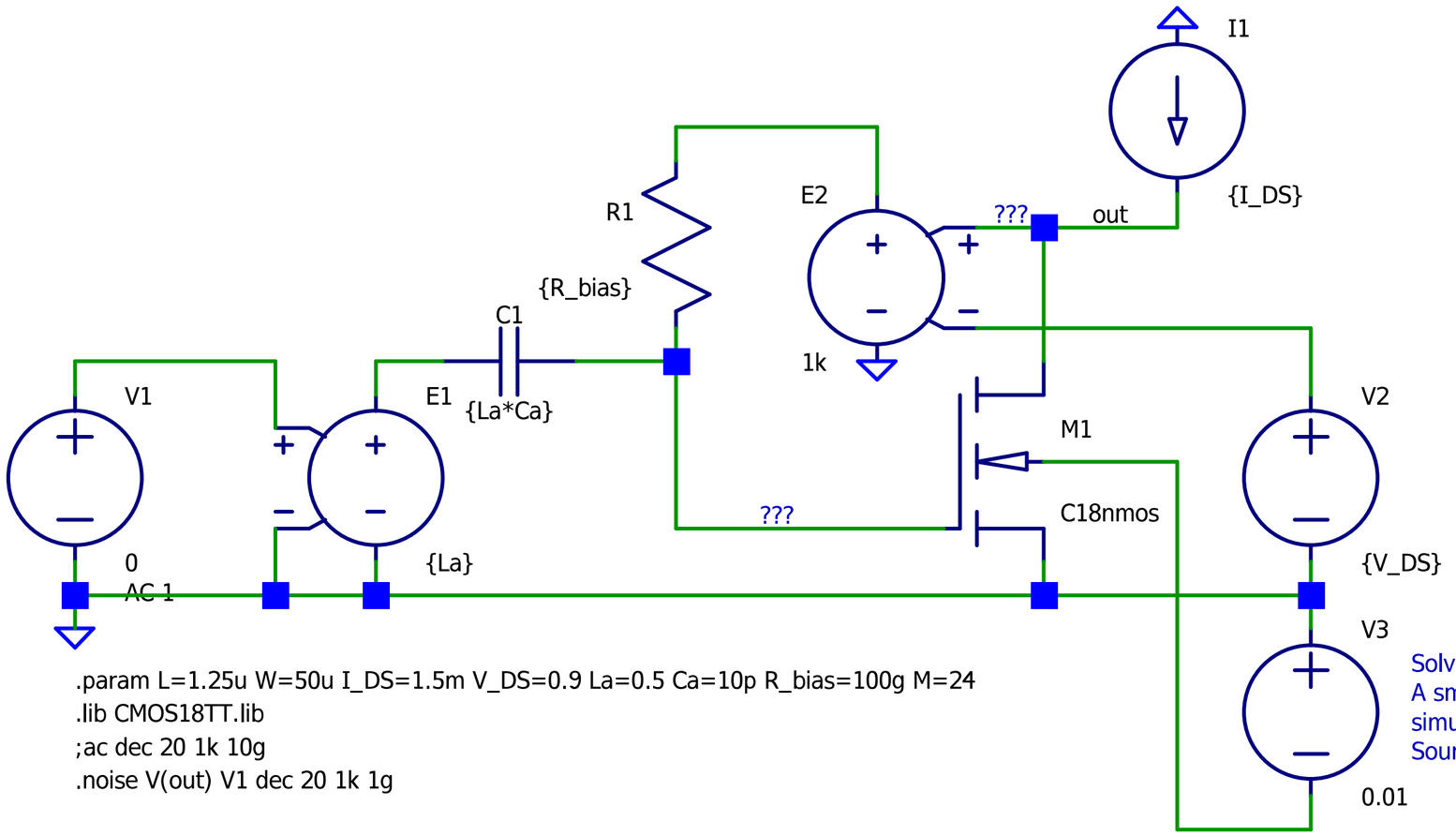

.param L=1.25u W=50u I_DS=1.5m V_DS=0.9 La=0.5 Ca=10p R_bias=100g M=24
.lib CMOS18TT.lib
;ac dec 20 1k 10g
.noise V(out) V1 dec 20 1k 1g

Solve issue:
A small negative bias on the bulk for correct simulation of the small-signal behavior.
Source and drain regions not completely defined!

Structured Electronic Design

EE4109
Design of the output stage
of the active antenna

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Output stage

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Influence feedback capacitance on the noise performance as if it is in parallel with the load.

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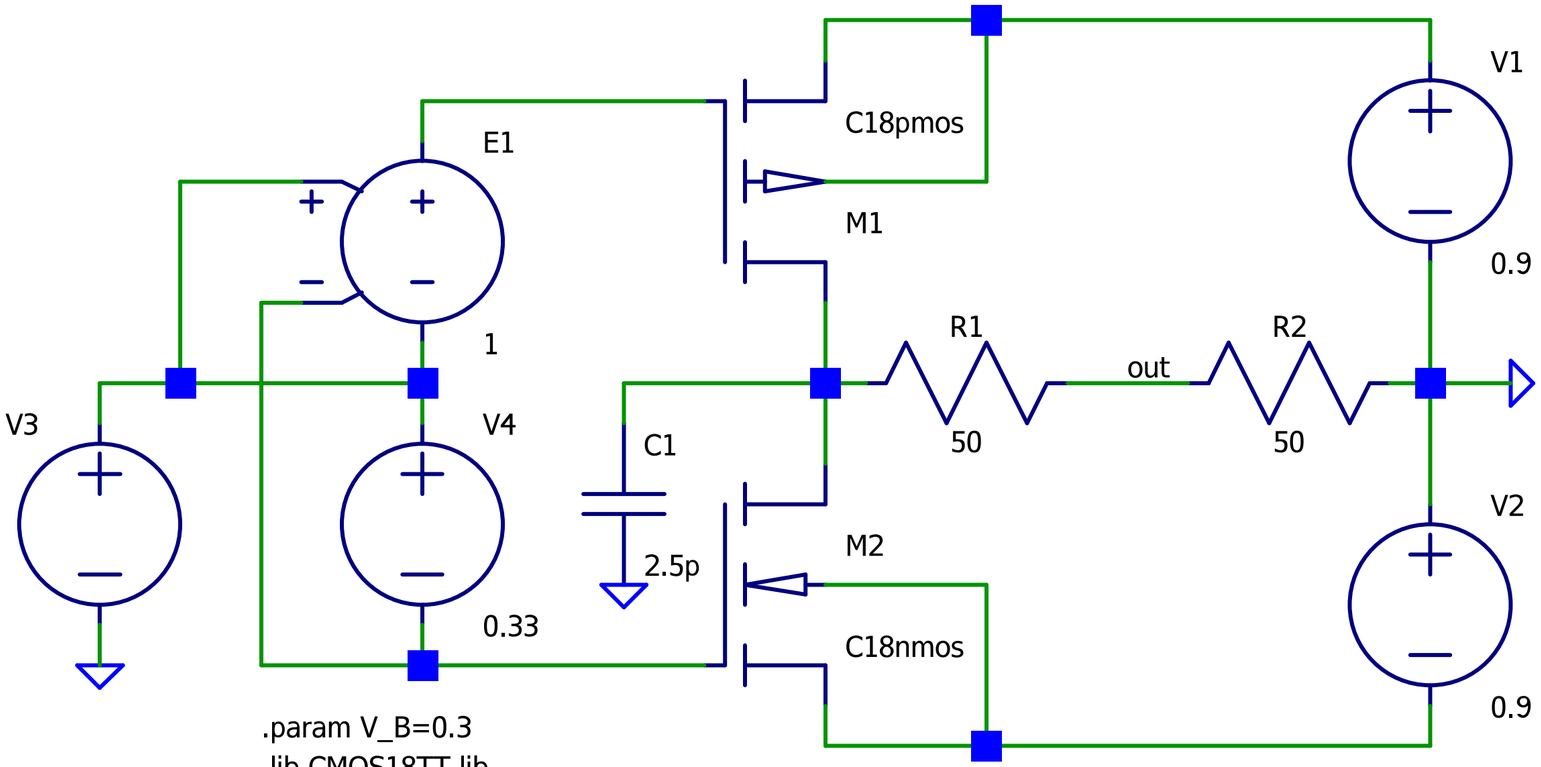


```
.param V_B=0.3
.lib CMOS18TT.lib
;dc V3 -0.5 0.5 0.01
.step param V_B 0 0.5 0.05
.meas DC Ibias FIND (I(V1)+I(V2))/2 AT 0
.tran 0 50n 0 100p
```

Structured Electronic Design

EE4109
Design the active antenna
with a dual-stage controller

Anton J.M. Montagne

Dual stage amplifier

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Two cascaded CS stages yield a noninverting controller

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  - CD or complementary parallel CD
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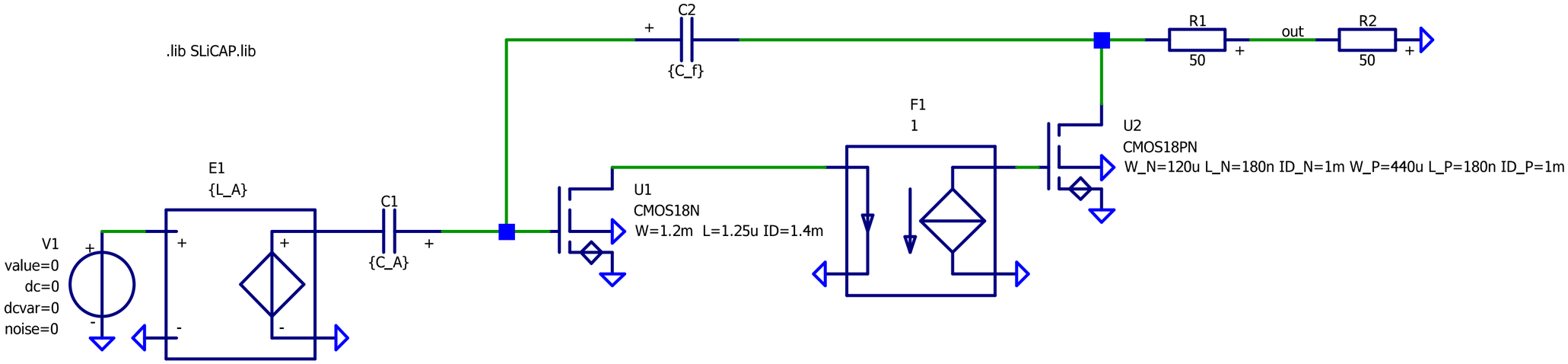

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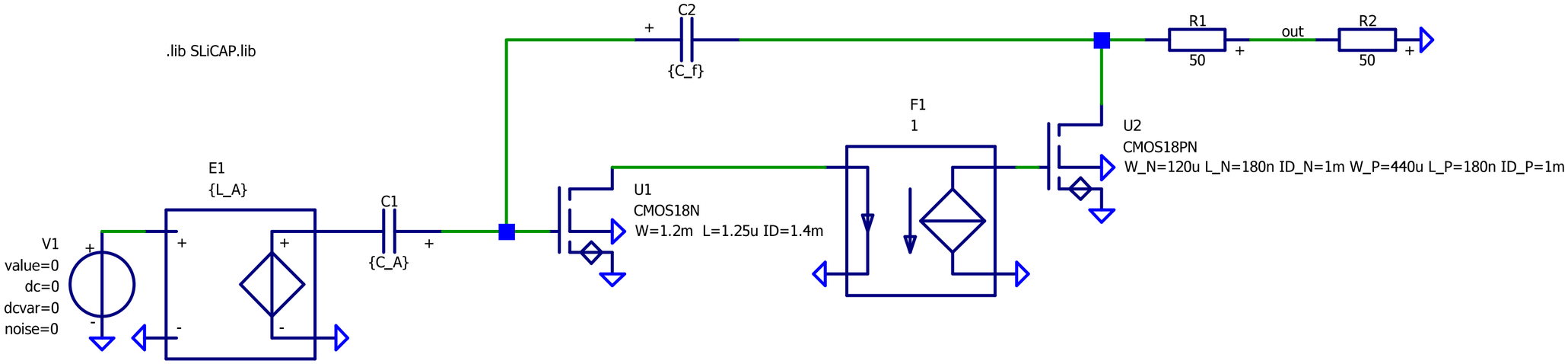

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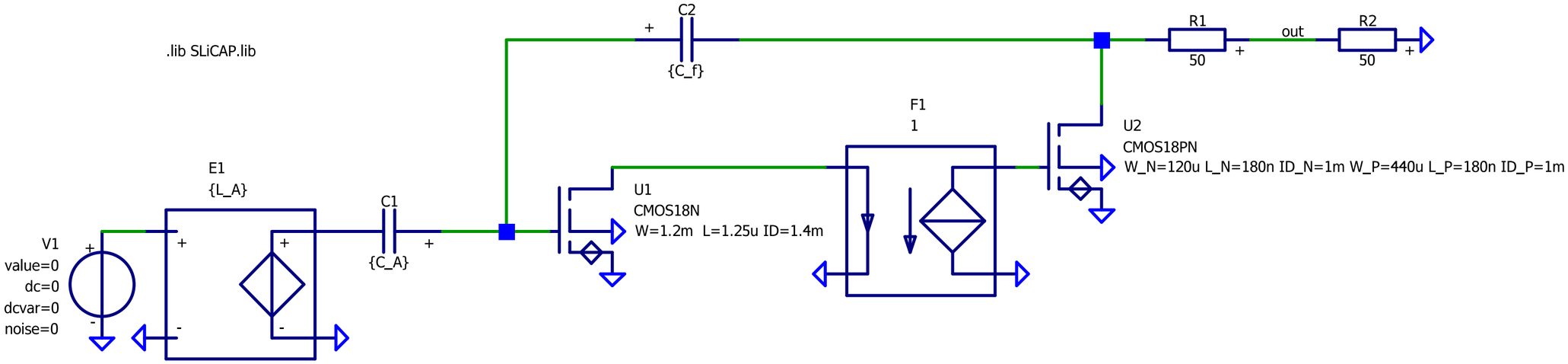

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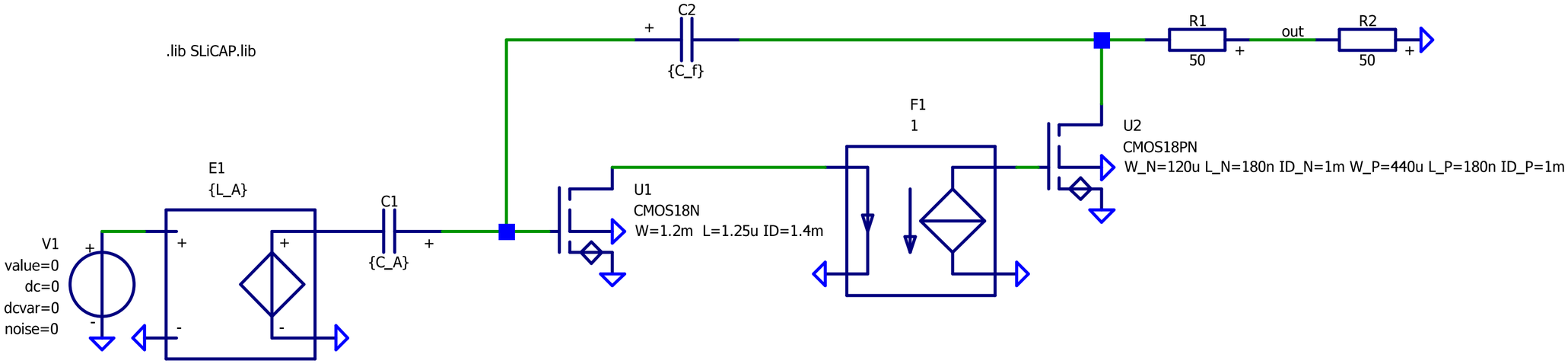

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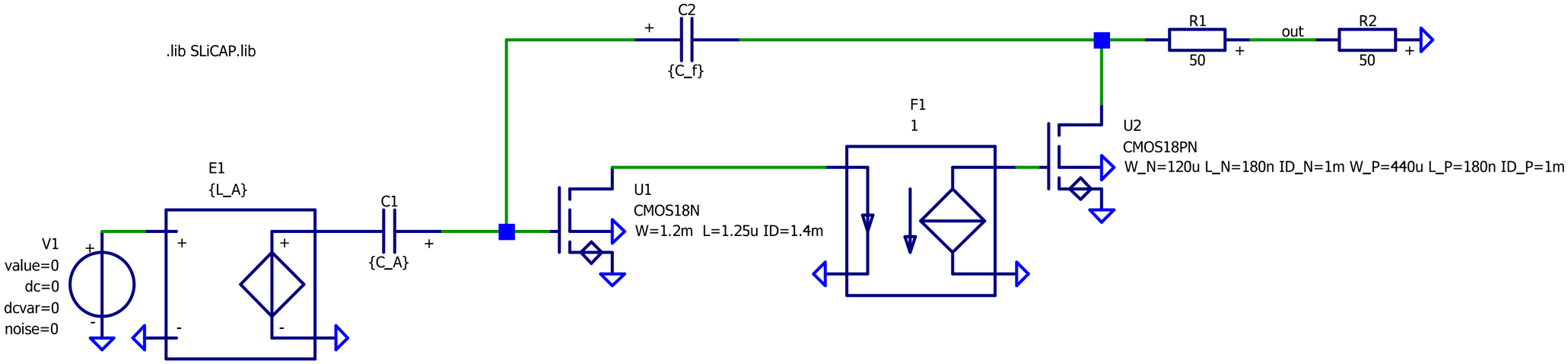

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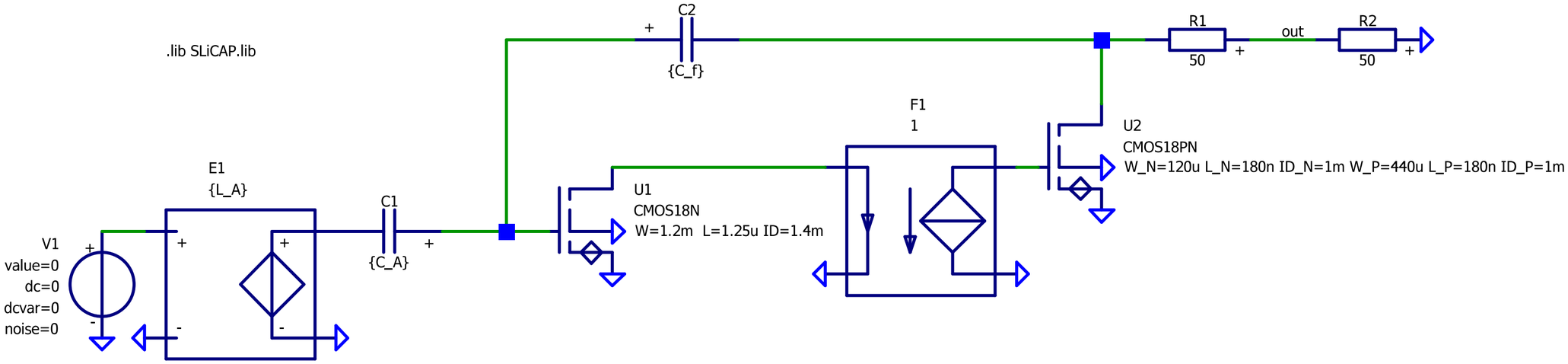

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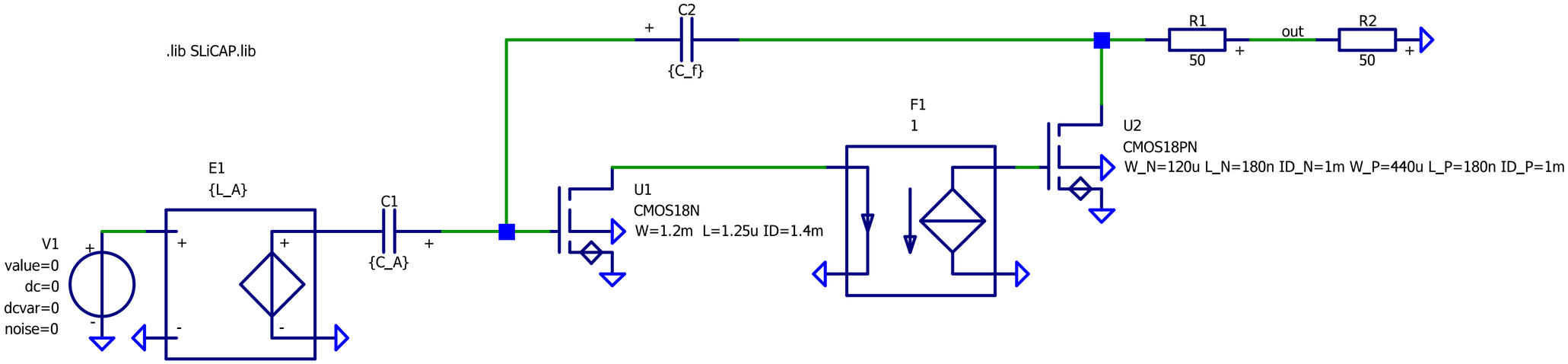

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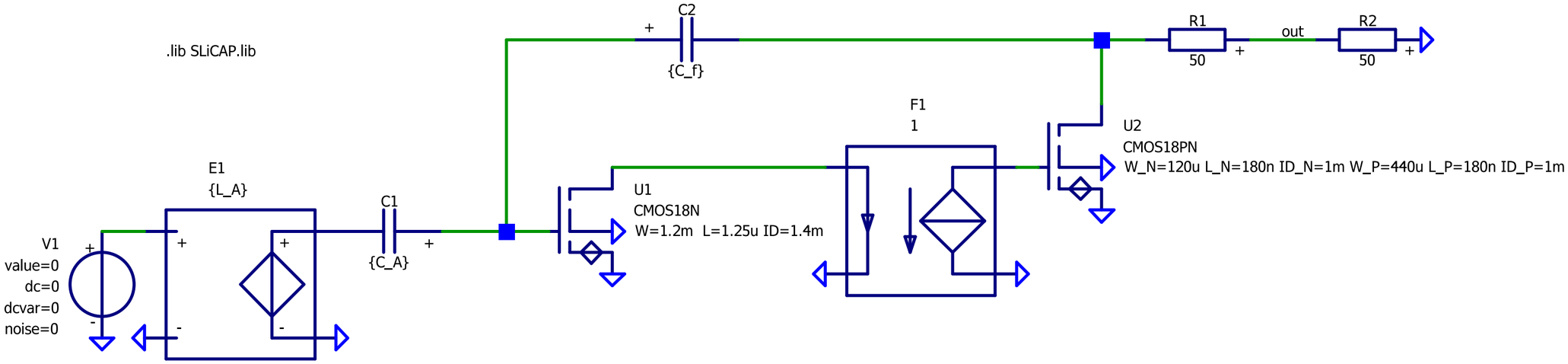

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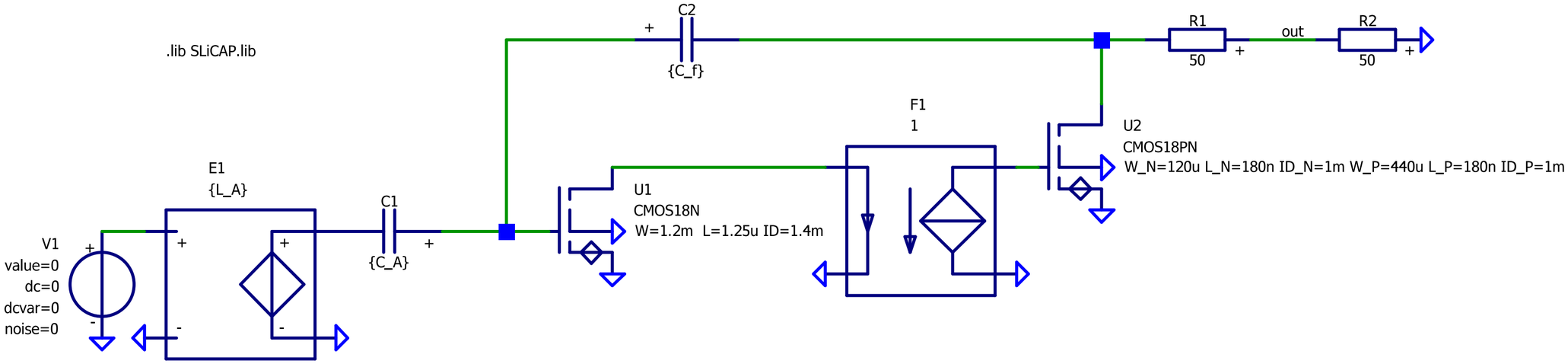

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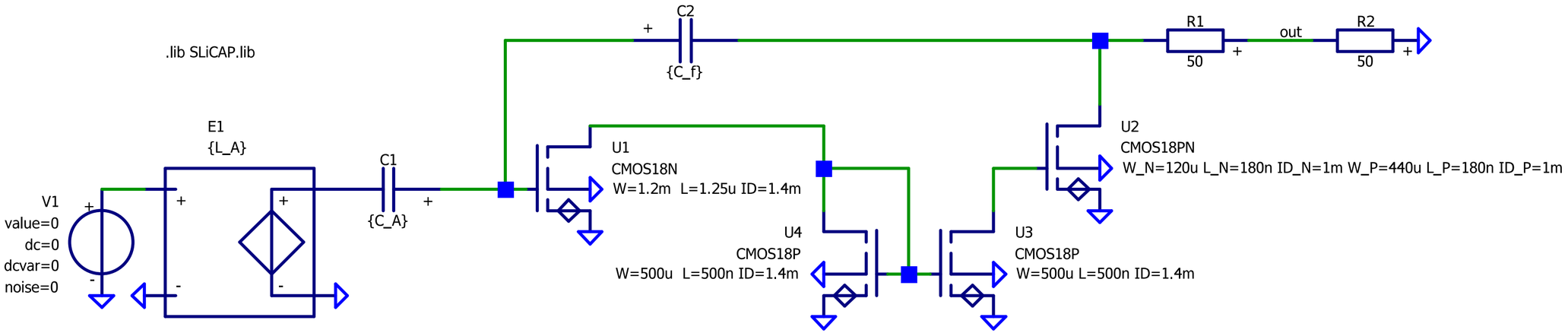

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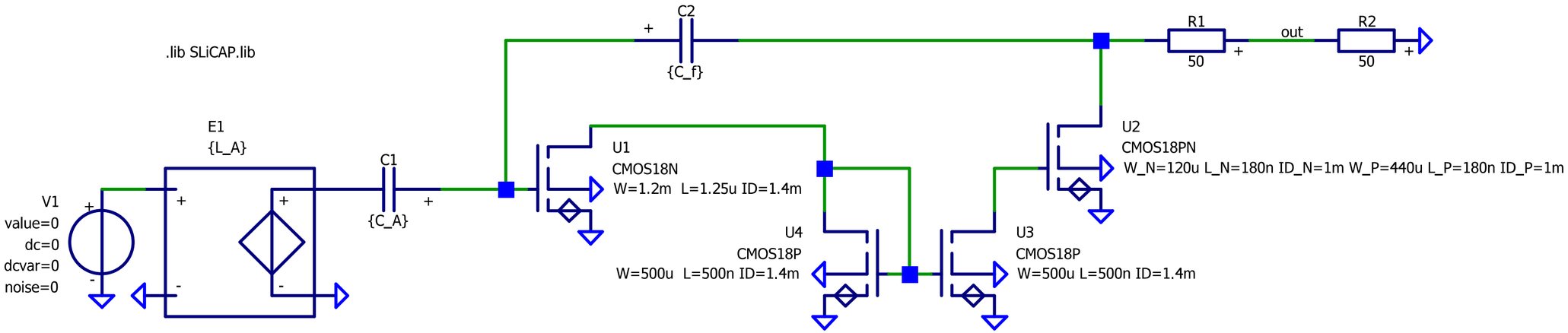

SLiCAP: DualStageMirror.py:

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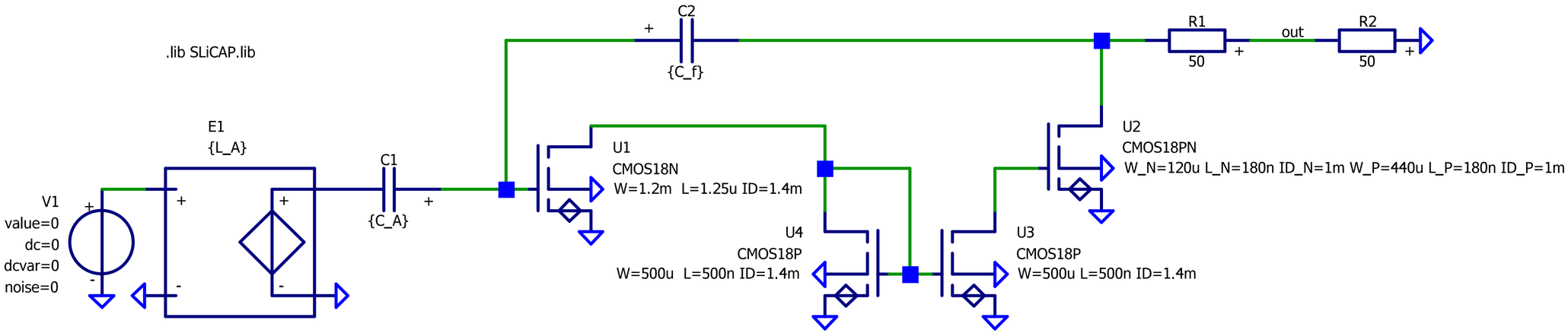

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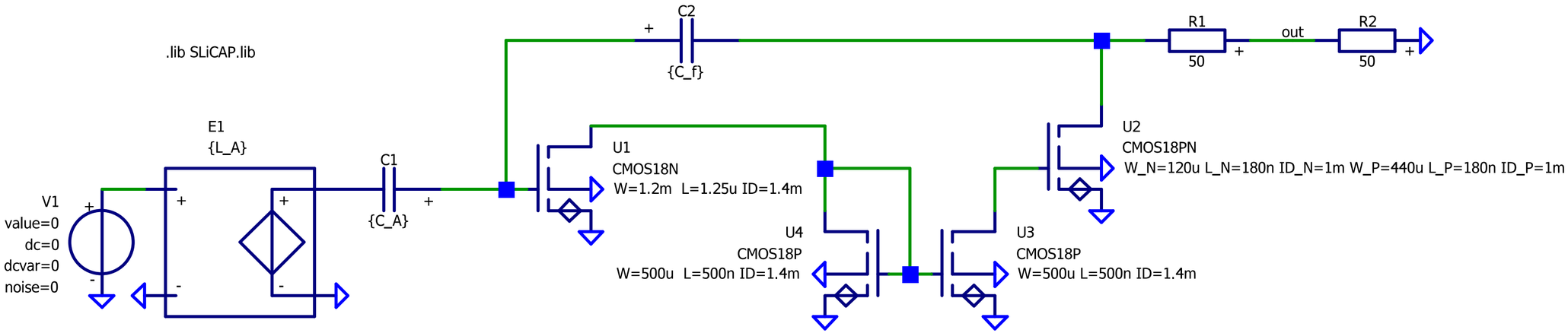

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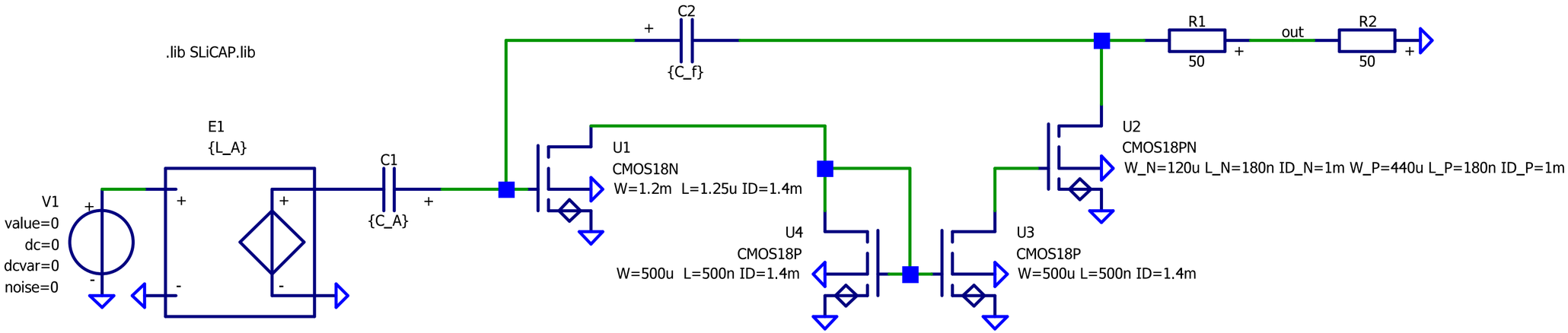

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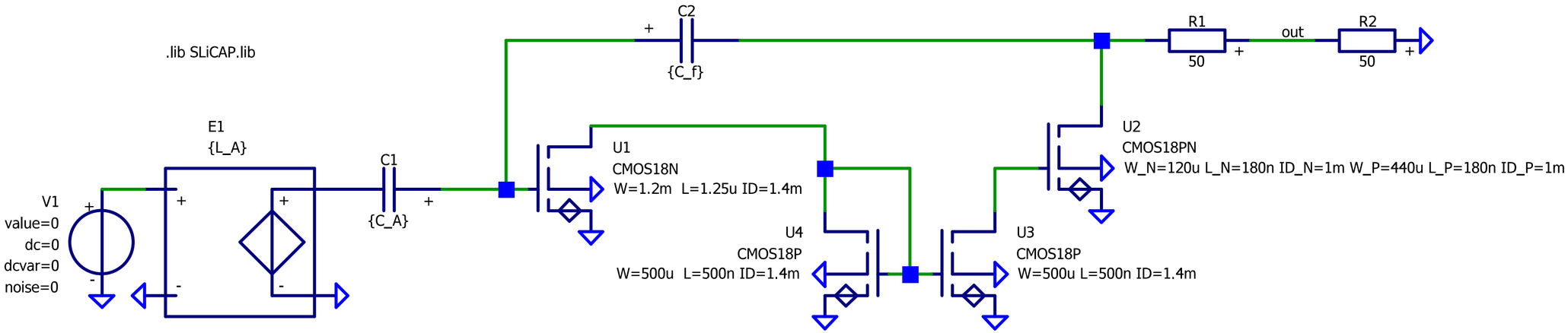

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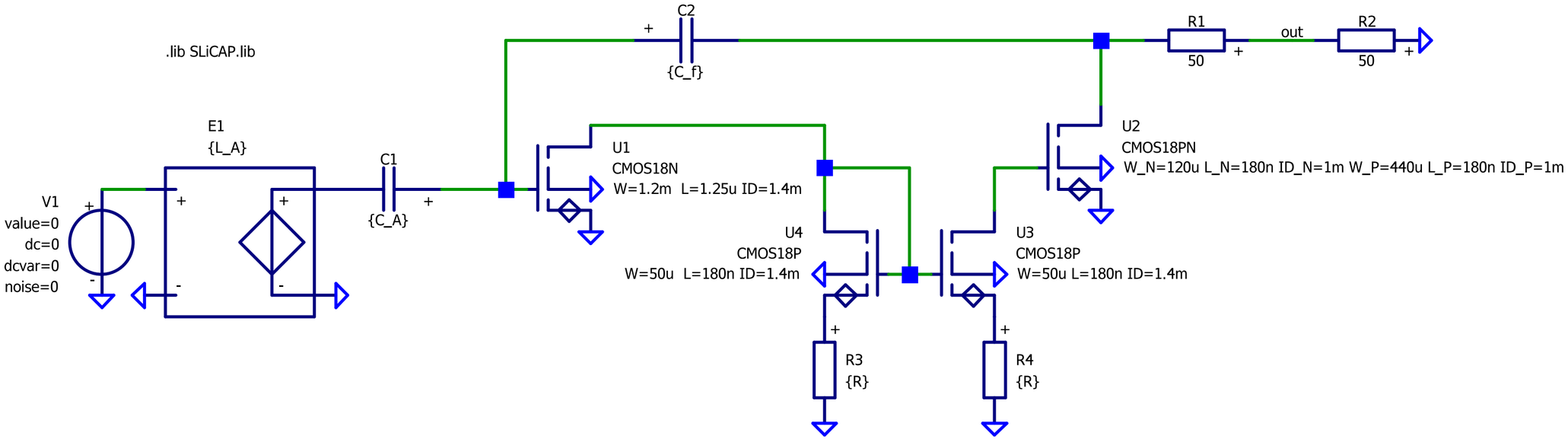

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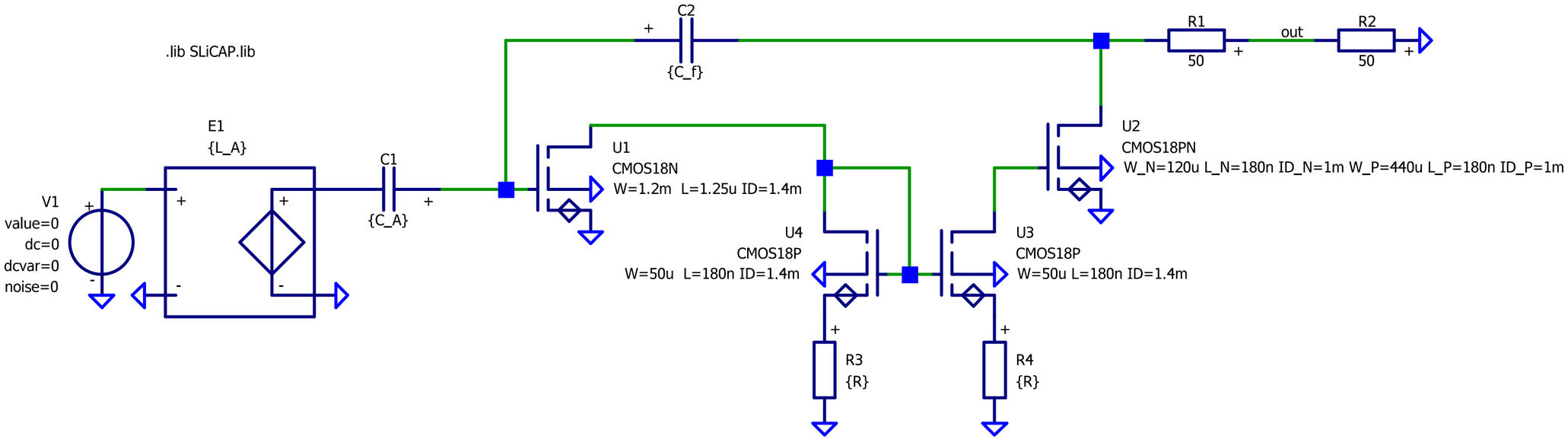

SLiCAP: DualStageMirrorRes.py:

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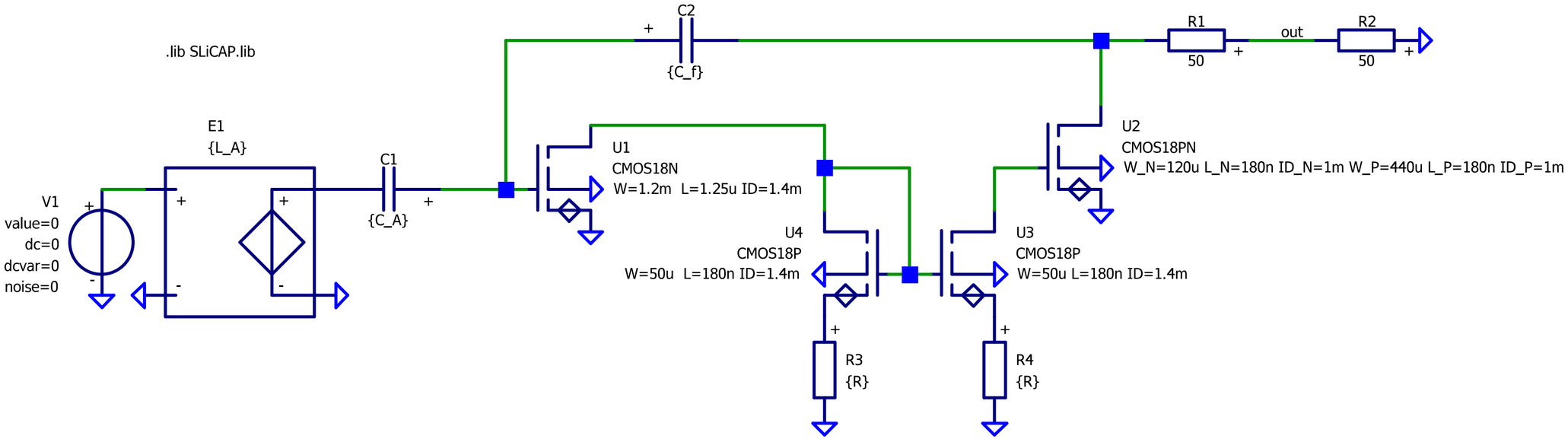

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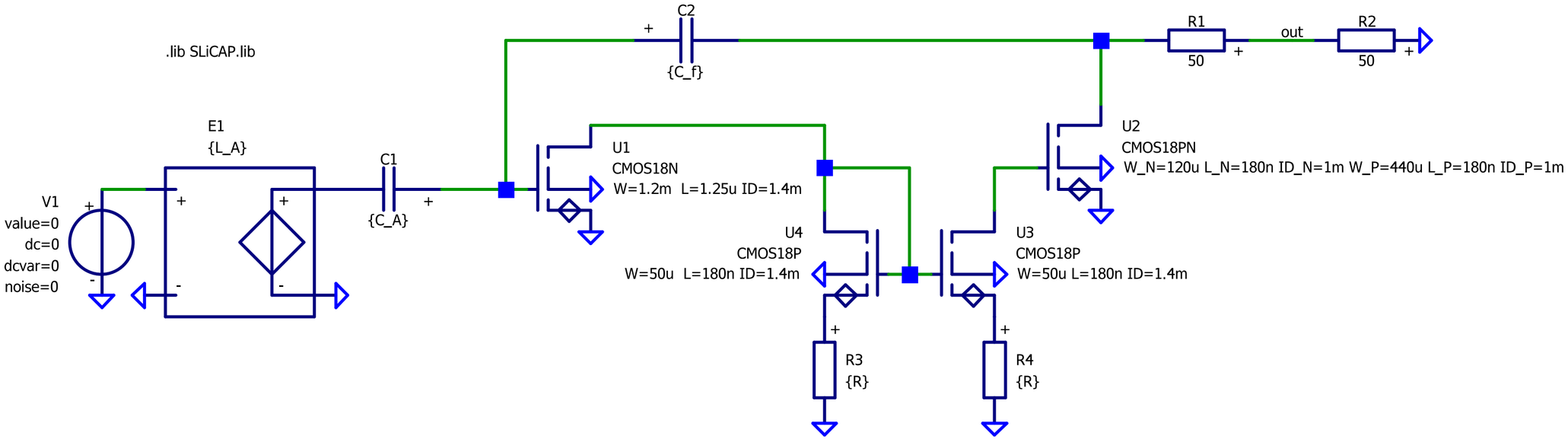

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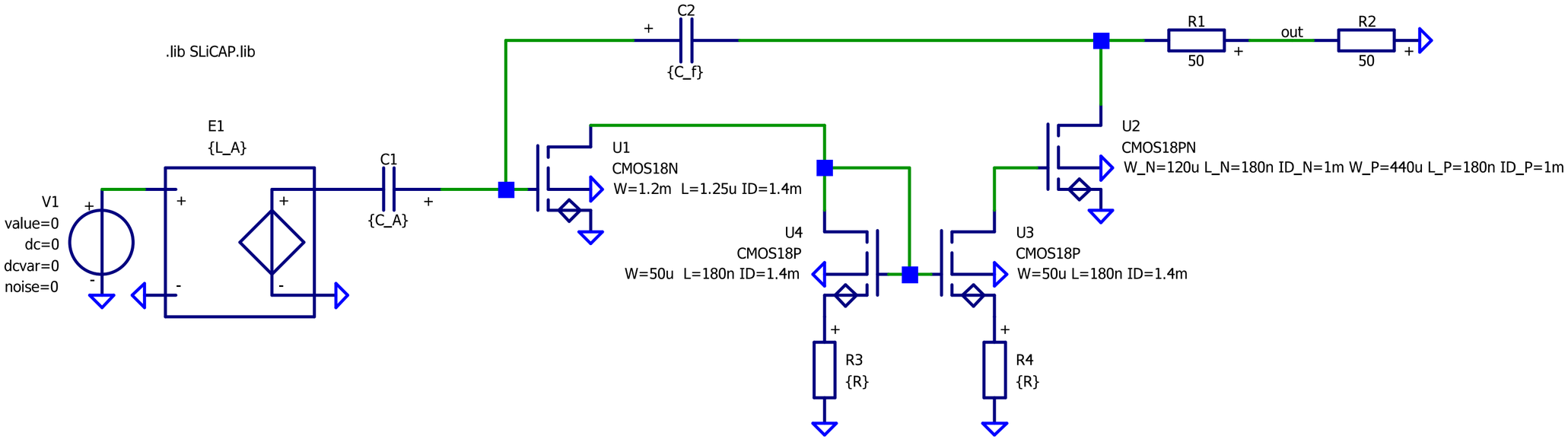

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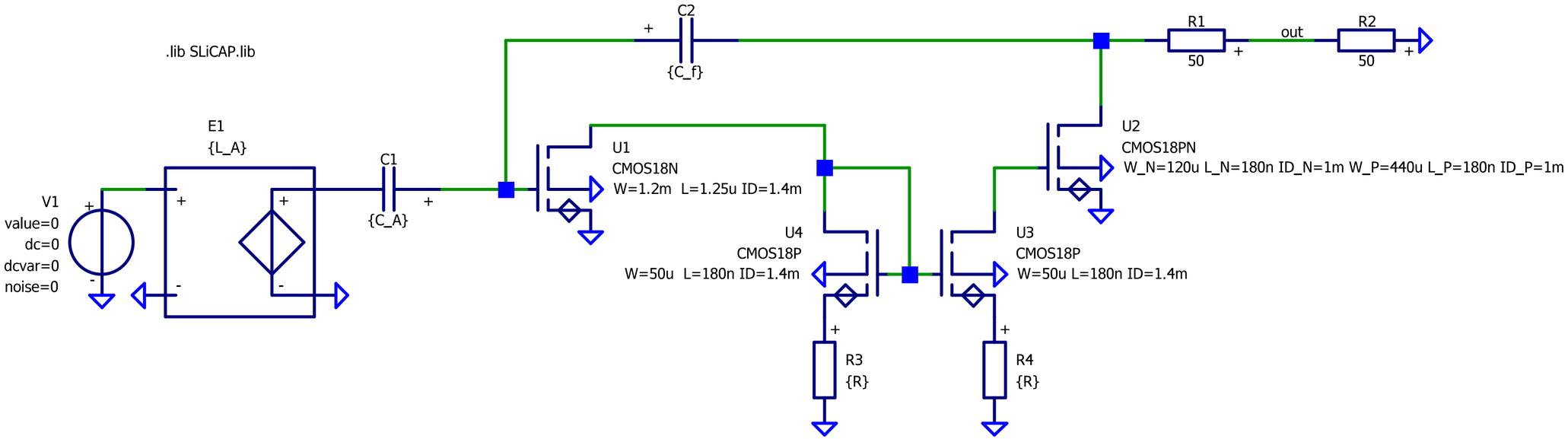

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