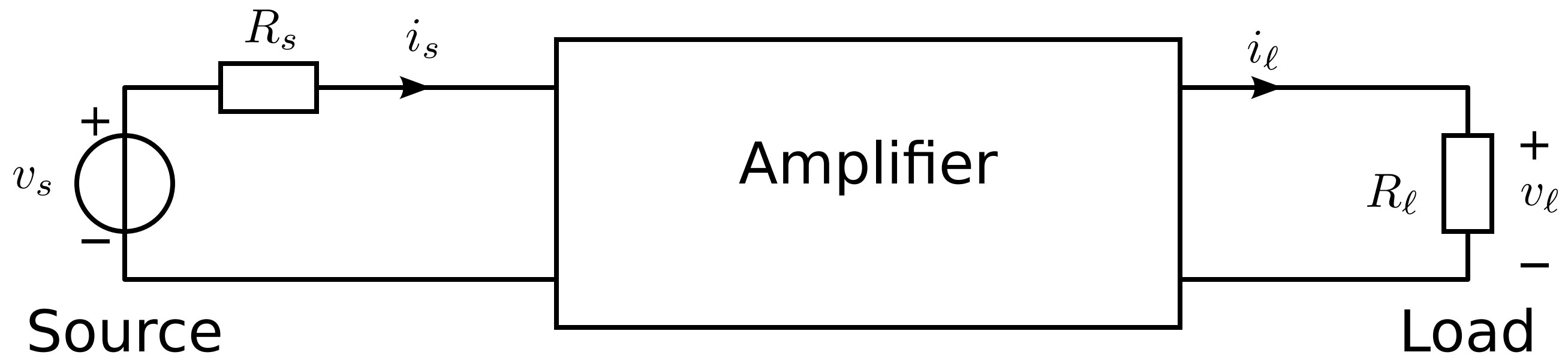


Structured Electronic Design

Principle of amplification
and
a formal approach to biasing

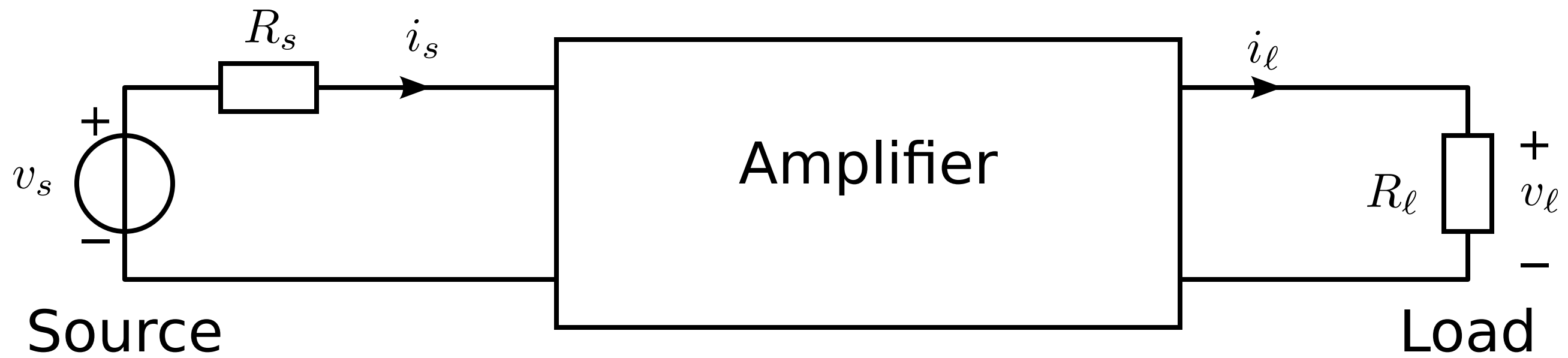
Anton J.M. Montagne

Amplification and biasing



Amplification and biasing

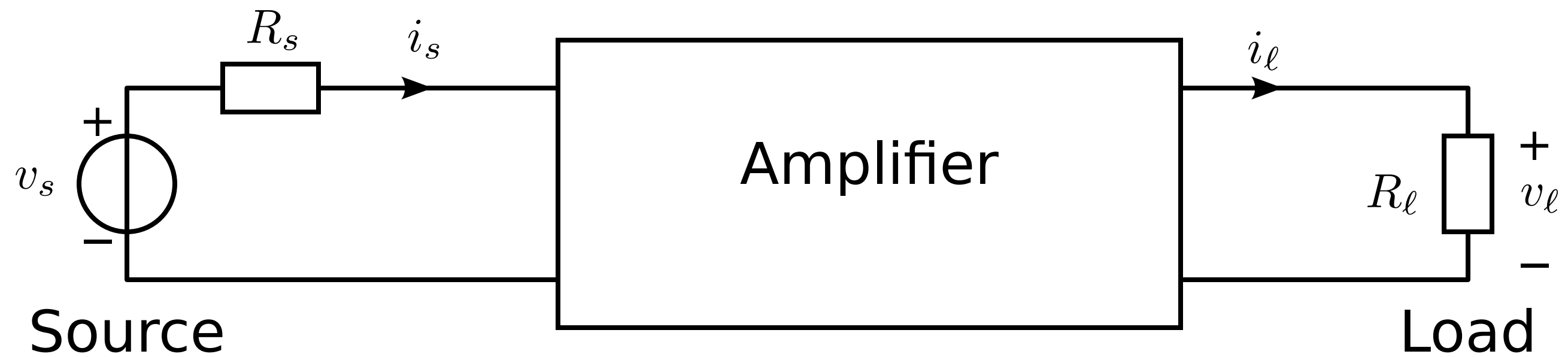
Signal values at the load should have a unique correspondence with those of the source



Amplification and biasing

Signal values at the load should have a unique correspondence with those of the source

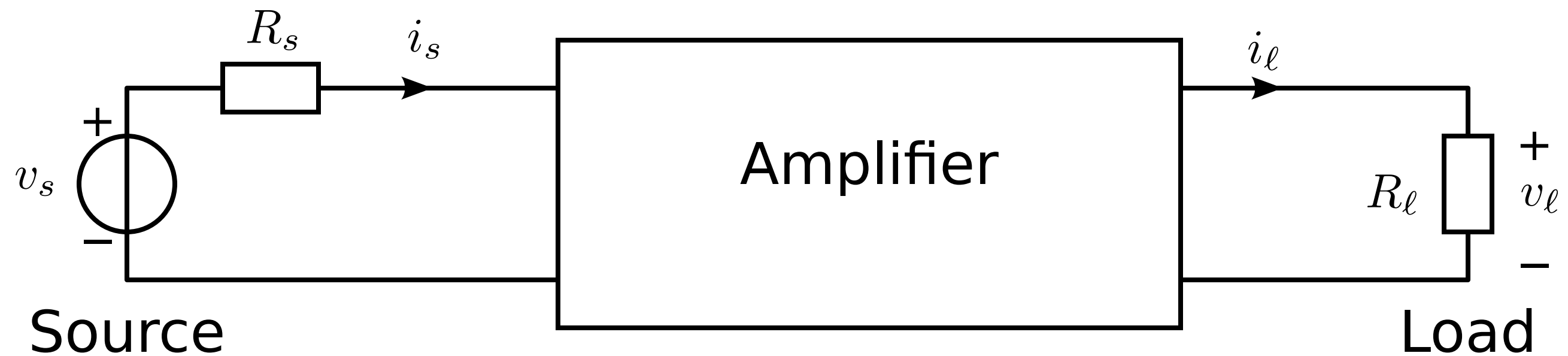
The available power at the output of the amplifier should exceed that of the source



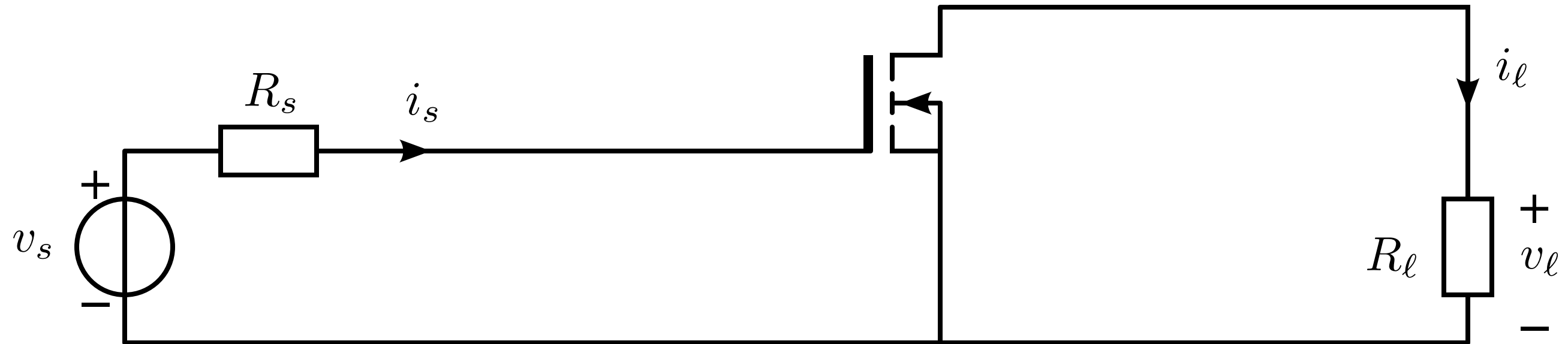
Amplification and biasing

Signal values at the load should have a unique correspondence with those of the source

The available power at the output of the amplifier should exceed that of the source

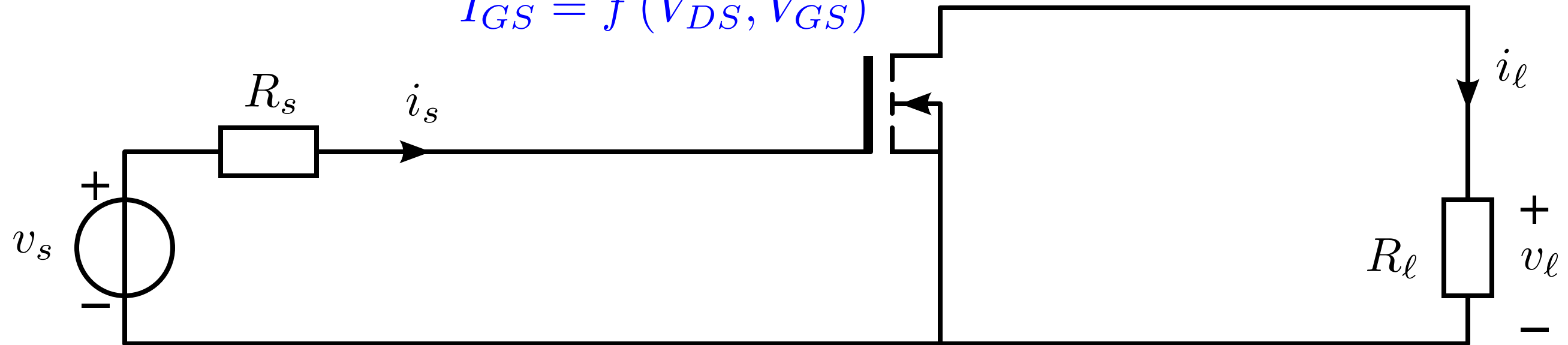


Amplification and biasing



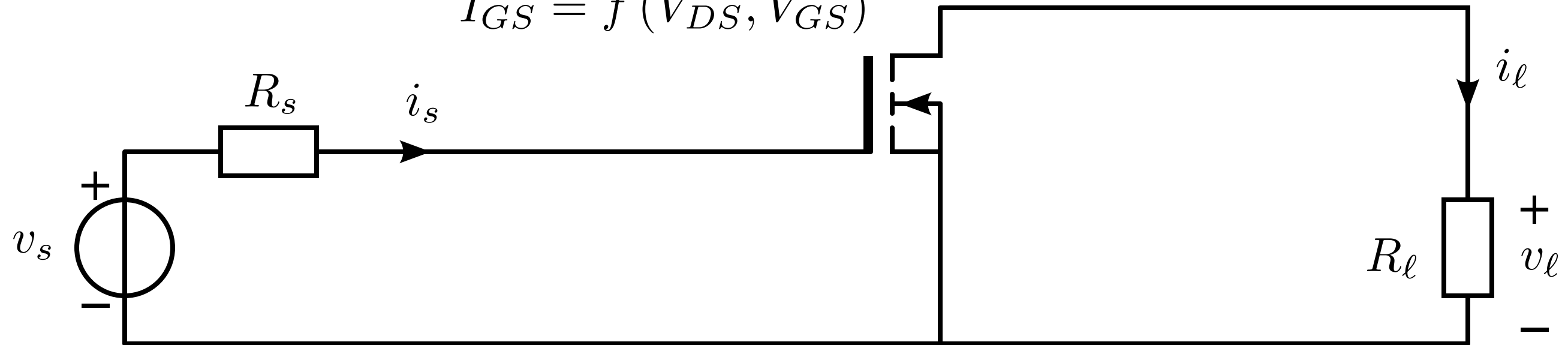
Amplification and biasing

Device equations: $I_{DS} = f(V_{DS}, V_{GS})$
 $I_{GS} = f(V_{DS}, V_{GS})$



Amplification and biasing

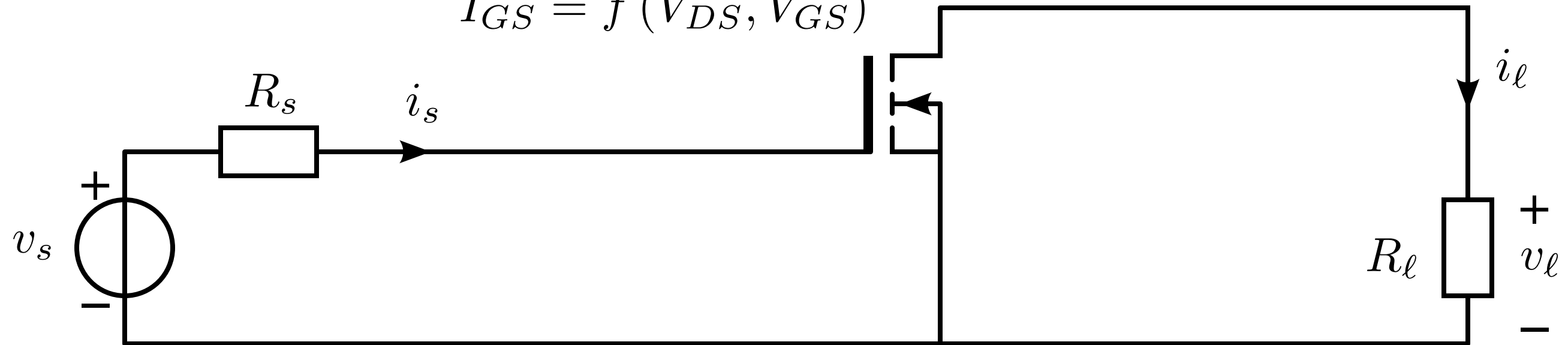
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Only drain current if:

Amplification and biasing

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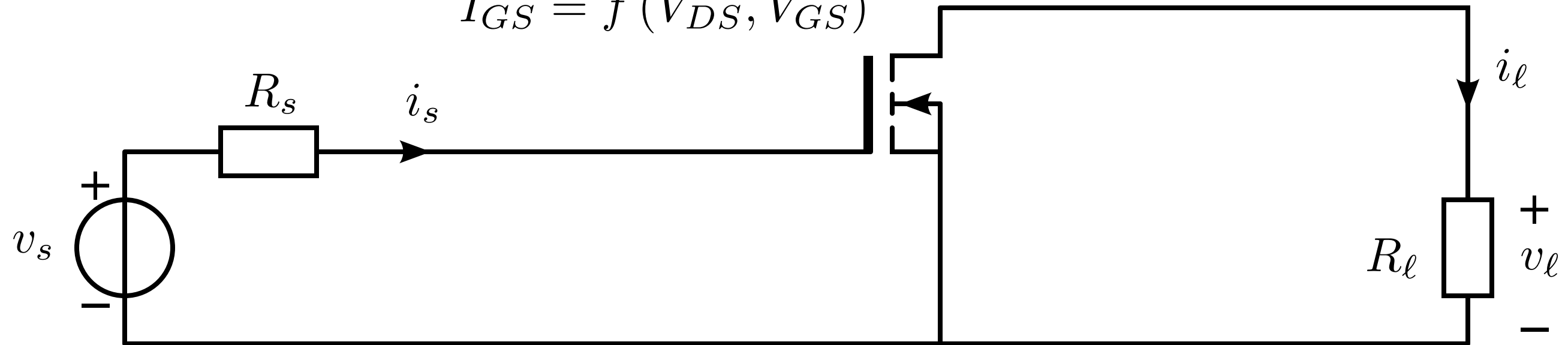


Only drain current if:

nonzero drain-source voltage

Amplification and biasing

Device equations: $I_{DS} = f(V_{DS}, V_{GS})$
 $I_{GS} = f(V_{DS}, V_{GS})$



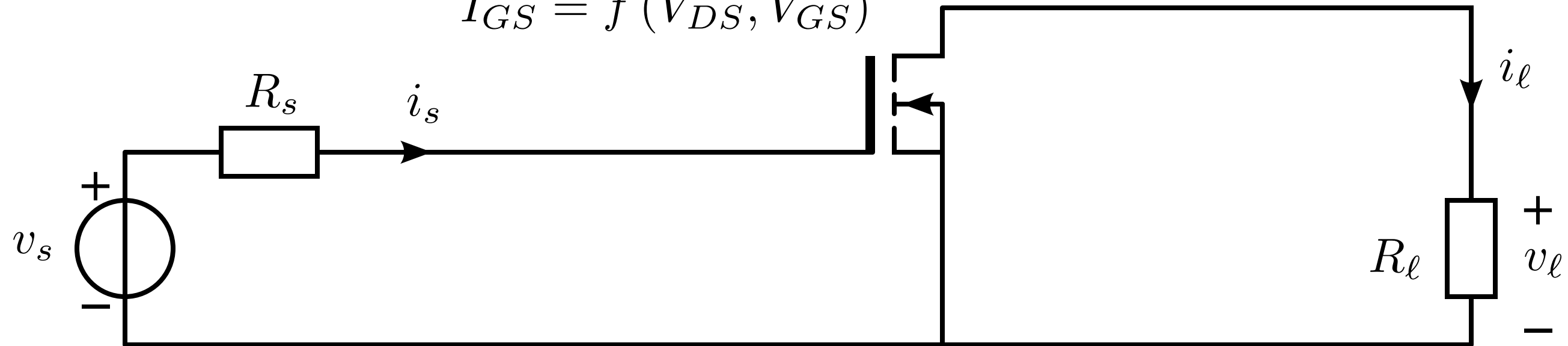
Only drain current if:

nonzero drain-source voltage

gate-source voltage exceeds the threshold voltage

Amplification and biasing

Device equations: $I_{DS} = f(V_{DS}, V_{GS})$
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Only drain current if:

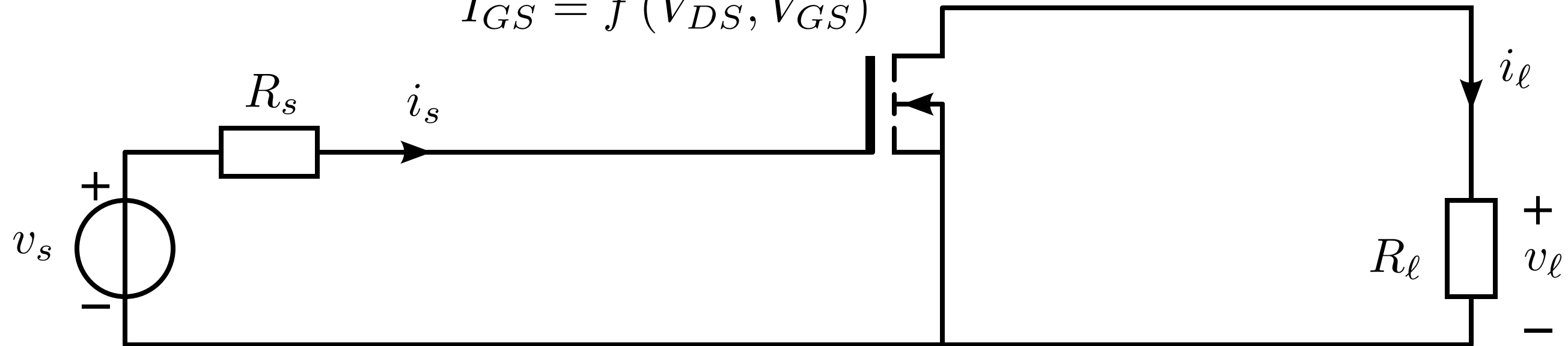
nonzero drain-source voltage

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Zero-signal operating point:

Amplification and biasing

Device equations: $I_{DS} = f(V_{DS}, V_{GS})$
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Only drain current if:

nonzero drain-source voltage

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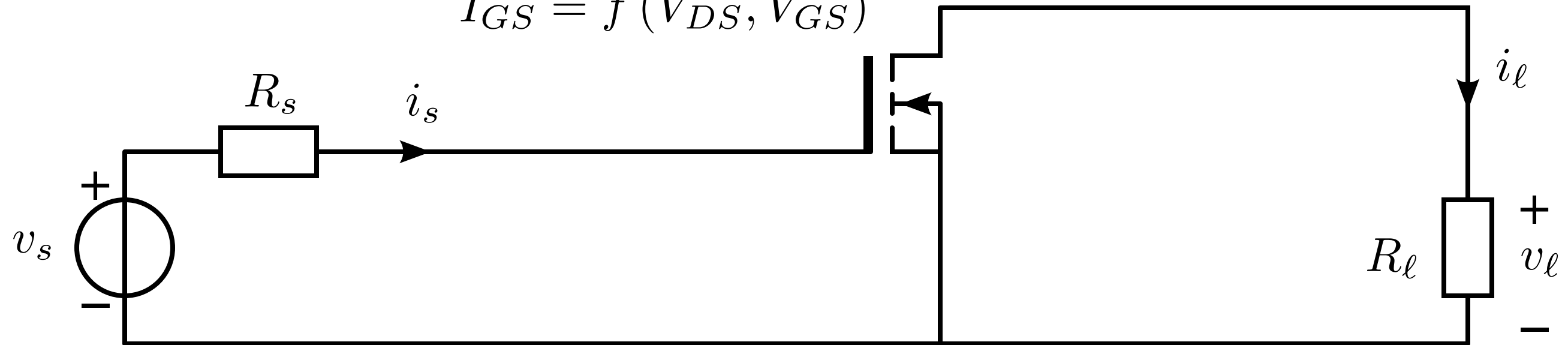
Zero-signal operating point:

$$V_{GS} = 0 \quad V_{DS} = 0$$

$$I_{GS} = 0 \quad I_{DS} = 0$$

Amplification and biasing

Device equations: $I_{DS} = f(V_{DS}, V_{GS})$
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Only drain current if:

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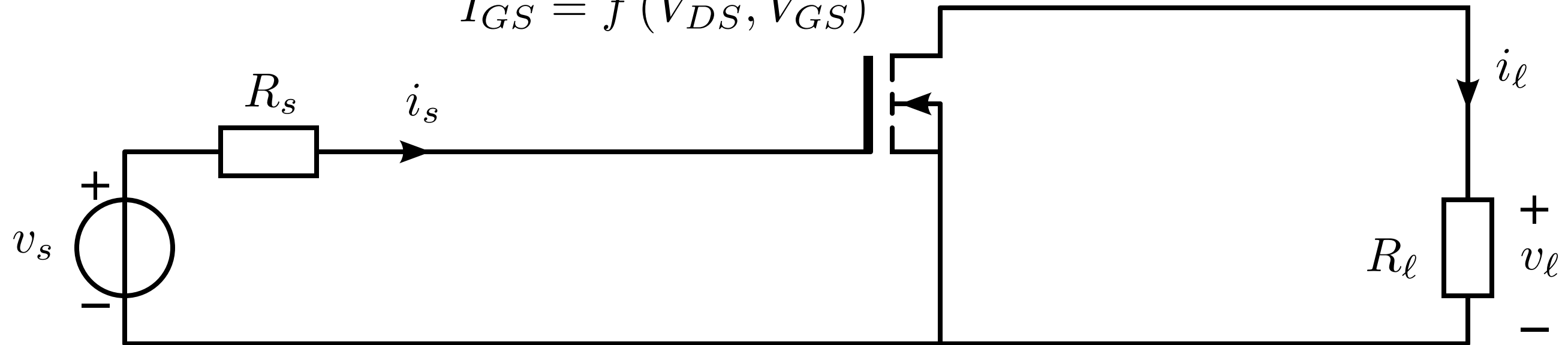
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No load signal

Amplification and biasing

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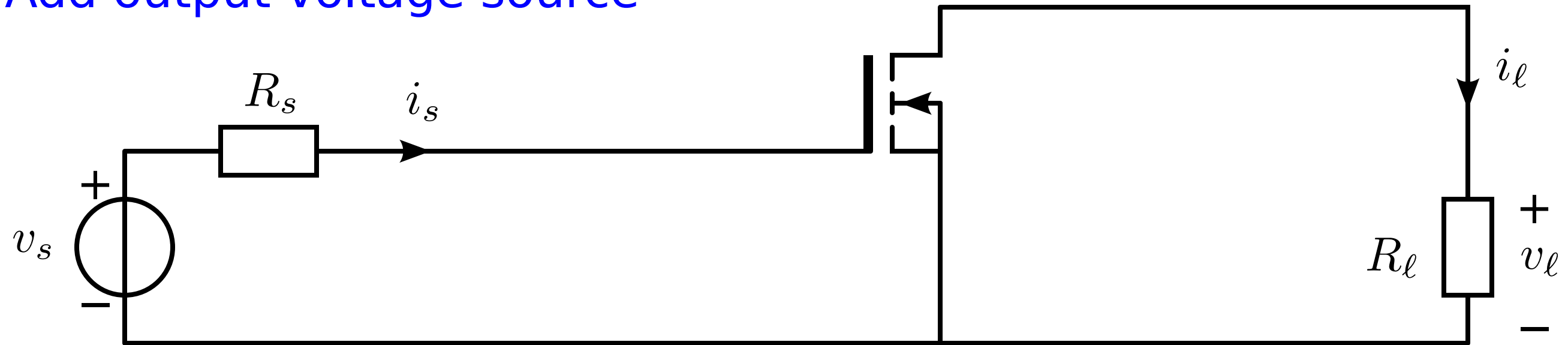
$$V_{GS} = 0 \quad V_{DS} = 0$$

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No load signal

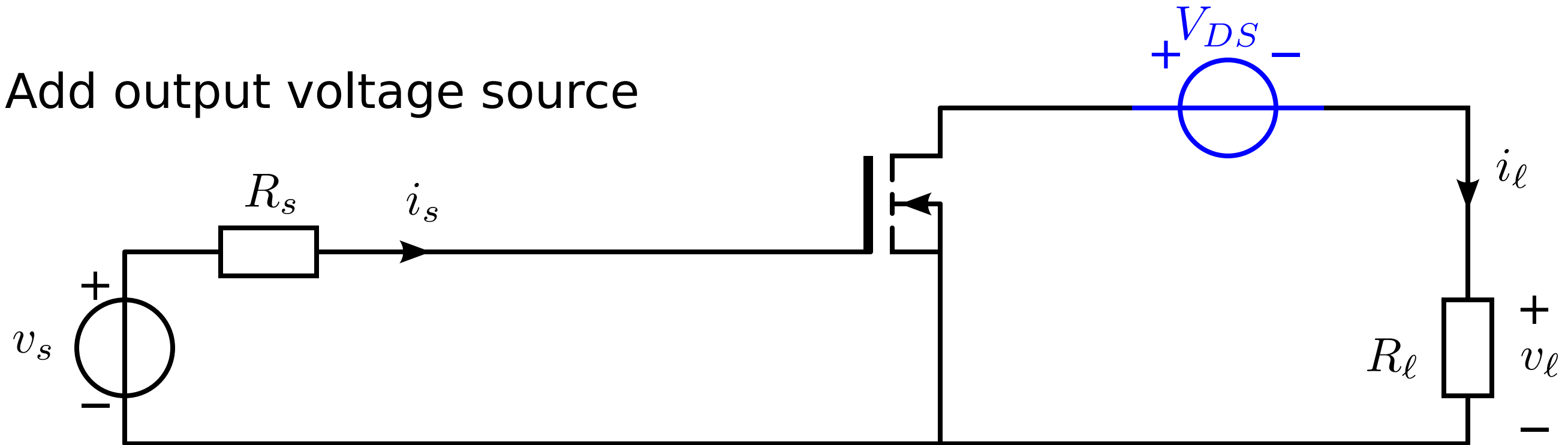
Amplification and biasing

Add output voltage source



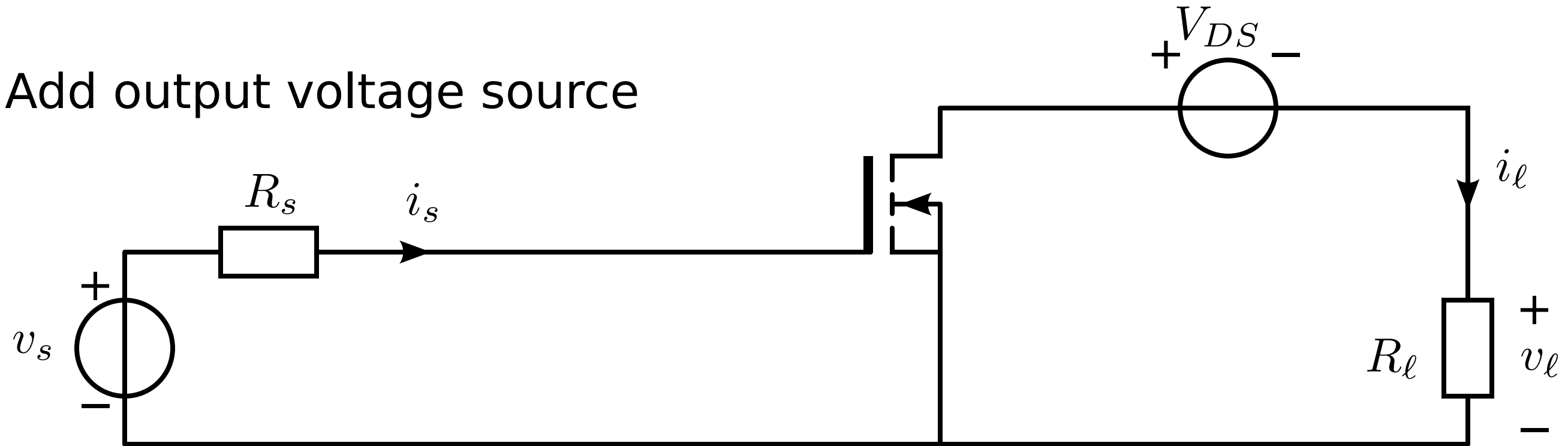
Amplification and biasing

Add output voltage source



Amplification and biasing

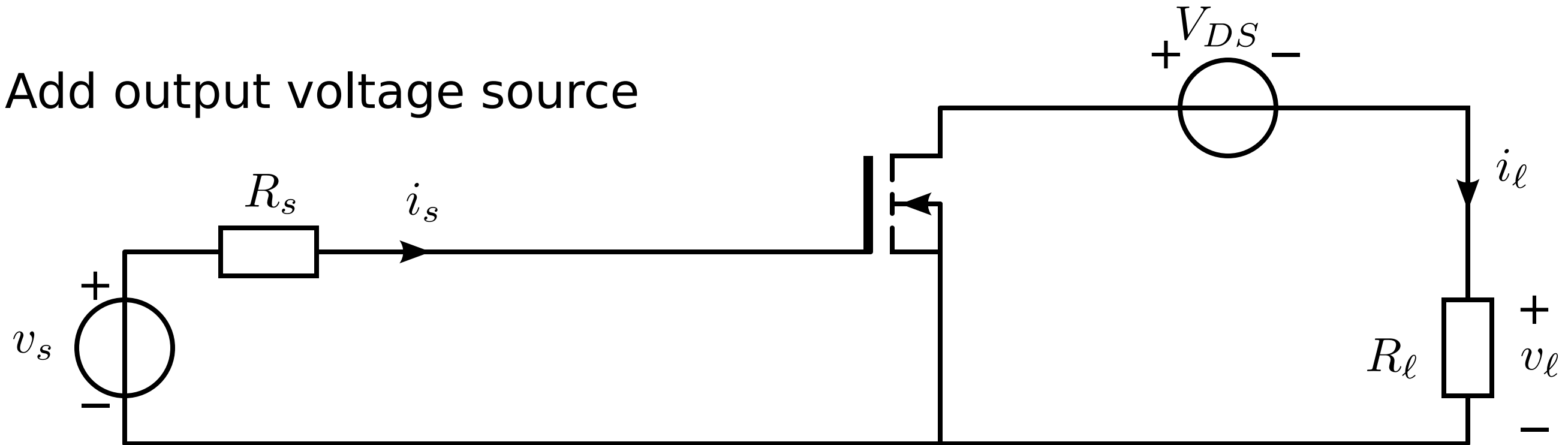
Add output voltage source



Load signal if the source voltage exceeds the threshold voltage

Amplification and biasing

Add output voltage source

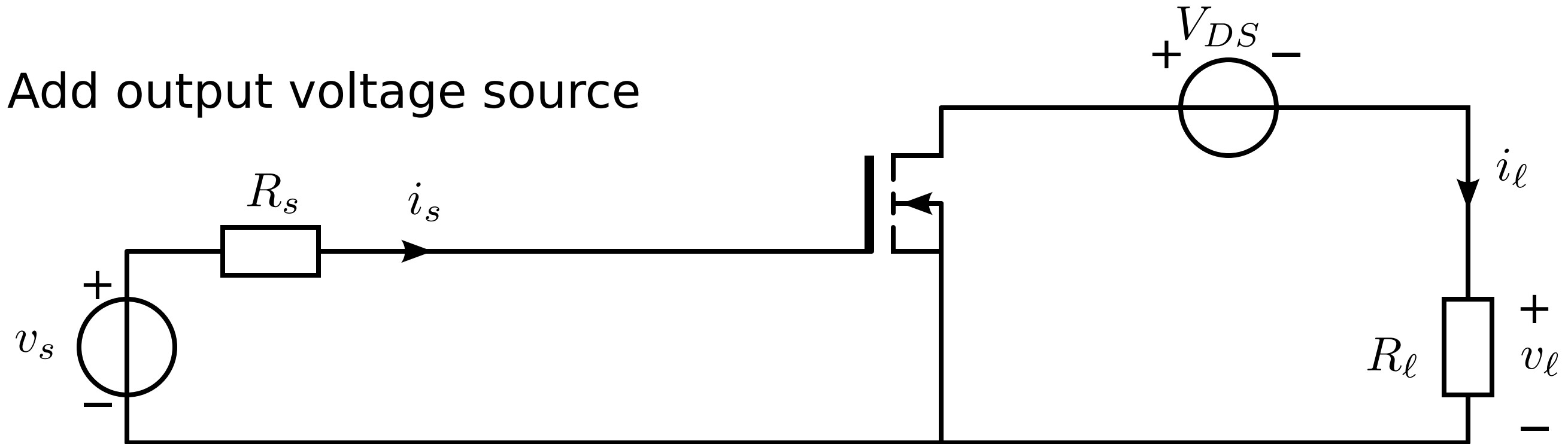


Load signal if the source voltage exceeds the threshold voltage

No unique correspondence between source and load signal values

Amplification and biasing

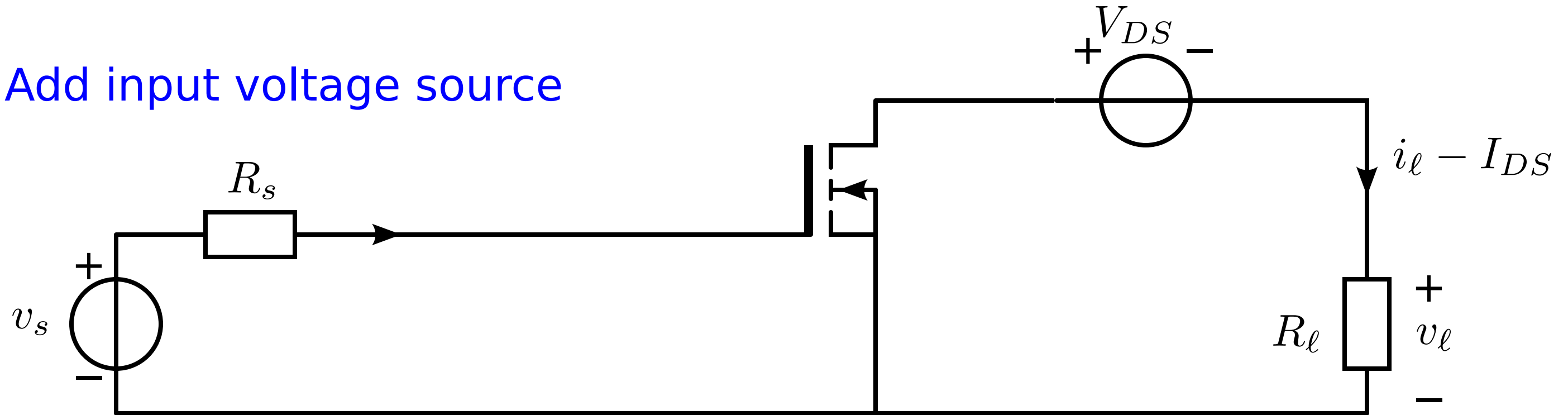
Add output voltage source



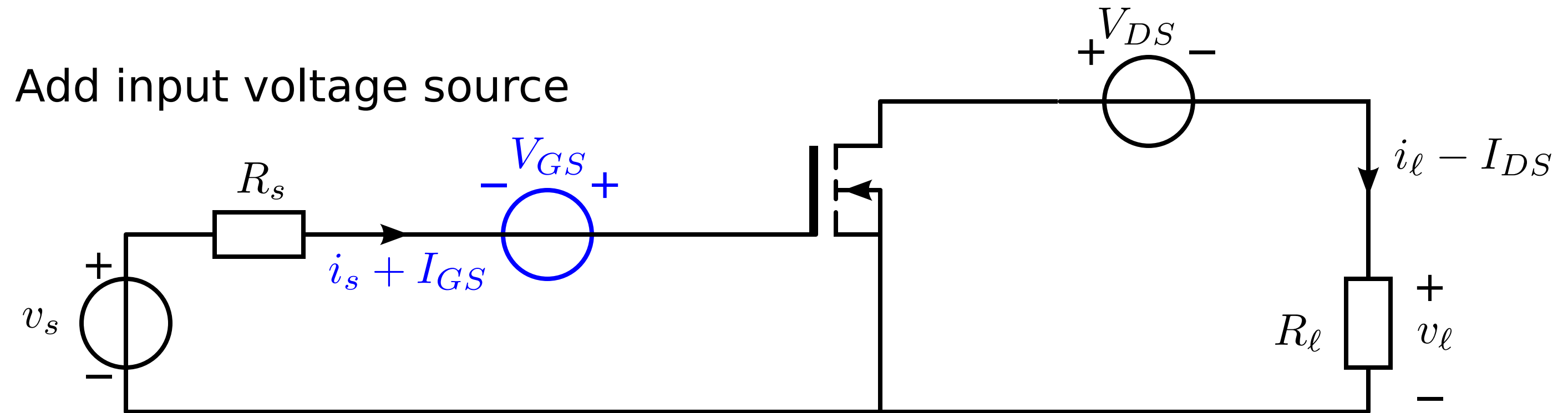
Load signal if the source voltage exceeds the threshold voltage
No unique correspondence between source and load signal values

Amplification and biasing

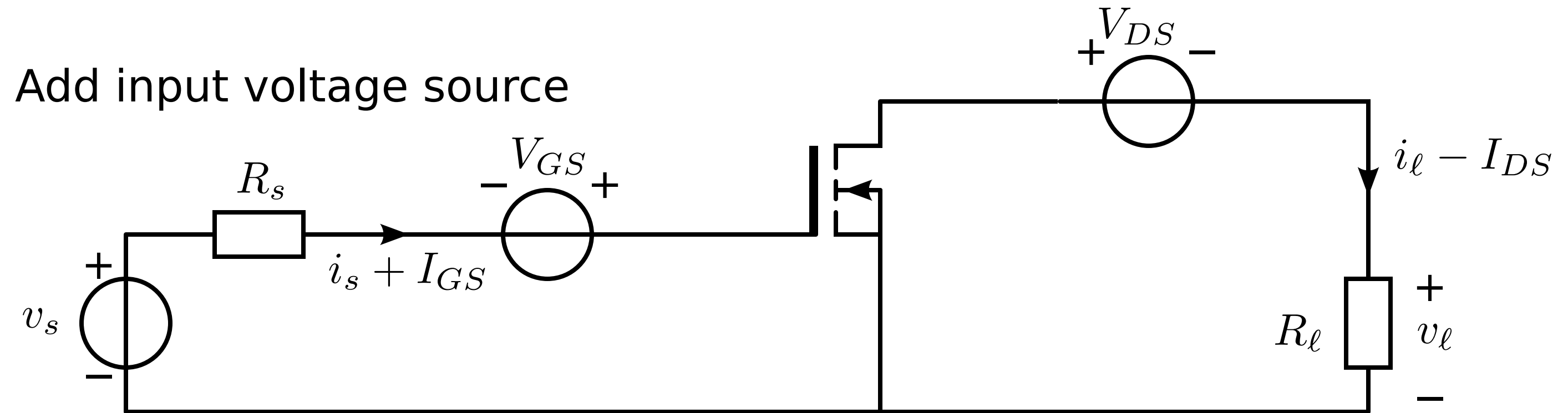
Add input voltage source



Amplification and biasing



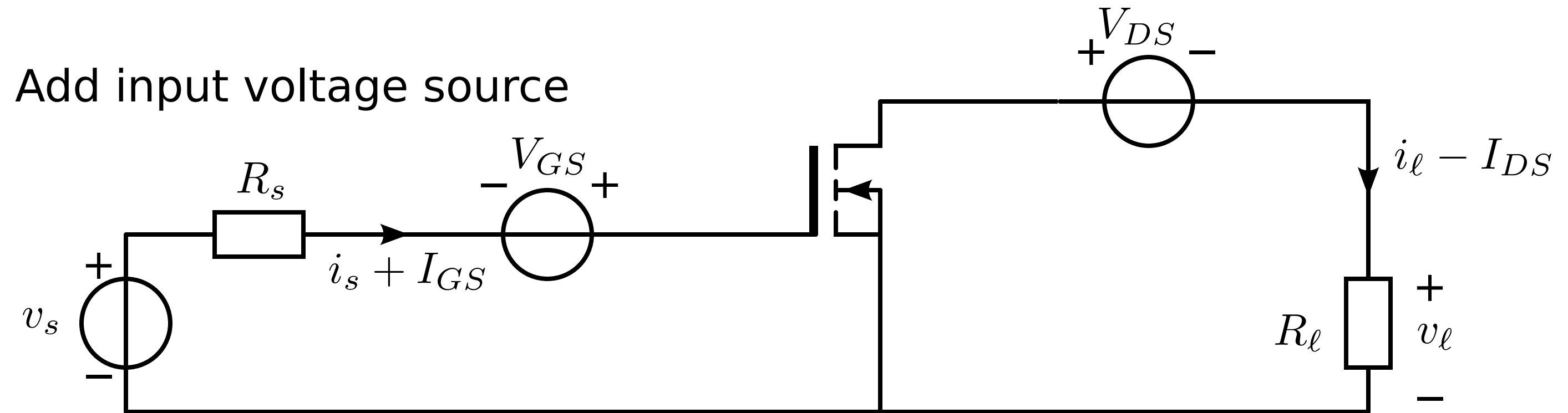
Amplification and biasing



Load signal for all values of the source signal if:

$$V_{GS} + v_s > V_{th} \text{ (threshold voltage)}$$

Amplification and biasing

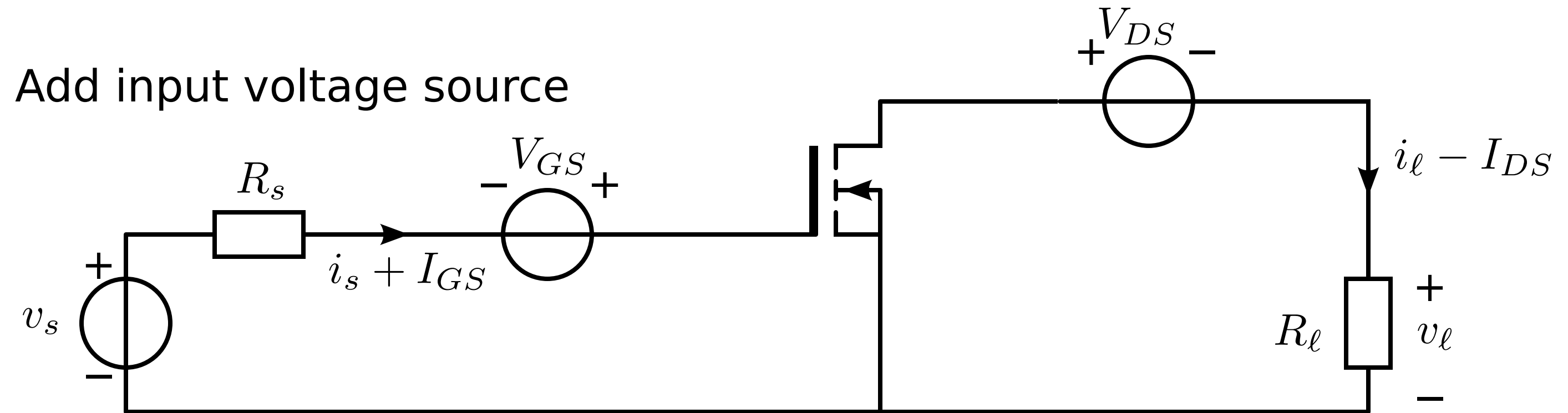


Load signal for all values of the source signal if:

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Unique correspondence between the source voltage and the load voltage

Amplification and biasing



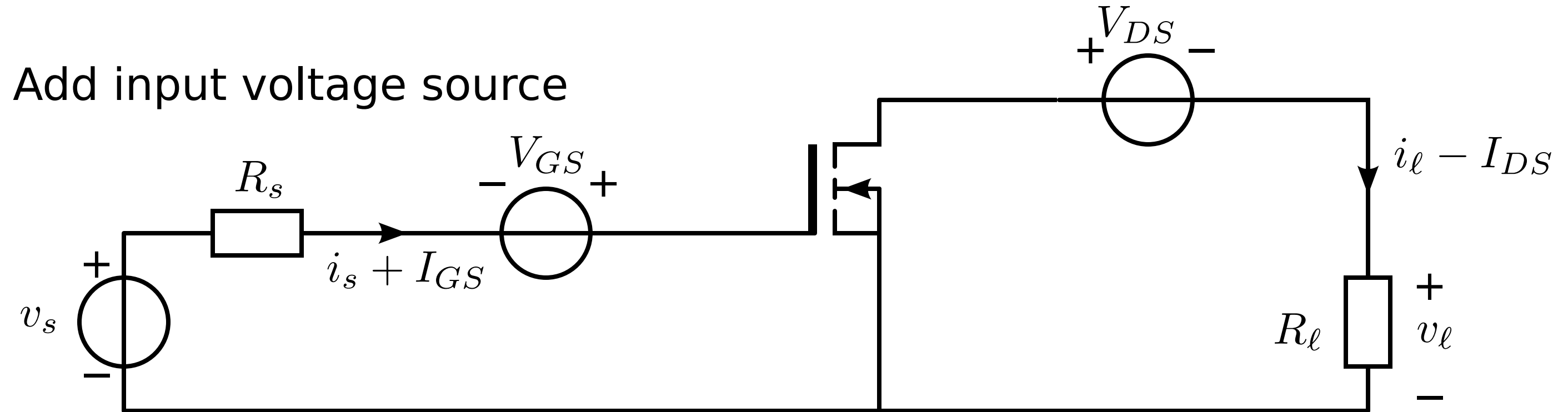
Load signal for all values of the source signal if:

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Unique correspondence between the source voltage and the load voltage

I_{GS} and I_{DS} bias currents flow through the source and the load

Amplification and biasing



Load signal for all values of the source signal if:

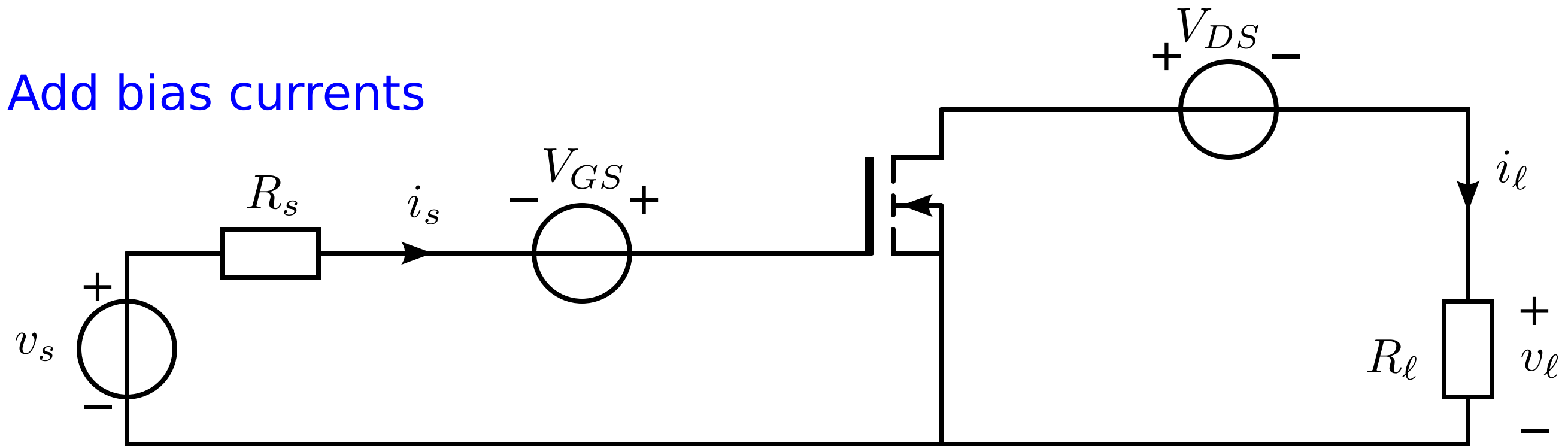
$$V_{GS} + v_s > V_{th} \text{ (threshold voltage)}$$

Unique correspondence between the source voltage and the load voltage

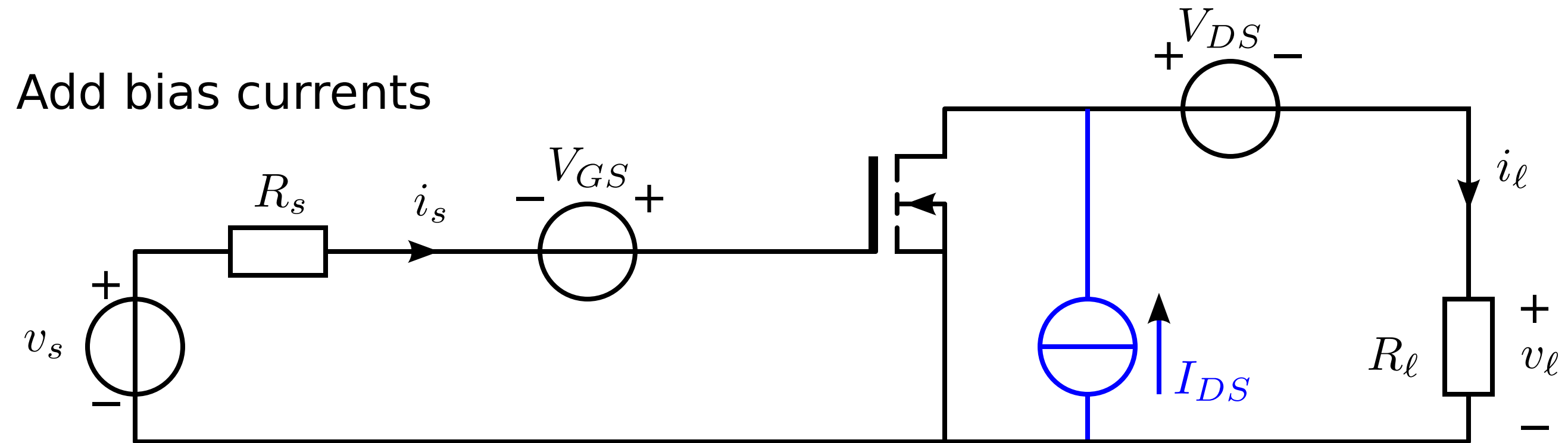
I_{GS} and I_{DS} bias currents flow through the source and the load

Amplification and biasing

Add bias currents

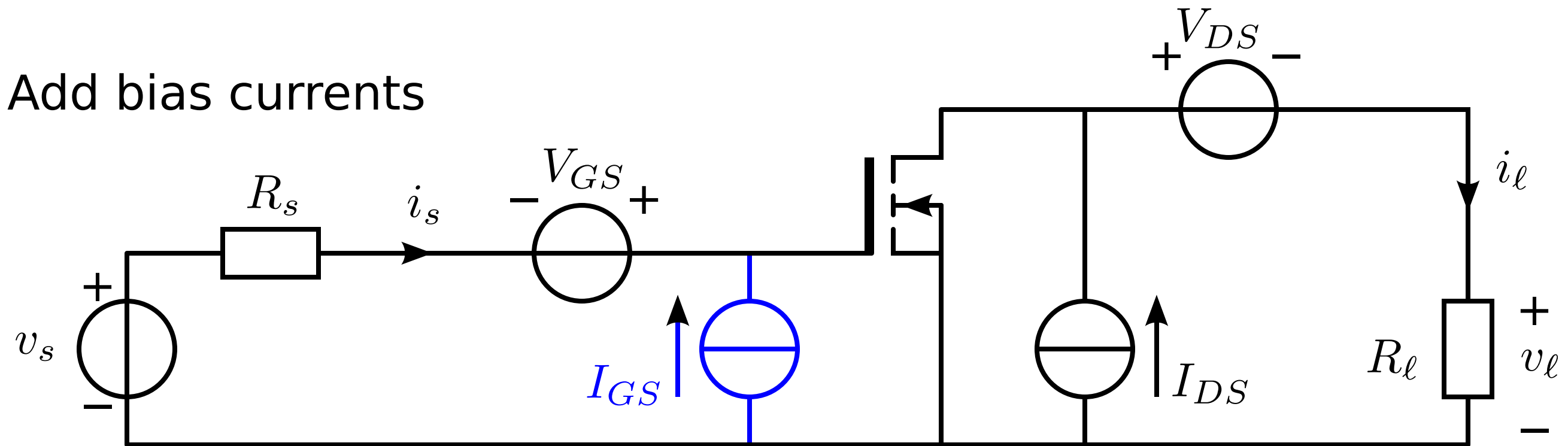


Amplification and biasing

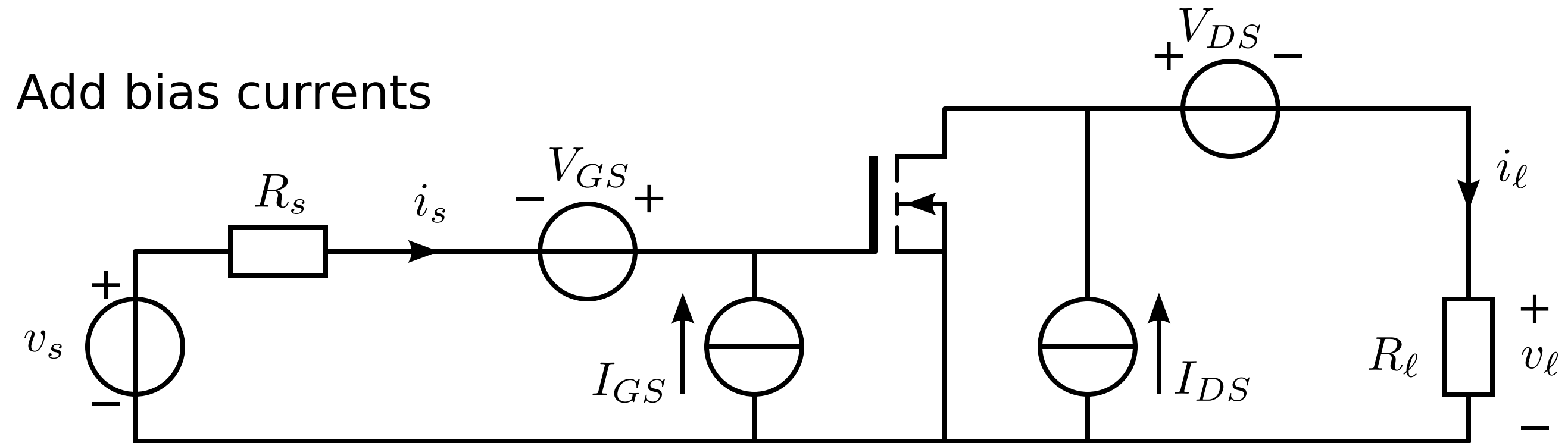


Amplification and biasing

Add bias currents

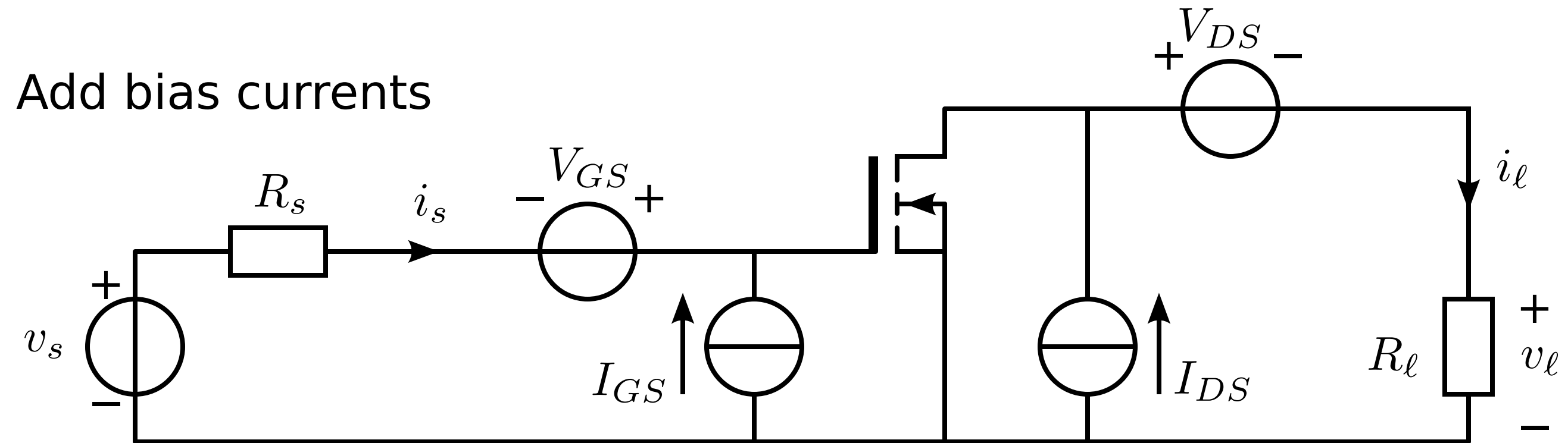


Amplification and biasing



No bias currents flow through the source and the load

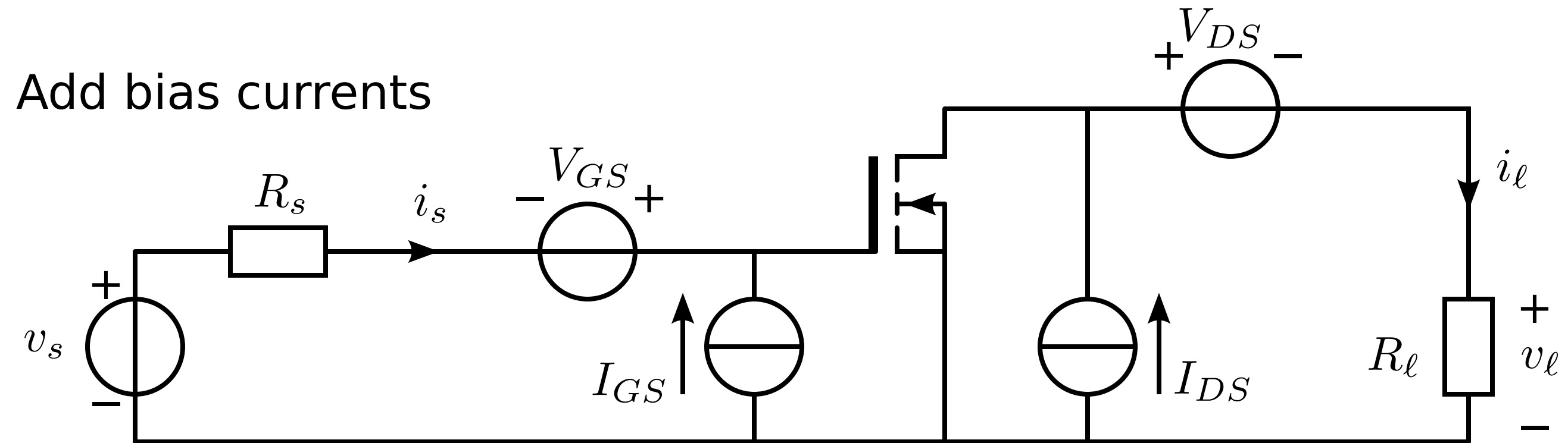
Amplification and biasing



No bias currents flow through the source and the load

(v_s, v_ℓ) , (v_s, i_ℓ) , (i_s, v_ℓ) , (i_s, i_ℓ) characteristics pass through the origin

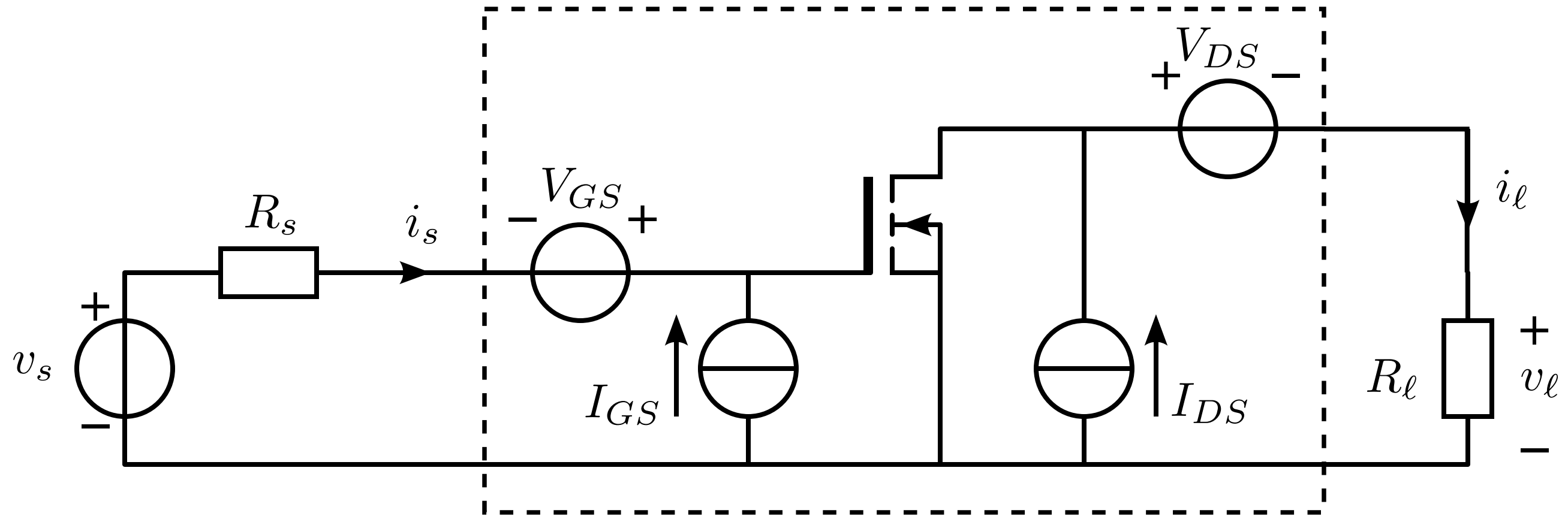
Amplification and biasing



No bias currents flow through the source and the load

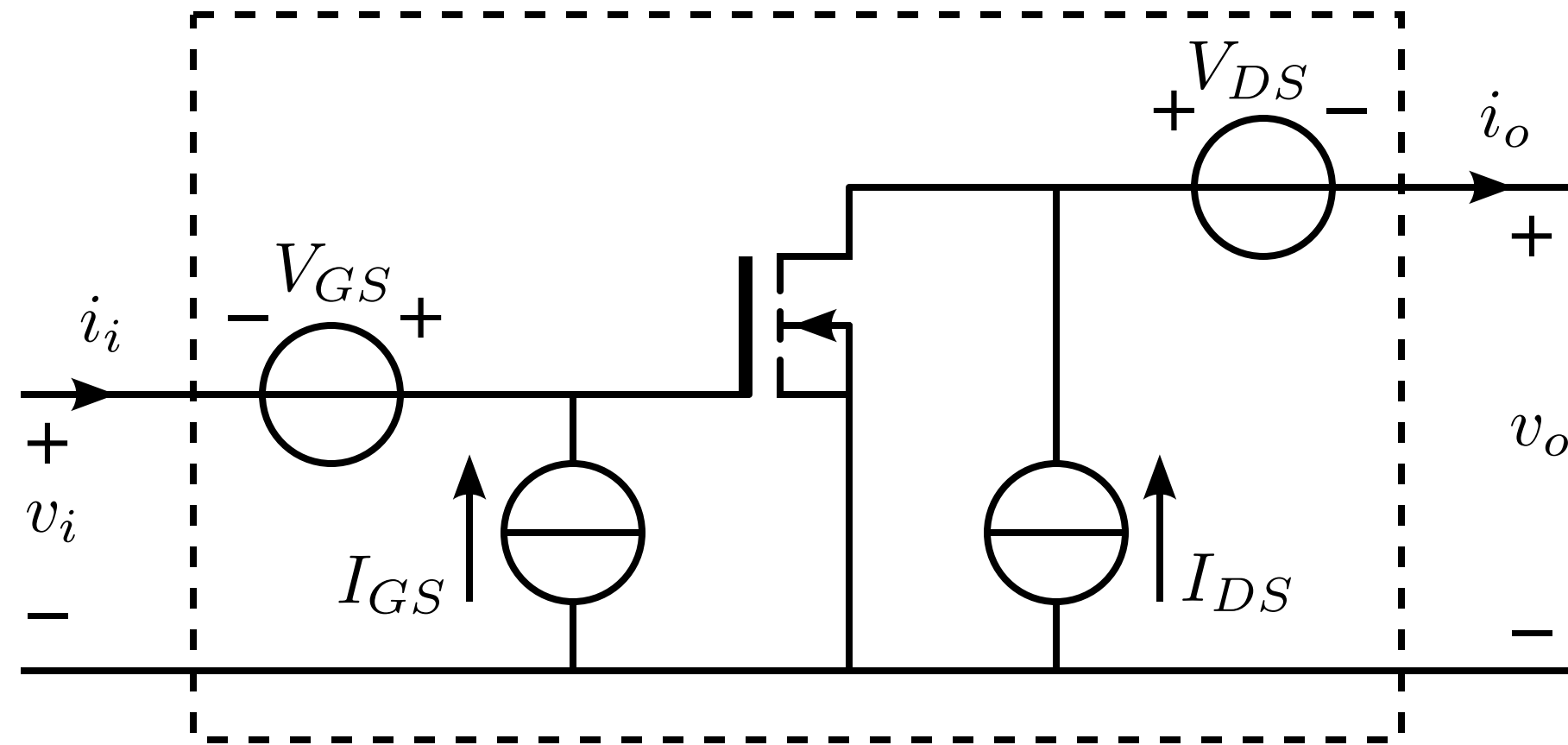
(v_s, v_ℓ) , (v_s, i_ℓ) , (i_s, v_ℓ) , (i_s, i_ℓ) characteristics pass through the origin

Amplification and biasing



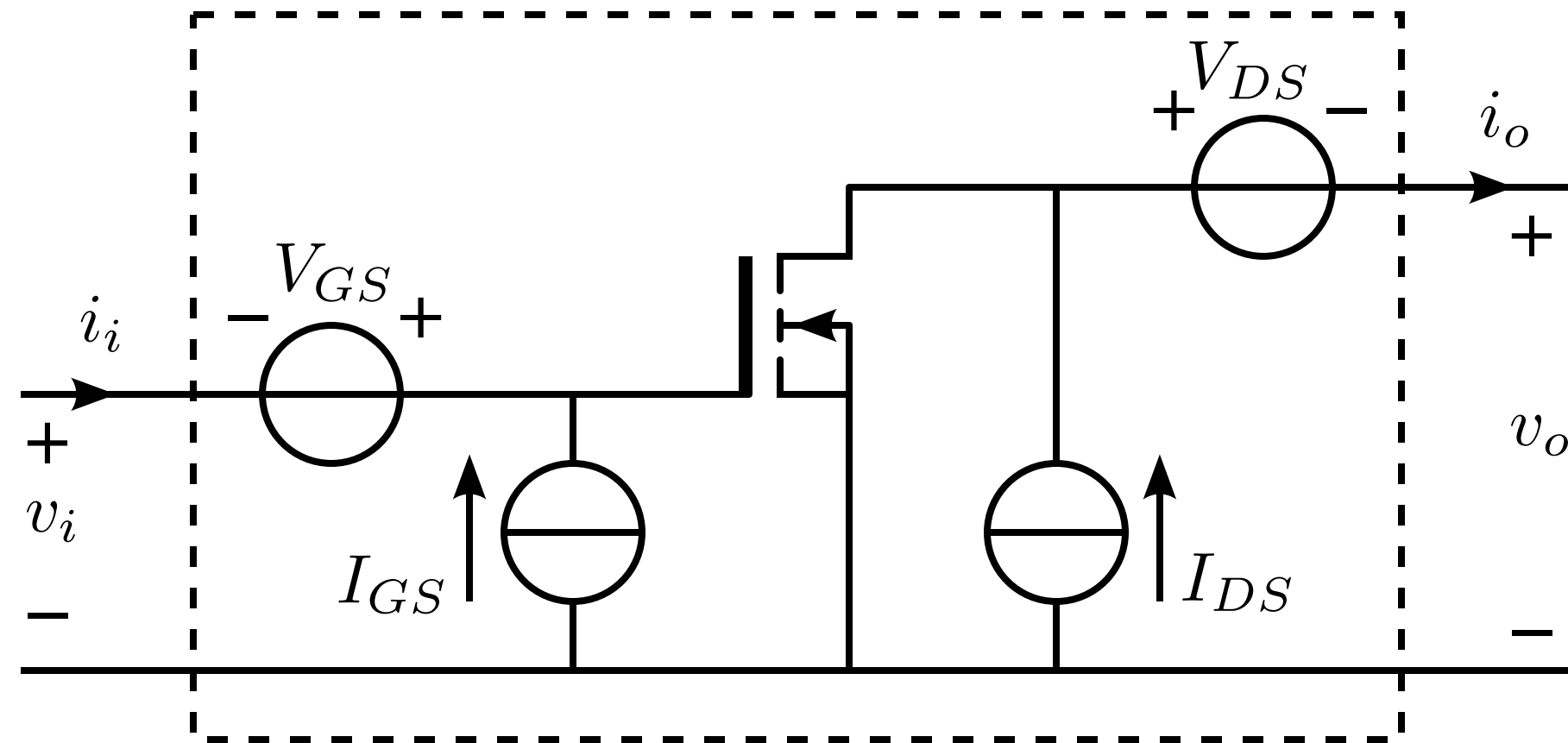
Biased amplifier stage

Amplification and biasing



Biased amplifier stage

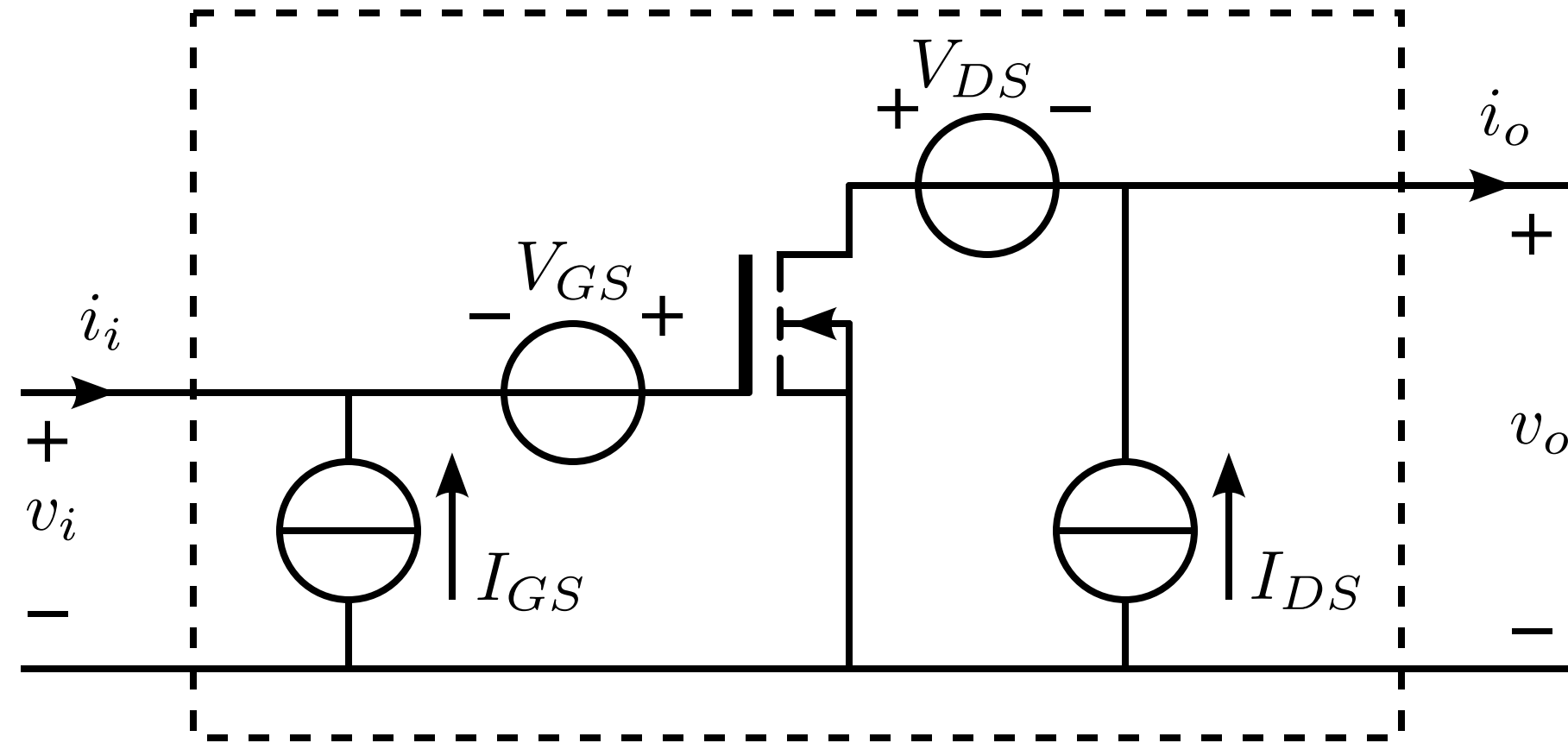
Amplification and biasing



Biased amplifier stage

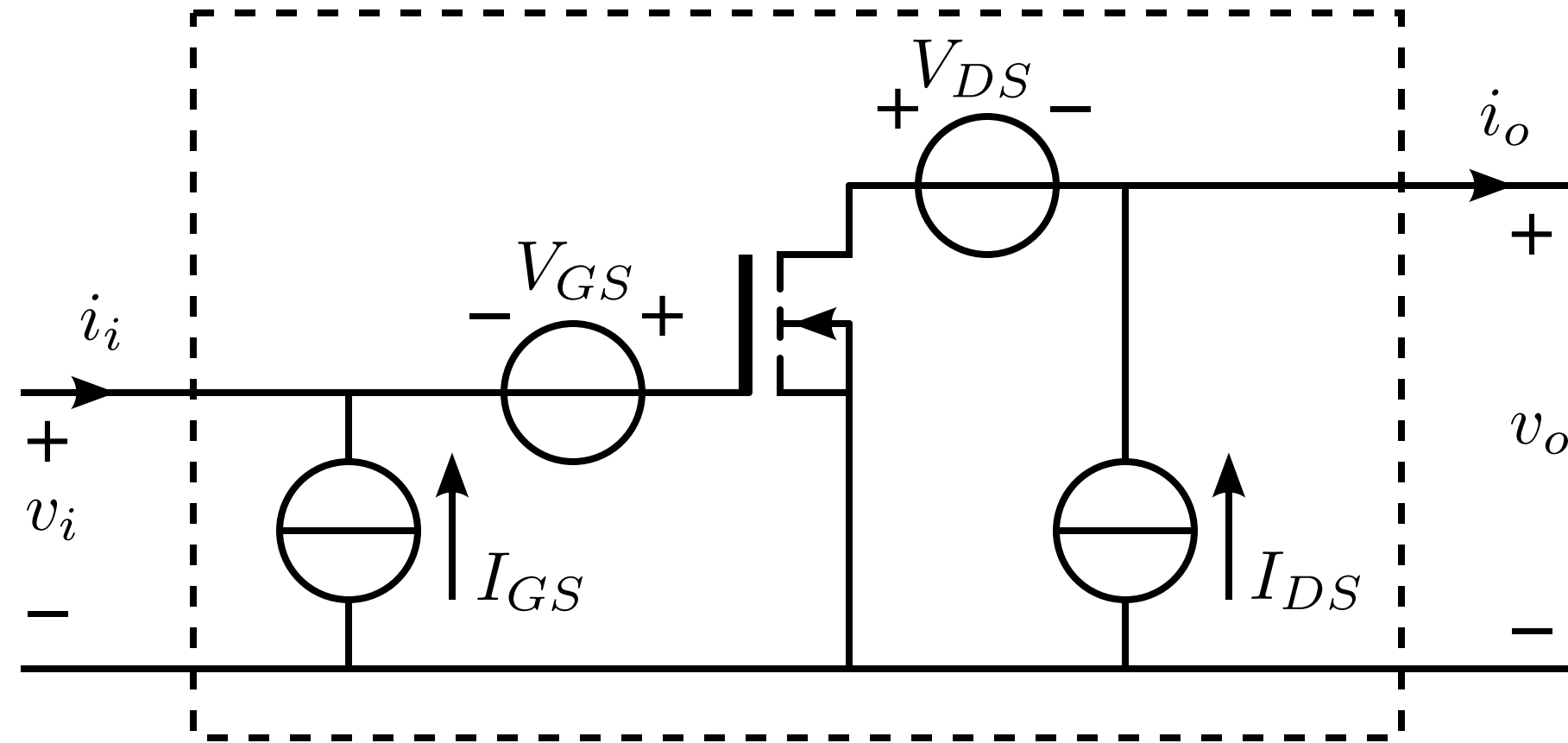
Bias power delivered by I_{GS} and I_{DS}

Amplification and biasing



Biased amplifier stage, alternative arrangement

Amplification and biasing

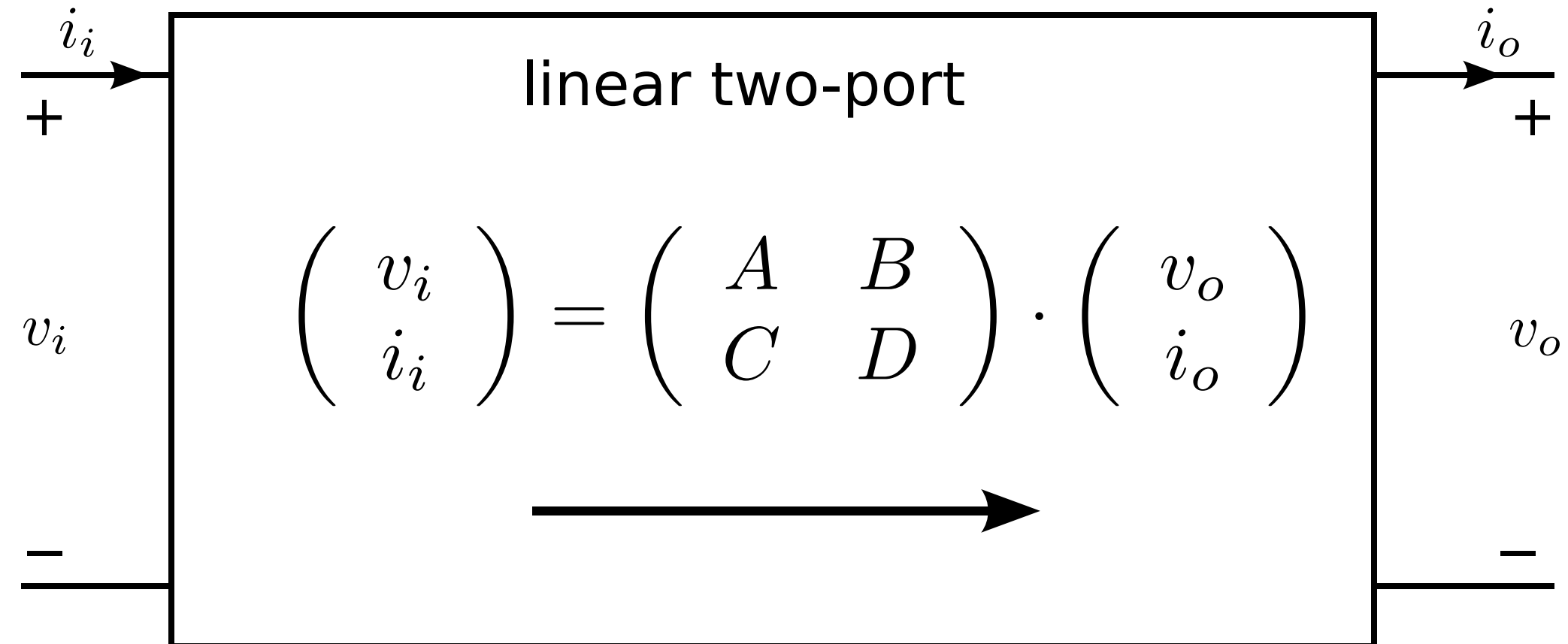


Biased amplifier stage, alternative arrangement

Bias power delivered by V_{GS} and V_{DS}

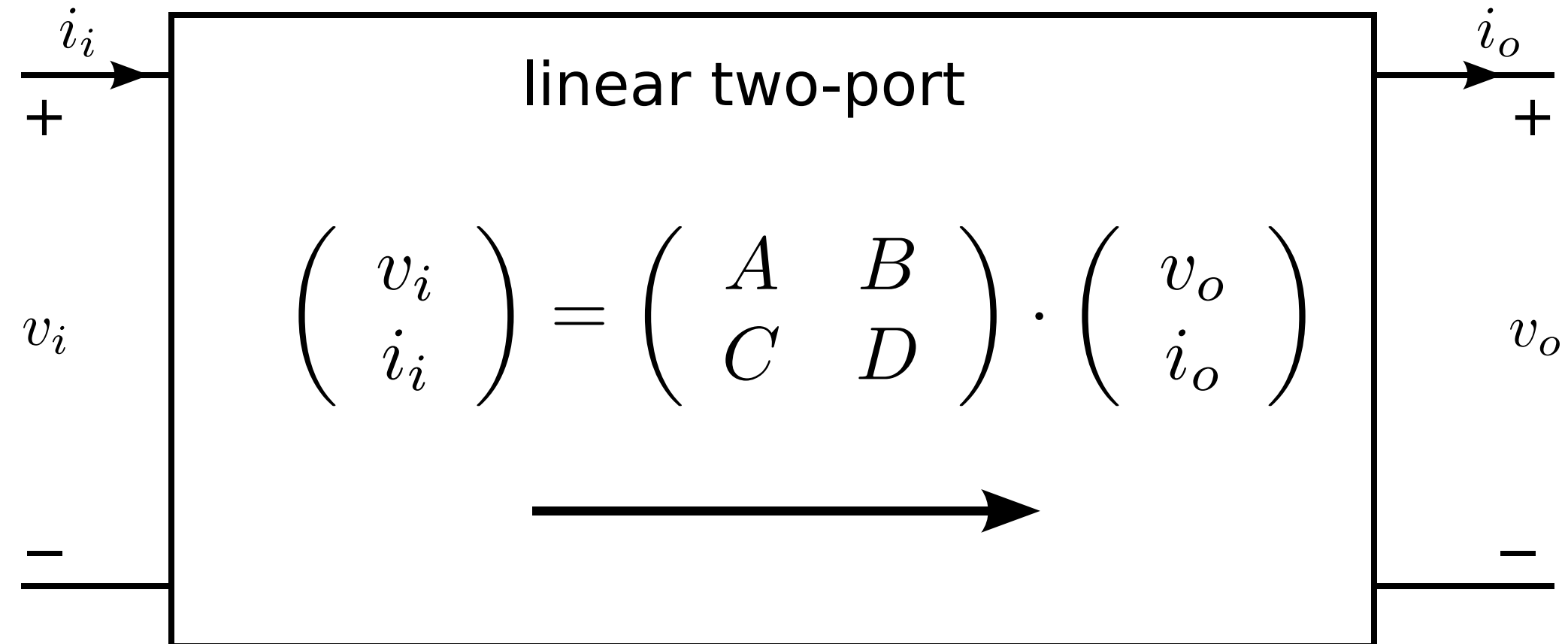
Amplification and biasing

Linearization in the operating point:



Amplification and biasing

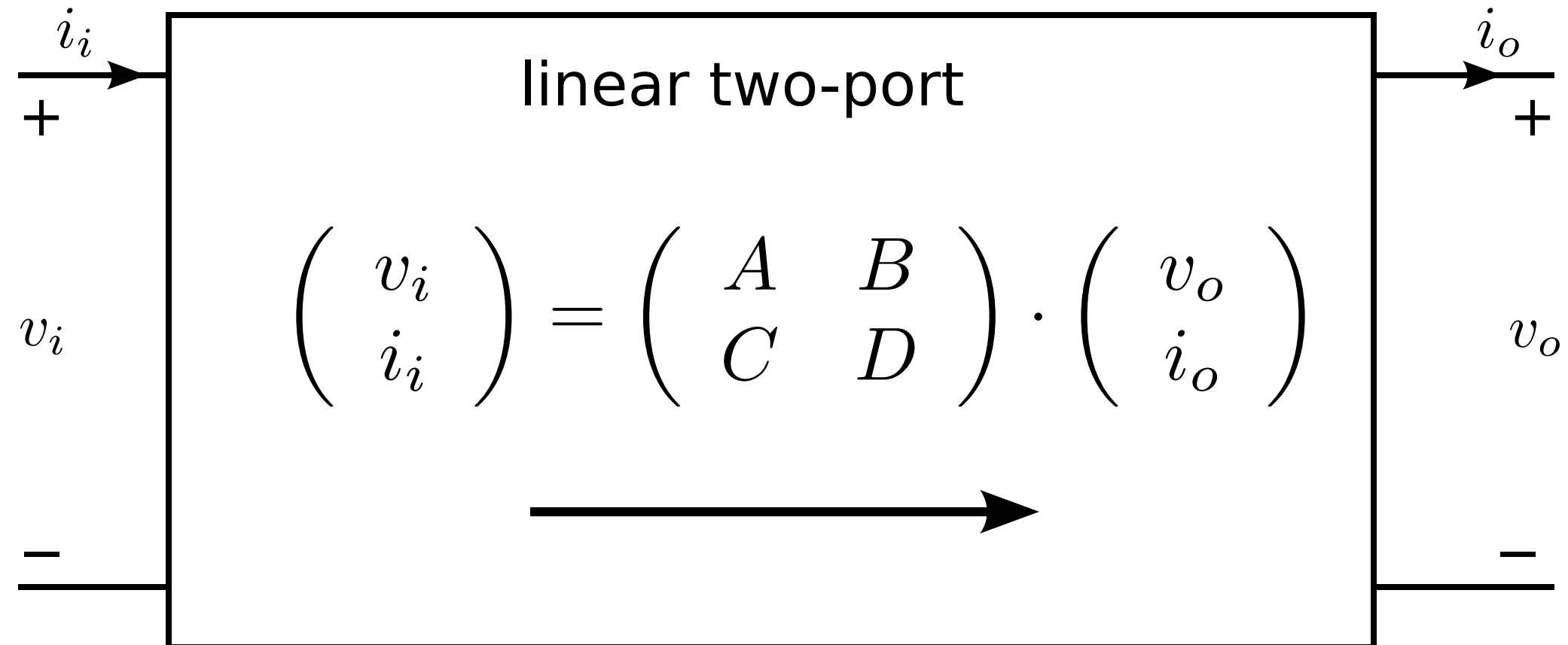
Linearization in the operating point:



Maximum available power gain of a unilateral linear resistive two-port:

Amplification and biasing

Linearization in the operating point:

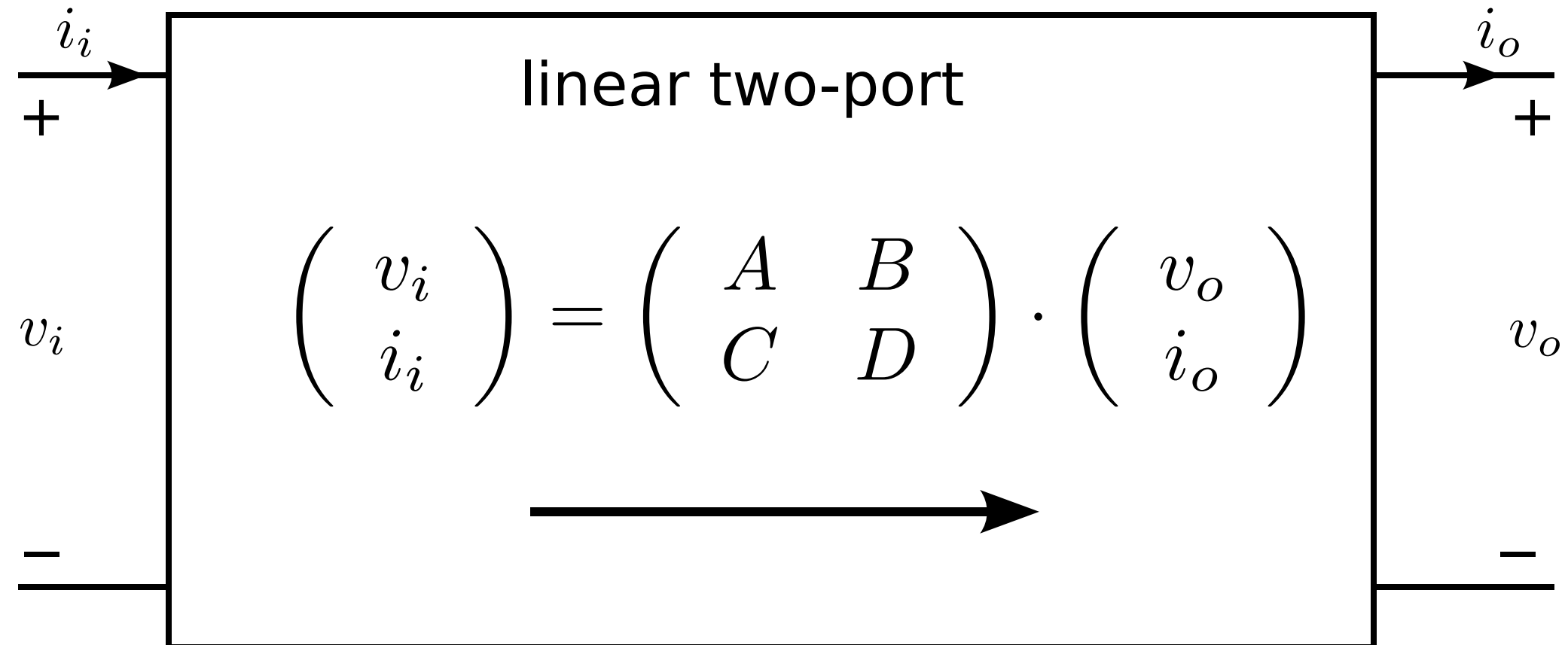


Maximum available power gain of a unilateral linear resistive two-port:

$$P_{av,\max} = \frac{1}{4AD}$$

Amplification and biasing

Linearization in the operating point:



Maximum available power gain of a unilateral linear resistive two-port:

$$P_{av,\max} = \frac{1}{4AD}$$