Structured Electronic Design

Principle of amplification and a formal approach to biasing

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Amplification and biasing

Source

Amplifier

Load

$R_s$ $i_s$ $i_\ell$

$v_s$ $v_\ell$

$R_\ell$
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Signal values at the load should have a unique correspondence with those of the source.
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The available power at the output of the amplifier should exceed that of the source.
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Device equations:

\[ I_{DS} = f(V_{DS}, V_{GS}) \]
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Only drain current if:

nonzero drain-source voltage
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Only drain current if:

- nonzero drain-source voltage
- gate-source voltage exceeds the threshold voltage
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Zero-signal operating point:
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Only drain current if:
- nonzero drain-source voltage
- gate-source voltage exceeds the threshold voltage

Zero-signal operating point:
\[ V_{GS} = 0 \quad V_{DS} = 0 \]
\[ I_{GS} = 0 \quad I_{DS} = 0 \]
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Device equations:

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Zero-signal operating point:

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No load signal
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No load signal
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Add output voltage source
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Add output voltage source
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Add output voltage source

Load signal if the source voltage exceeds the threshold voltage
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Add output voltage source

Load signal if the source voltage exceeds the threshold voltage

No unique correspondence between source and load signal values
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Add output voltage source

Load signal if the source voltage exceeds the threshold voltage
No unique correspondence between source and load signal values
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Add input voltage source
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Add input voltage source

\[ v_s \quad i_s + I_{GS} \quad -V_{GS}^+ \quad +V_{DS}^- \quad i_{\ell} - I_{DS} \quad R_{\ell} \quad v_{\ell}^- \]
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Add input voltage source

Load signal for all values of the source signal if:

\[ V_{GS} + v_s > V_{th} \] (threshold voltage)
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Add input voltage source

Load signal for all values of the source signal if:

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Unique correspondence between the source voltage and the load voltage
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Unique correspondence between the source voltage and the load voltage

\[ I_{GS} \text{ and } I_{DS} \] bias currents flow through the source and the load

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Unique correspondence between the source voltage and the load voltage

\[ I_{GS} \] and \[ I_{DS} \] bias currents flow through the source and the load
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Add bias currents
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Add bias currents

\[ v_s \rightarrow R_s \rightarrow i_s \rightarrow -V_{GS} \rightarrow + \]

\[ + \rightarrow V_{DS} \rightarrow - \rightarrow I_{DS} \rightarrow \]

\[ + \rightarrow R_f \rightarrow i_f \rightarrow + \]

\[ + \rightarrow v_f \rightarrow - \]
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Add bias currents
Amplification and biasing

Add bias currents

No bias currents flow through the source and the load
Amplification and biasing

Add bias currents

No bias currents flow through the source and the load

\((v_s, v_\ell), (v_s, i_\ell), (i_s, v_\ell), (i_s, i_\ell)\) characteristics pass through the origin
No bias currents flow through the source and the load

\((v_s, v_{\ell}), (v_s, i_{\ell}), (i_s, v_{\ell}), (i_s, i_{\ell})\) characteristics pass through the origin
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Biased amplifier stage
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Biased amplifier stage

Bias power delivered by $I_{GS}$ and $I_{DS}$
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Biased amplifier stage, alternative arrangement
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Biased amplifier stage, alternative arrangement

Bias power delivered by $V_{GS}$ and $V_{DS}$
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Linearization in the operating point:

\[
\begin{pmatrix}
    v_i \\
    i_i
\end{pmatrix}
= \begin{pmatrix}
    A & B \\
    C & D
\end{pmatrix}
\cdot
\begin{pmatrix}
    v_o \\
    i_o
\end{pmatrix}
\]
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Linearization in the operating point:

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Maximum available power gain of a unilateral linear resistive two-port:
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Maximum available power gain of a unilateral linear resistive two-port:

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P_{av,\text{max}} = \frac{1}{4AD}
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