

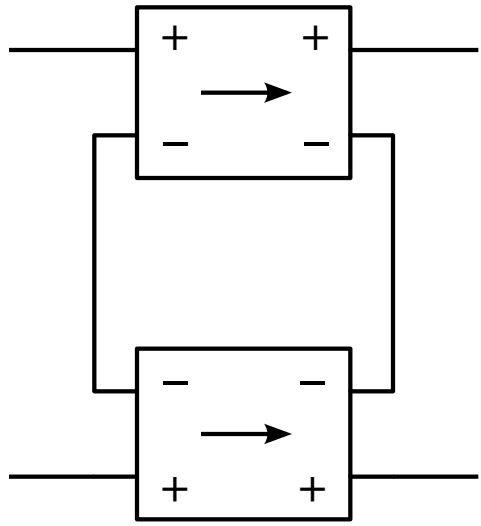
Structured Electronic Design

Balancing: differential pair

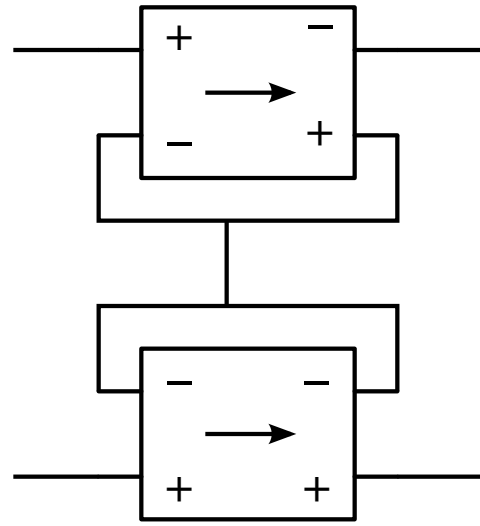
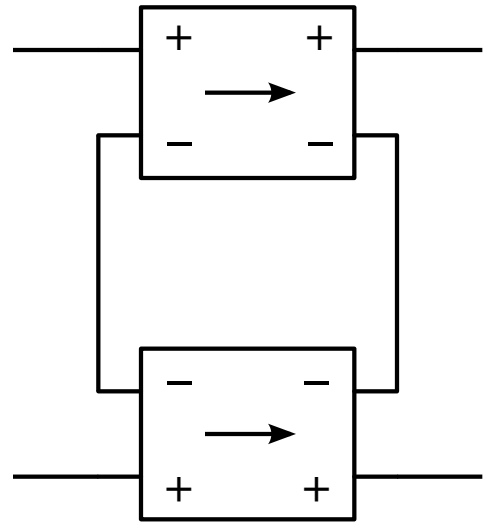
Anton J.M. Montagne

Anti-series connected CS stages

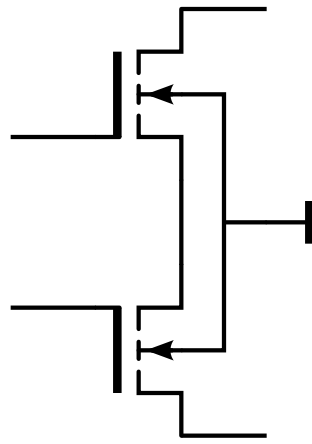
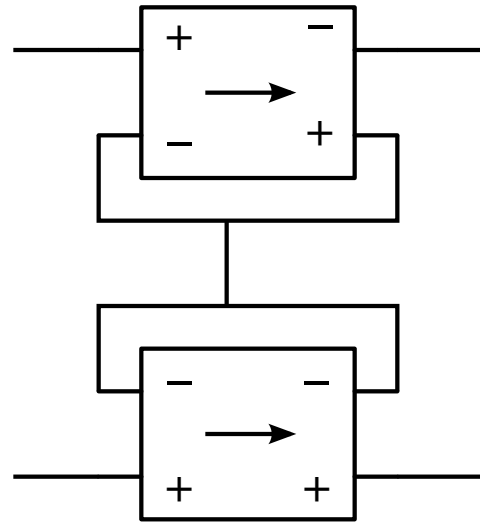
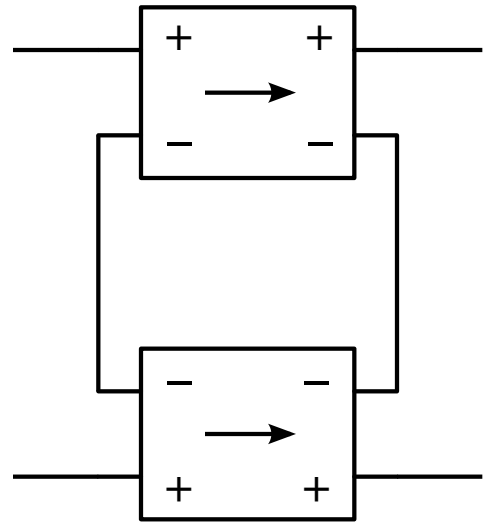
Anti-series connected CS stages



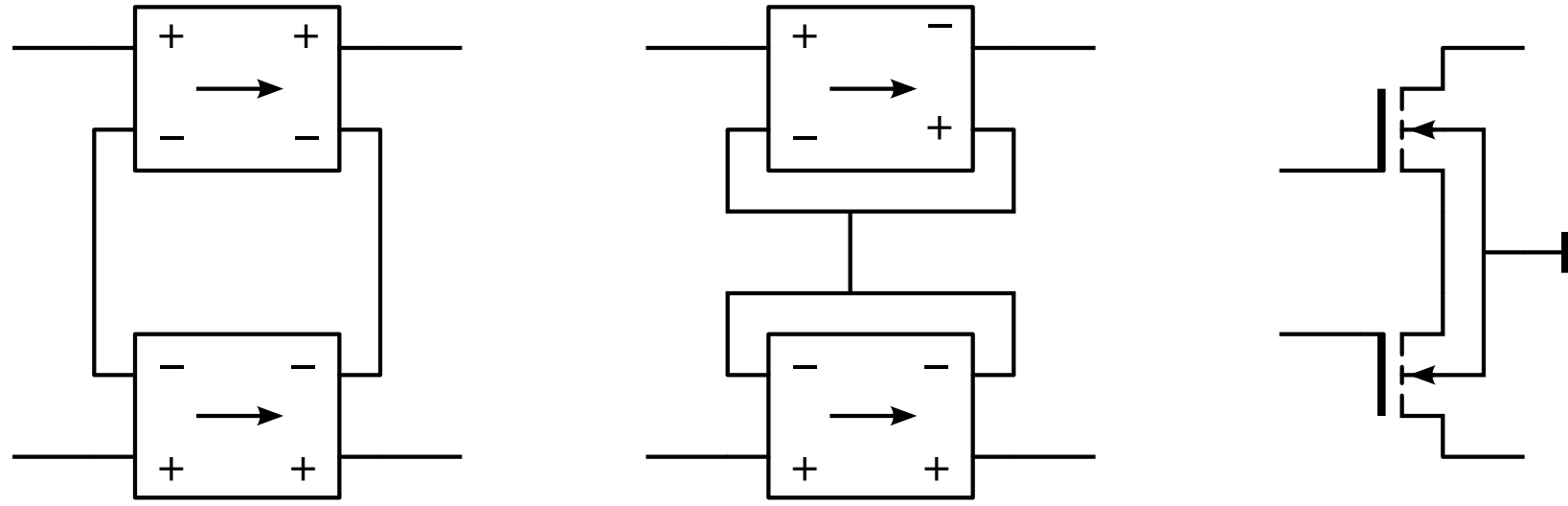
Anti-series connected CS stages



Anti-series connected CS stages

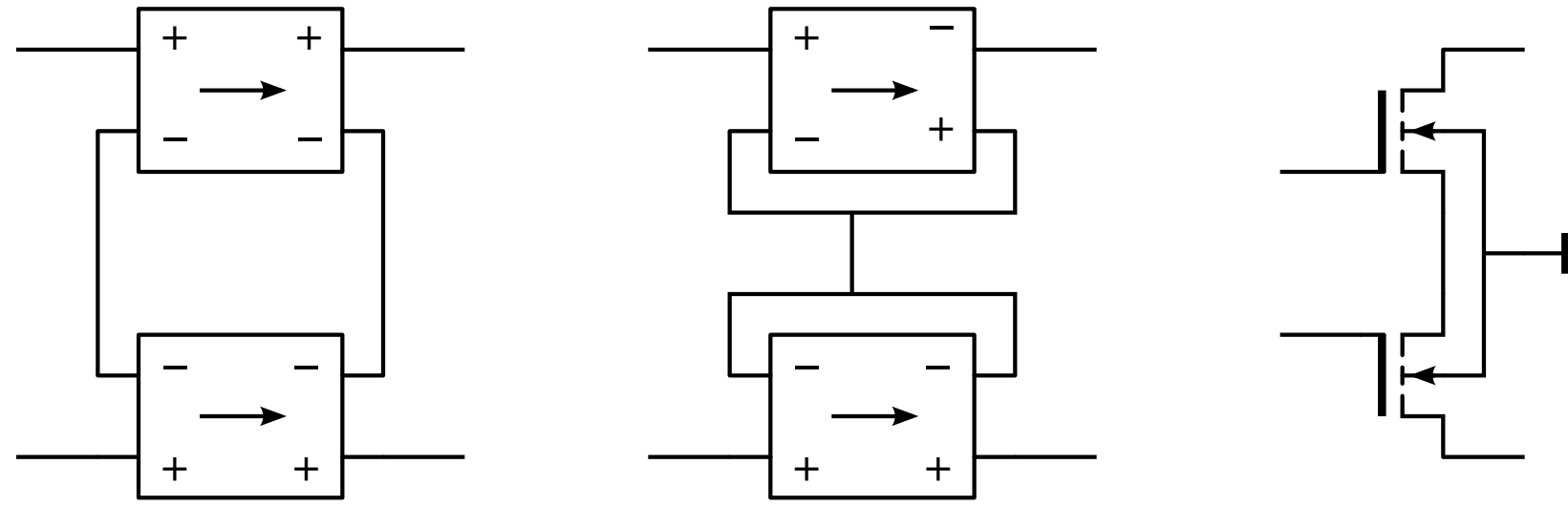


Anti-series connected CS stages

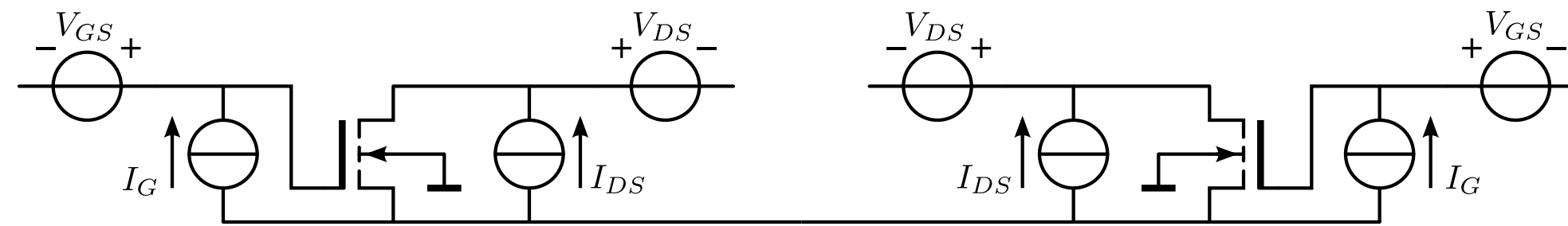


Anti-series biased CS stages

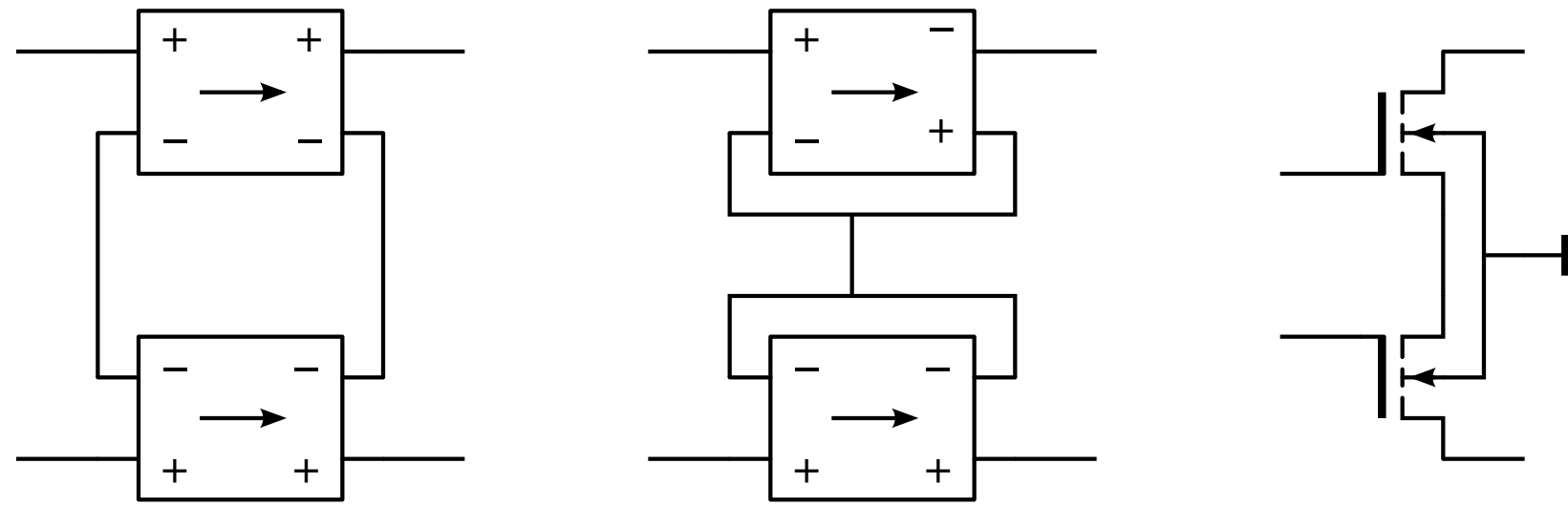
Anti-series connected CS stages



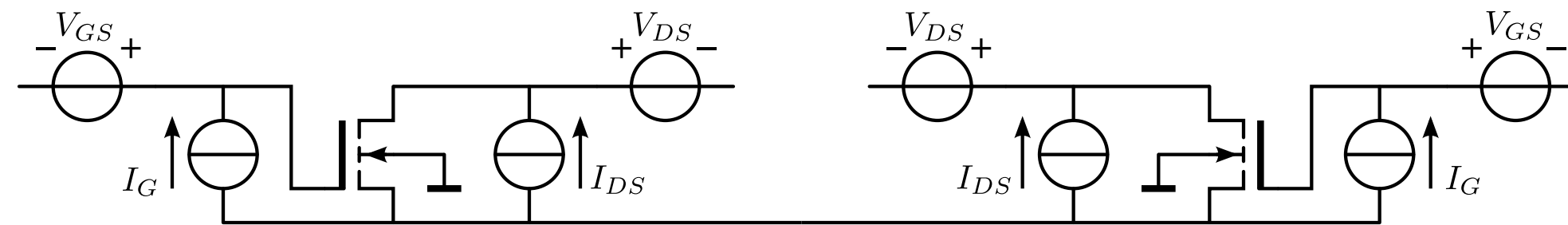
Anti-series biased CS stages



Anti-series connected CS stages

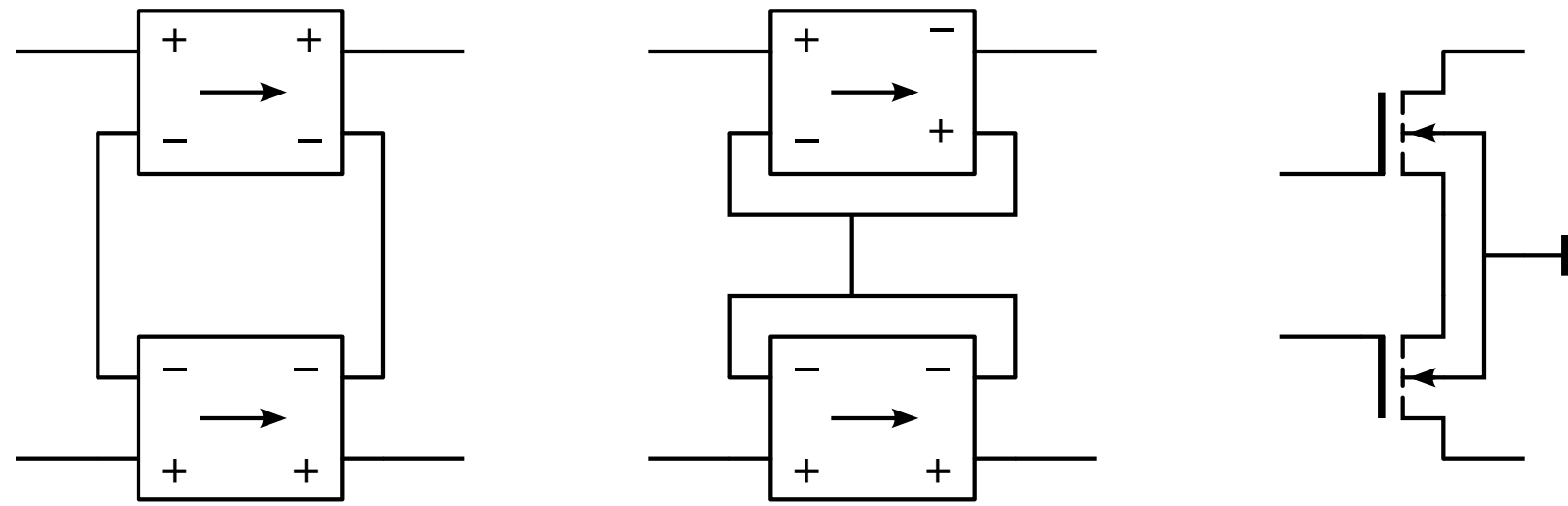


Anti-series biased CS stages

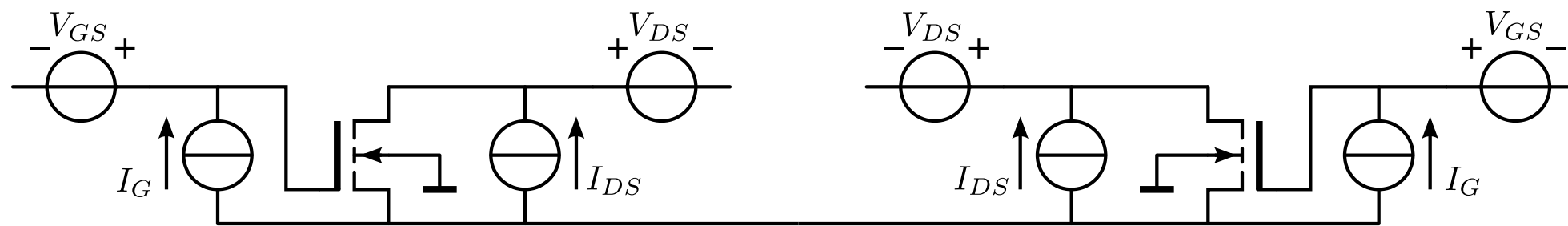


Four-terminal stage with improved port isolation

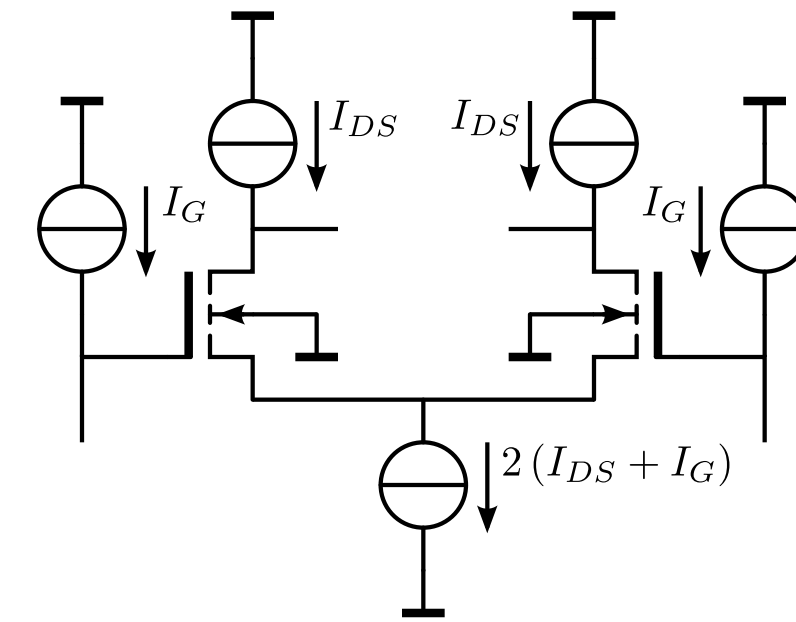
Anti-series connected CS stages



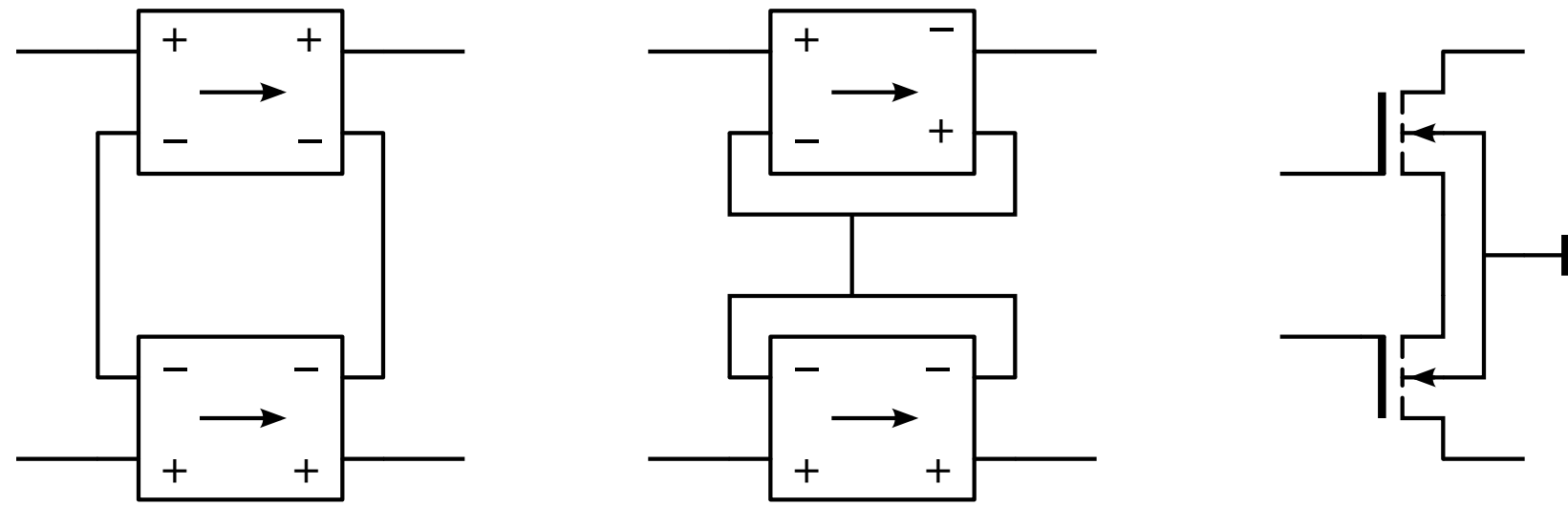
Anti-series biased CS stages



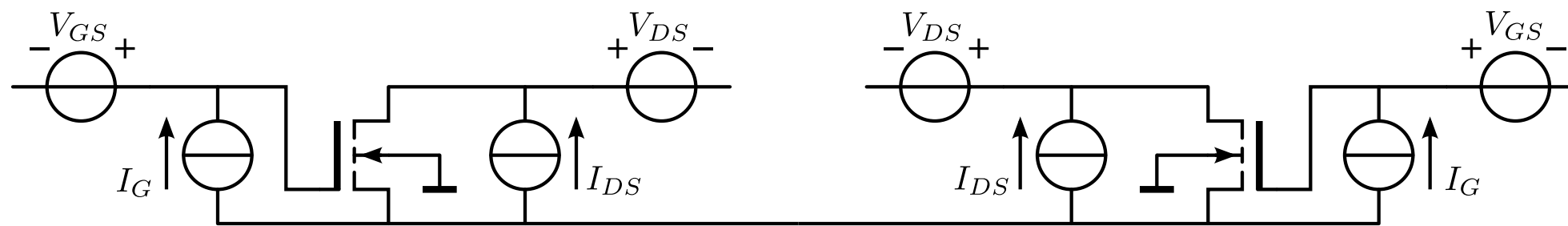
Four-terminal stage with improved port isolation



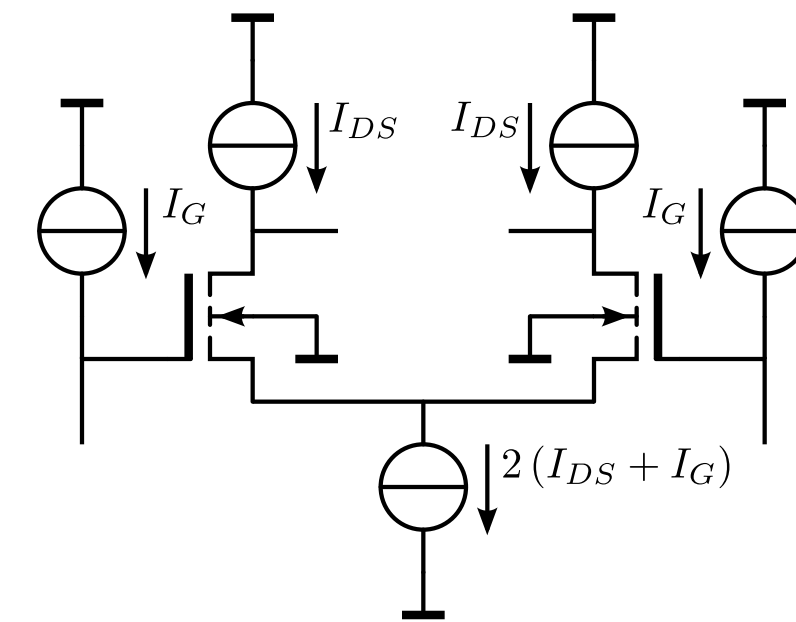
Anti-series connected CS stages



Anti-series biased CS stages

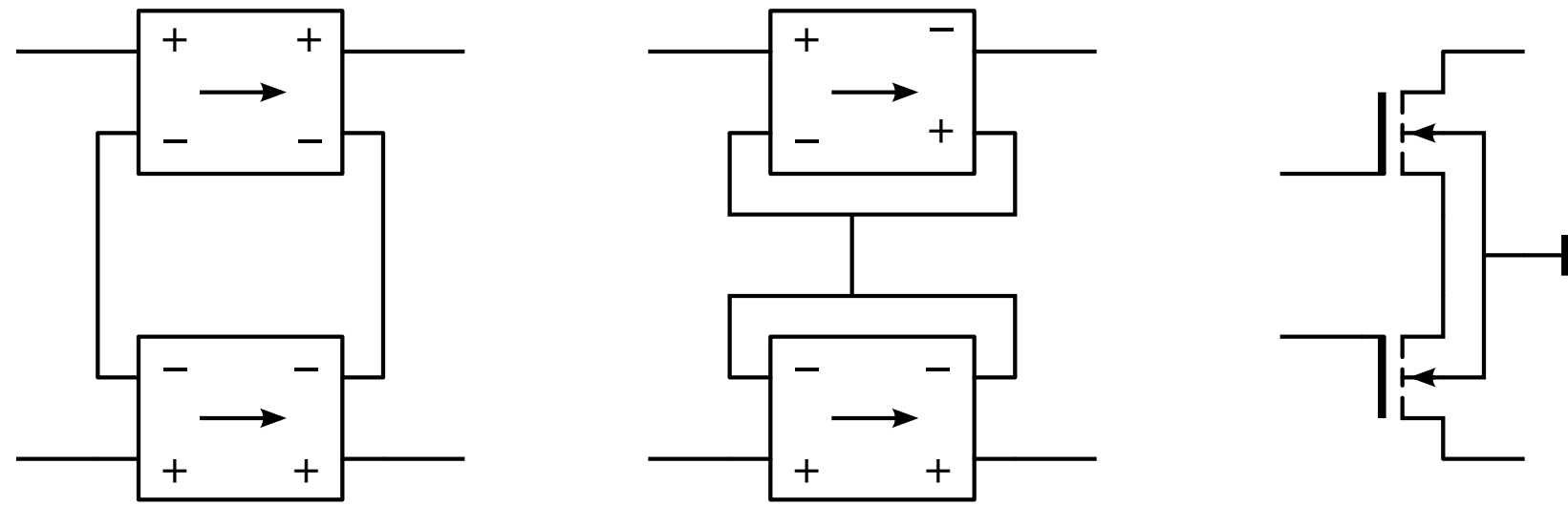


Four-terminal stage with improved port isolation

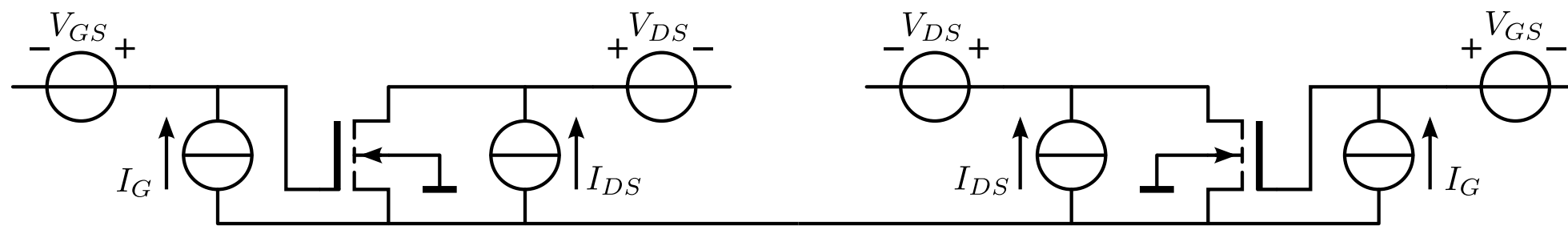


Common-mode voltage at one port has to be defined in the application

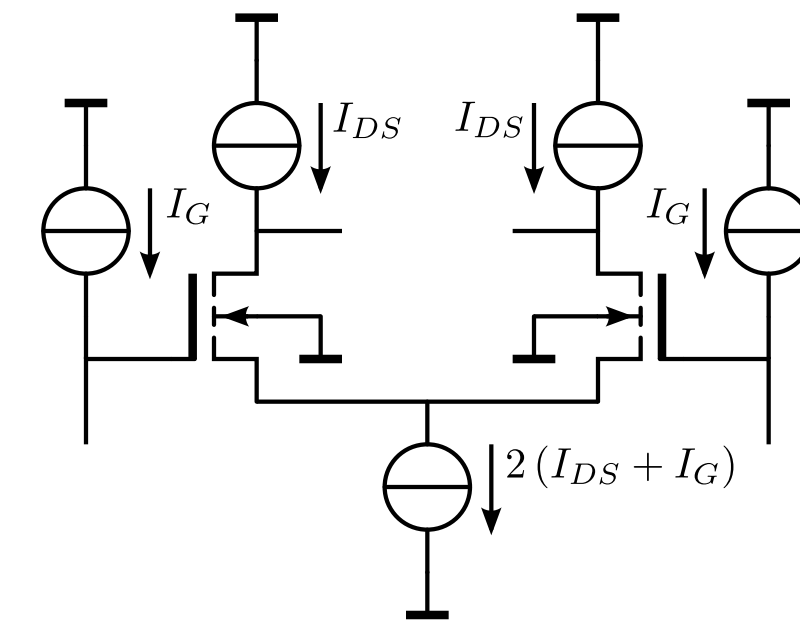
Anti-series connected CS stages



Anti-series biased CS stages



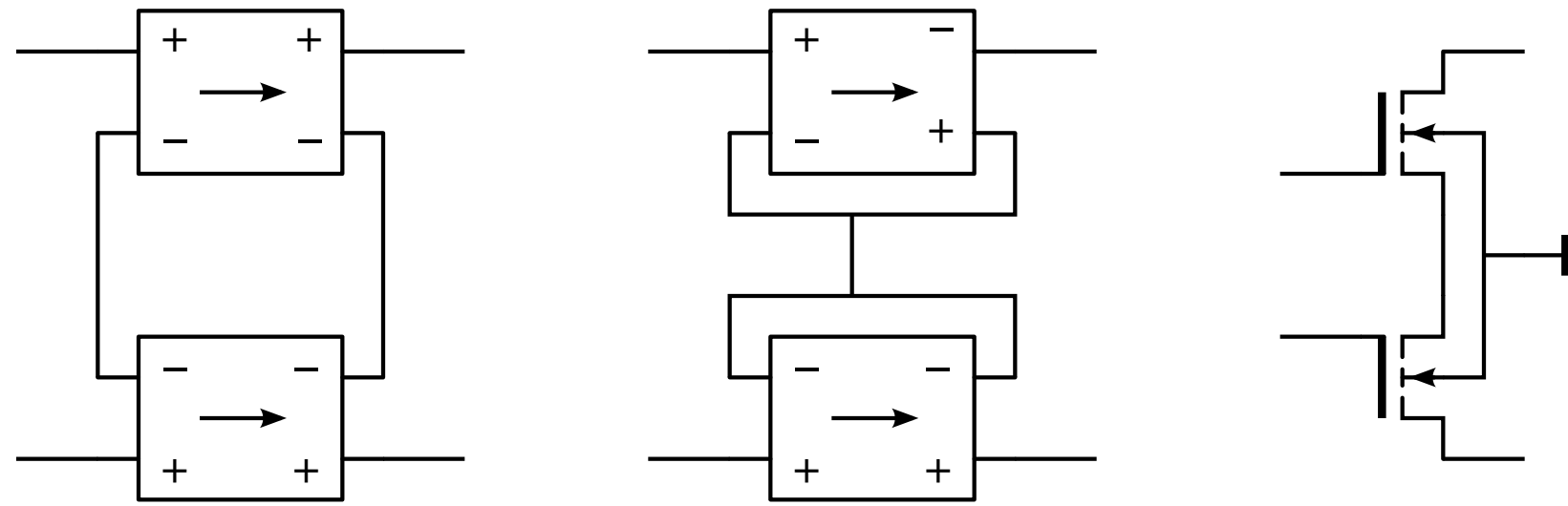
Four-terminal stage with improved port isolation



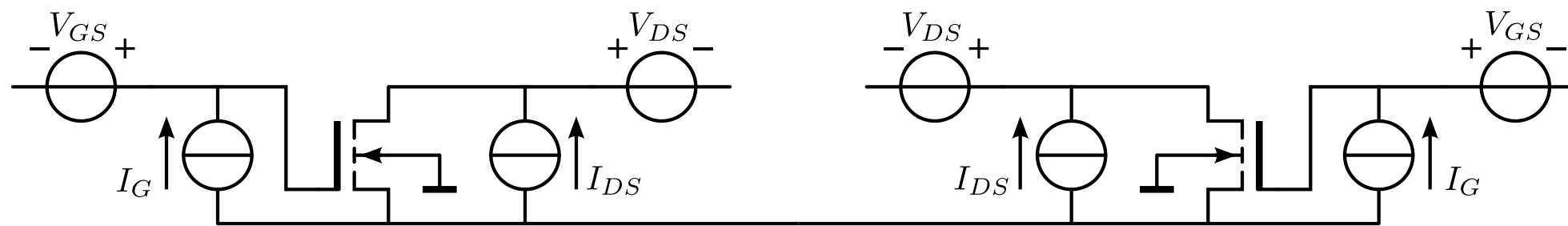
Common-mode voltage at one port has to be defined in the application

Common-mode voltage at the other port defined by CM bias sources and device characteristics

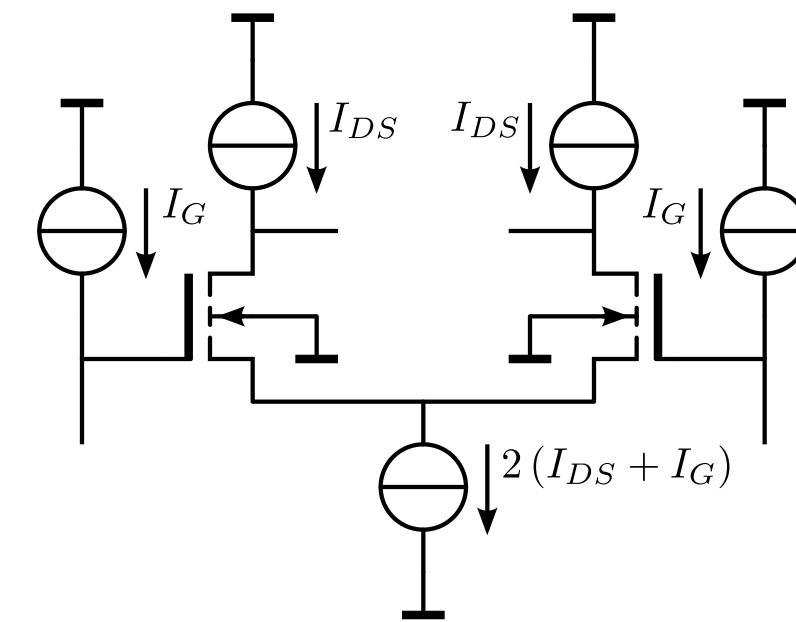
Anti-series connected CS stages



Anti-series biased CS stages



Four-terminal stage with improved port isolation

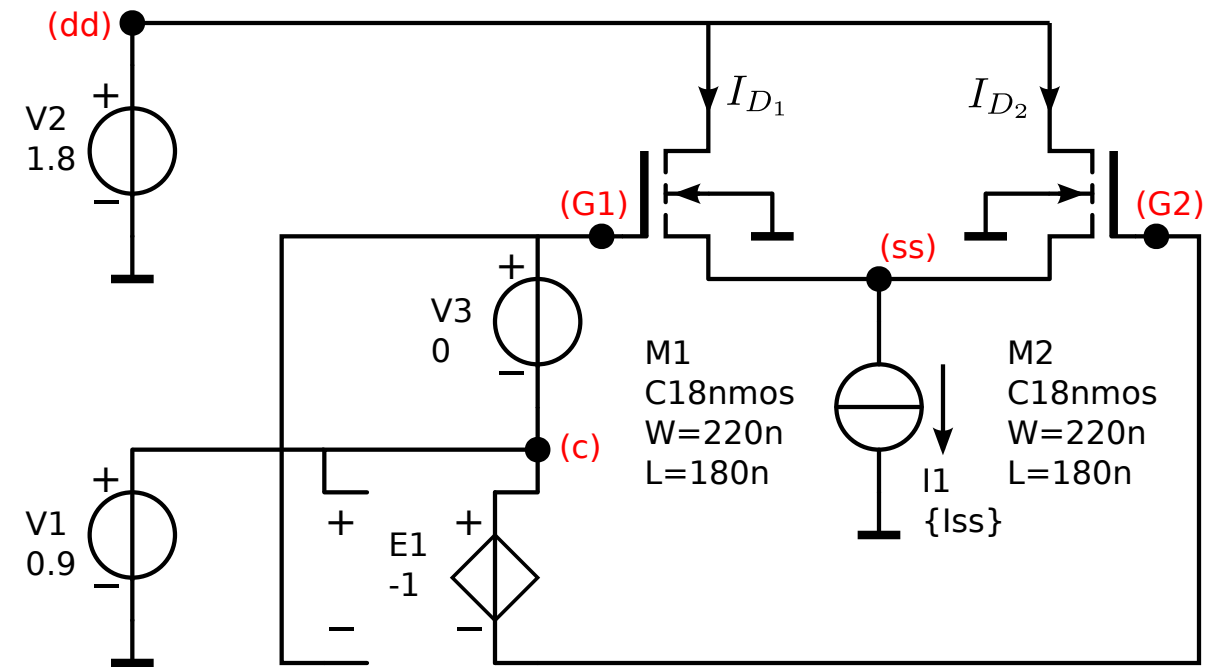


Common-mode voltage at one port has to be defined in the application

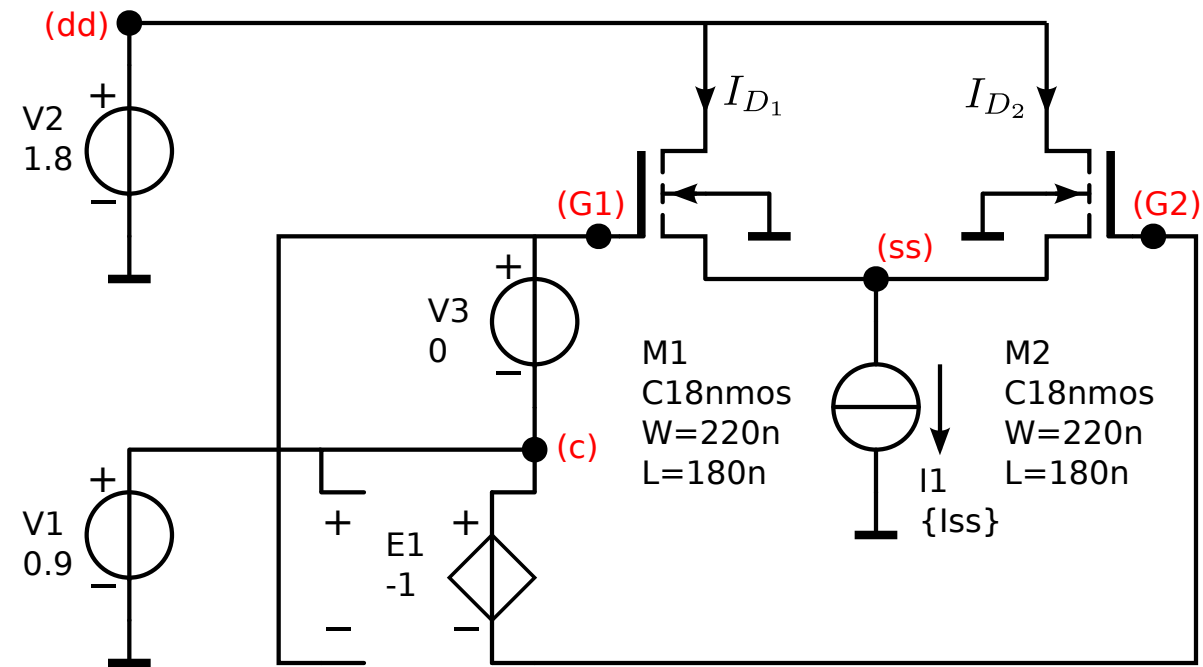
Common-mode voltage at the other port defined by CM bias sources and device characteristics

Differential pair V-I transfer

Differential pair V-I transfer

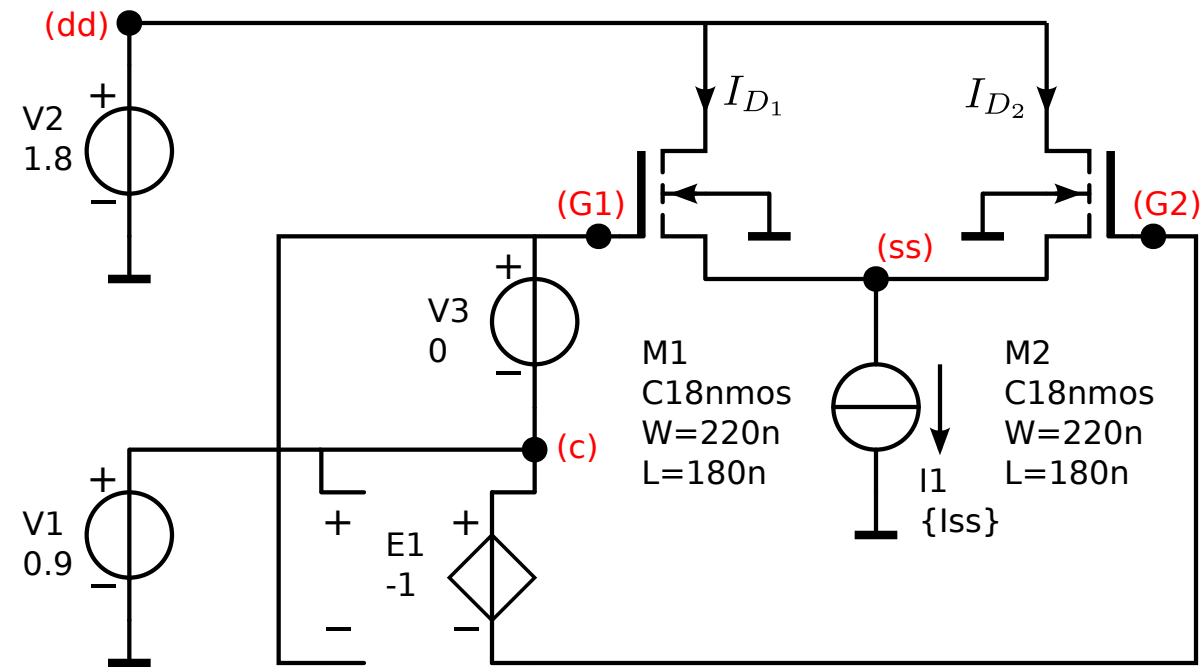


Differential pair V-I transfer

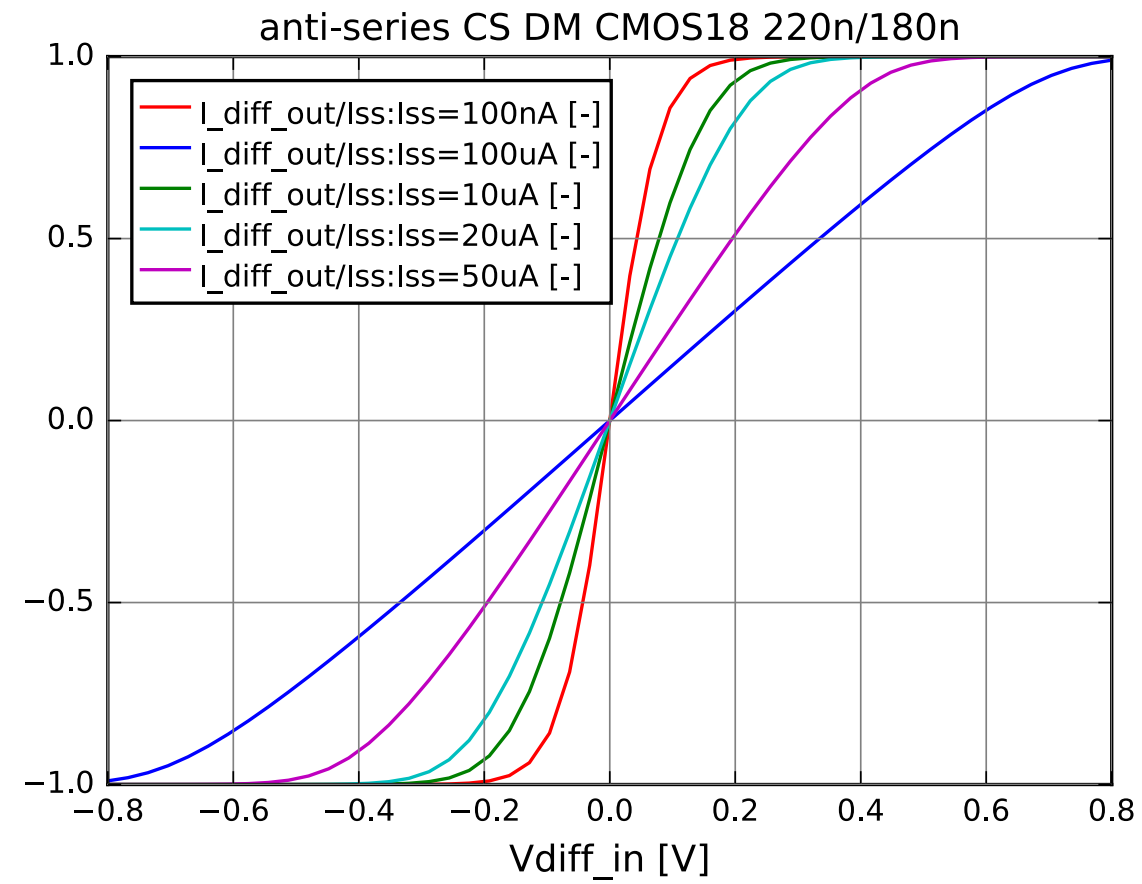


Common-mode voltages
fixed by V1 and V2

Differential pair V-I transfer

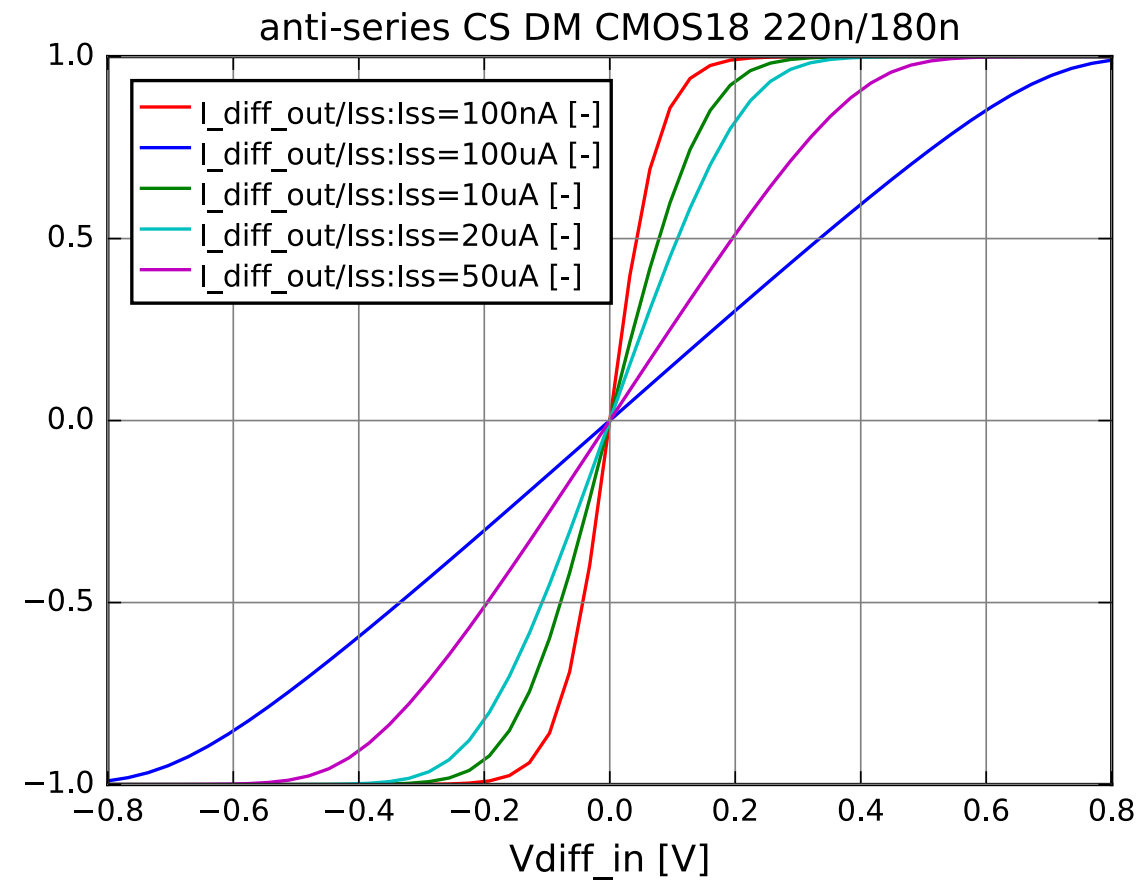
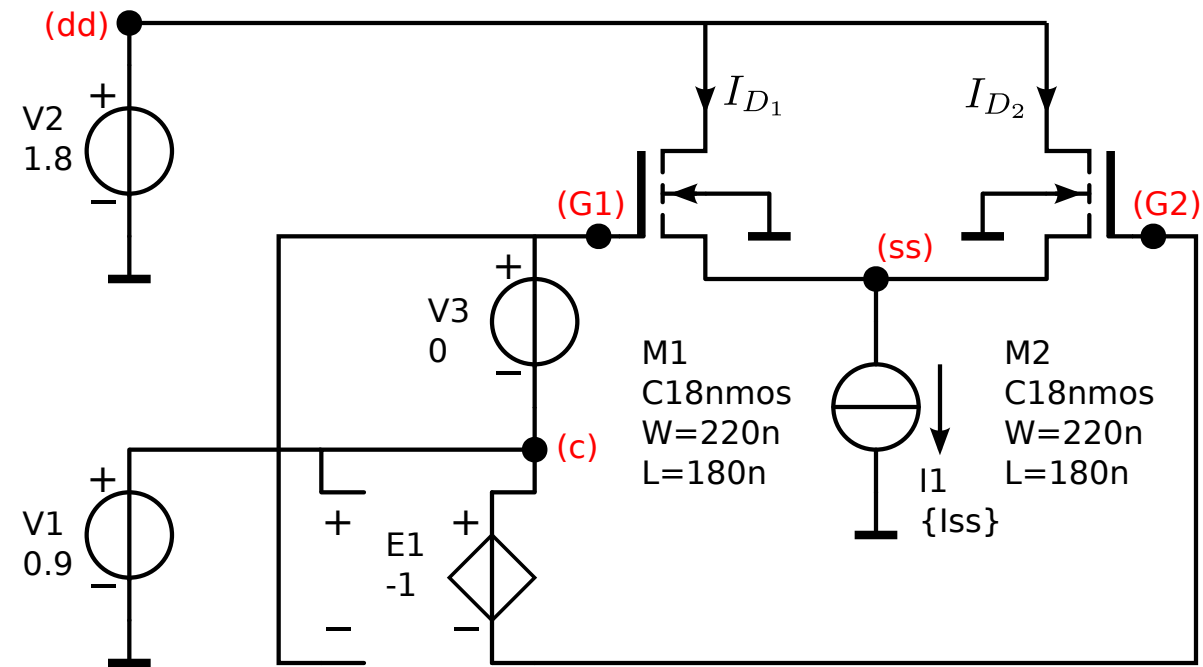


Common-mode voltages
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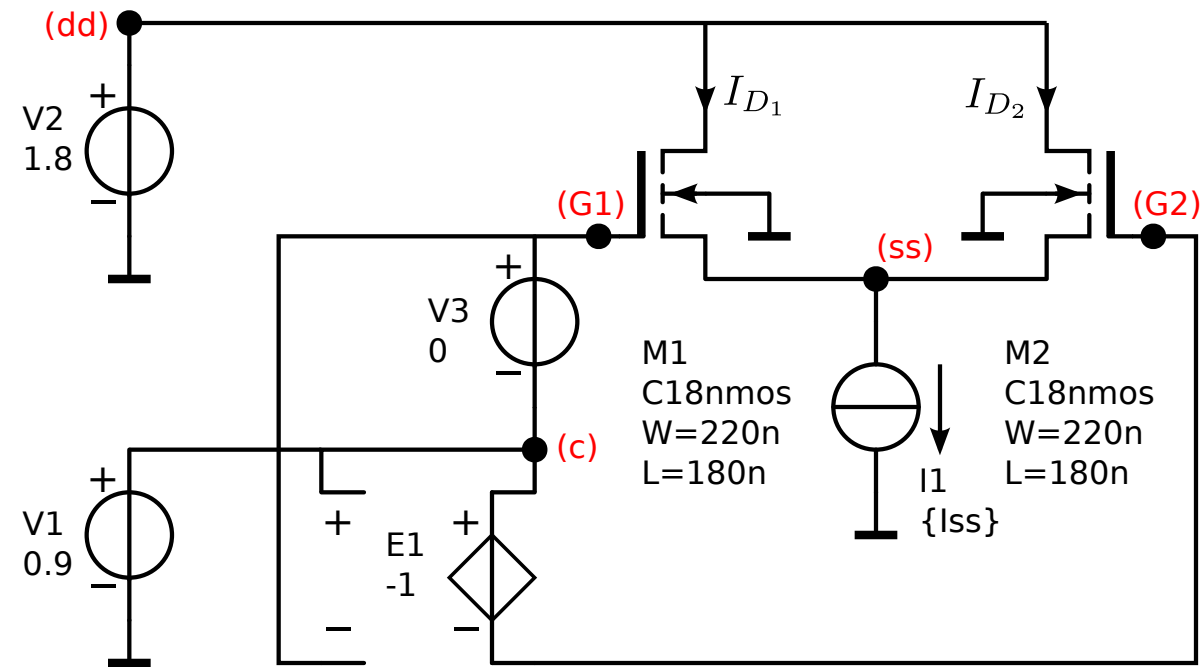
Relative differential
output current

Differential pair V-I transfer

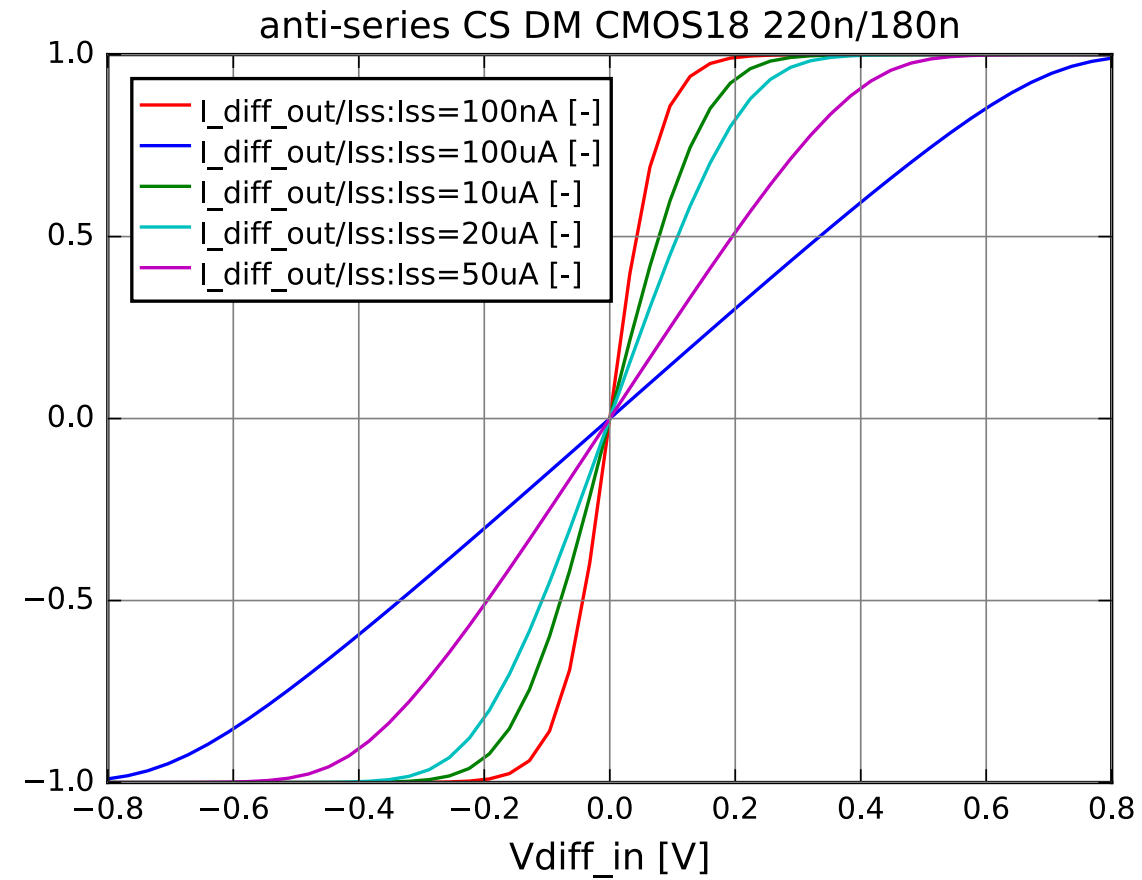


Odd characteristic

Differential pair V-I transfer



Common-mode voltages fixed by V1 and V2

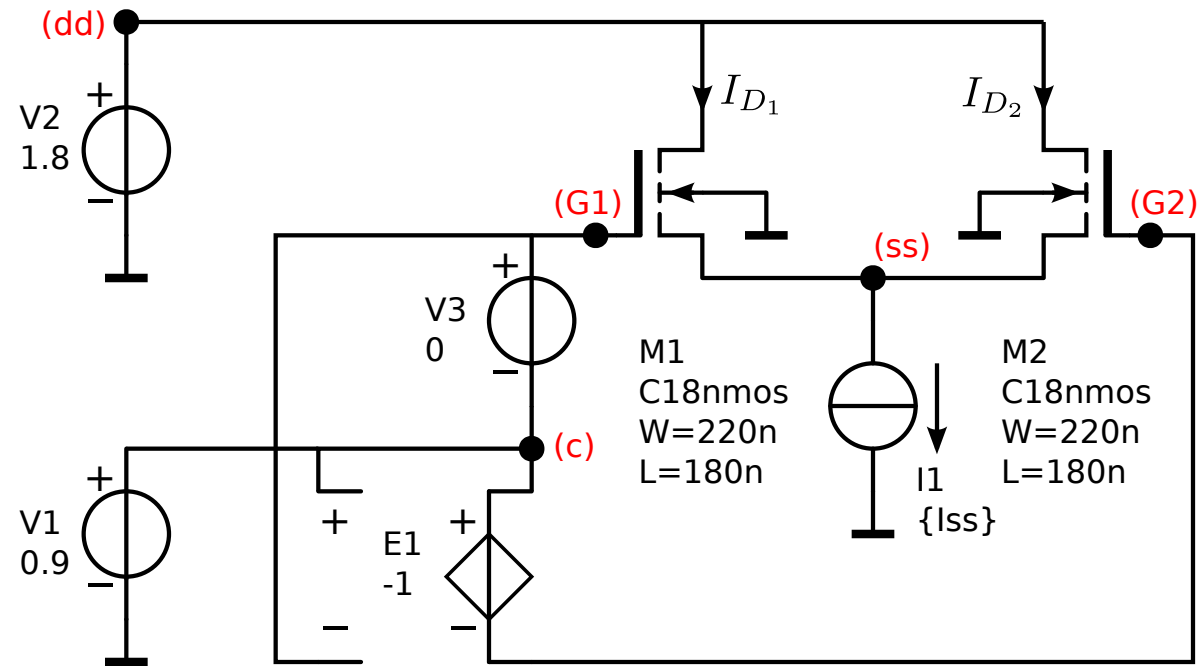


Relative differential output current

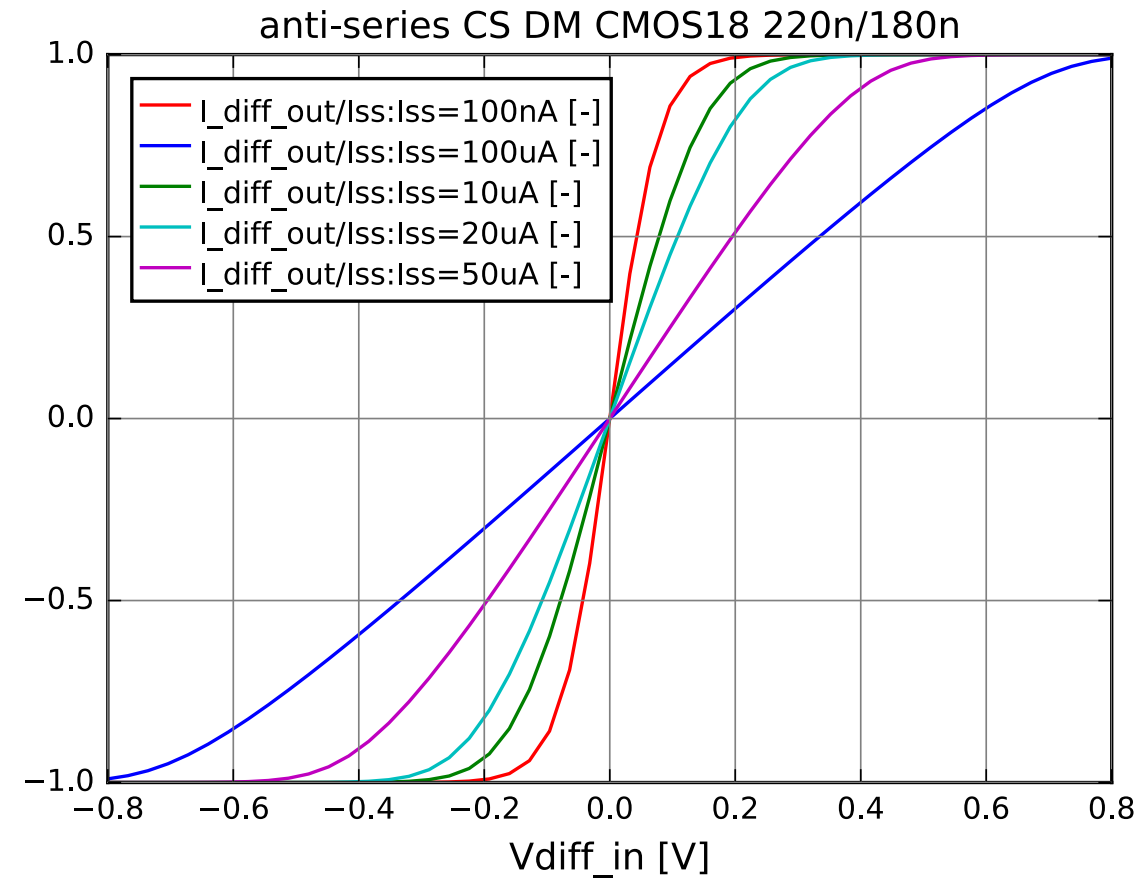
Odd characteristic

Increasing linearity with inversion coefficient

Differential pair V-I transfer



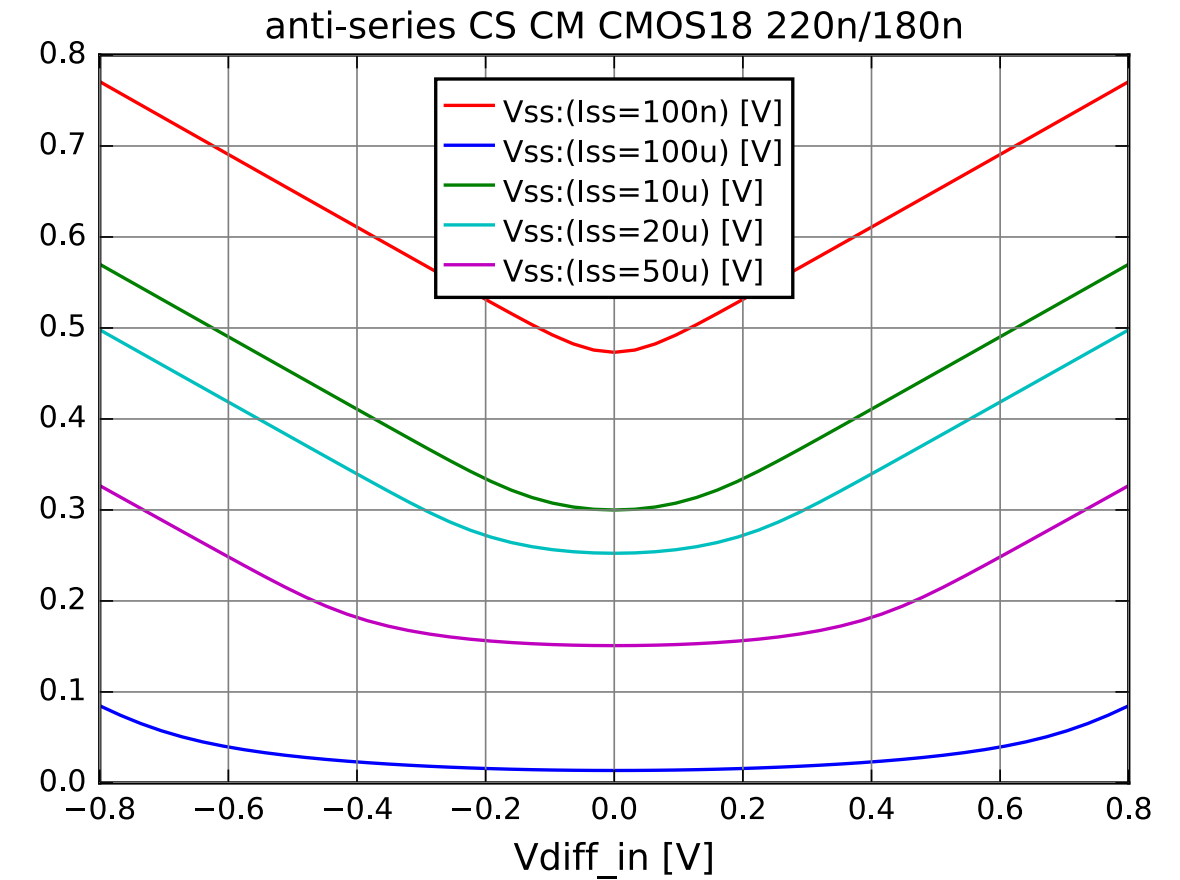
Common-mode voltages fixed by V1 and V2



Relative differential output current

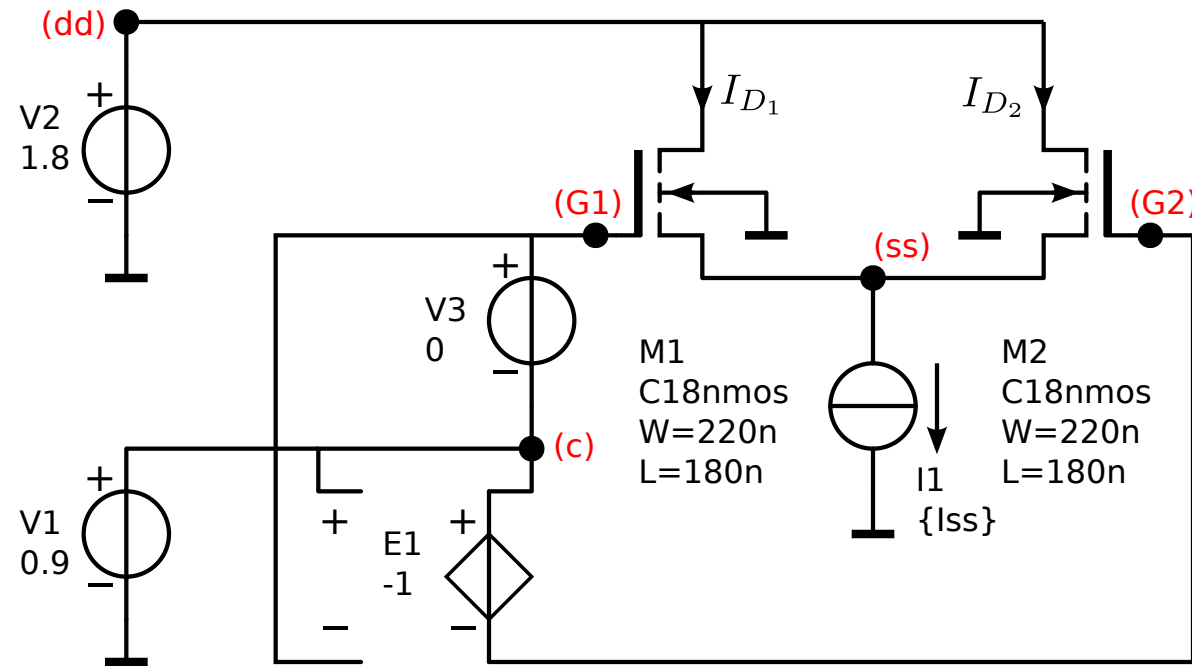
Odd characteristic

Increasing linearity with inversion coefficient

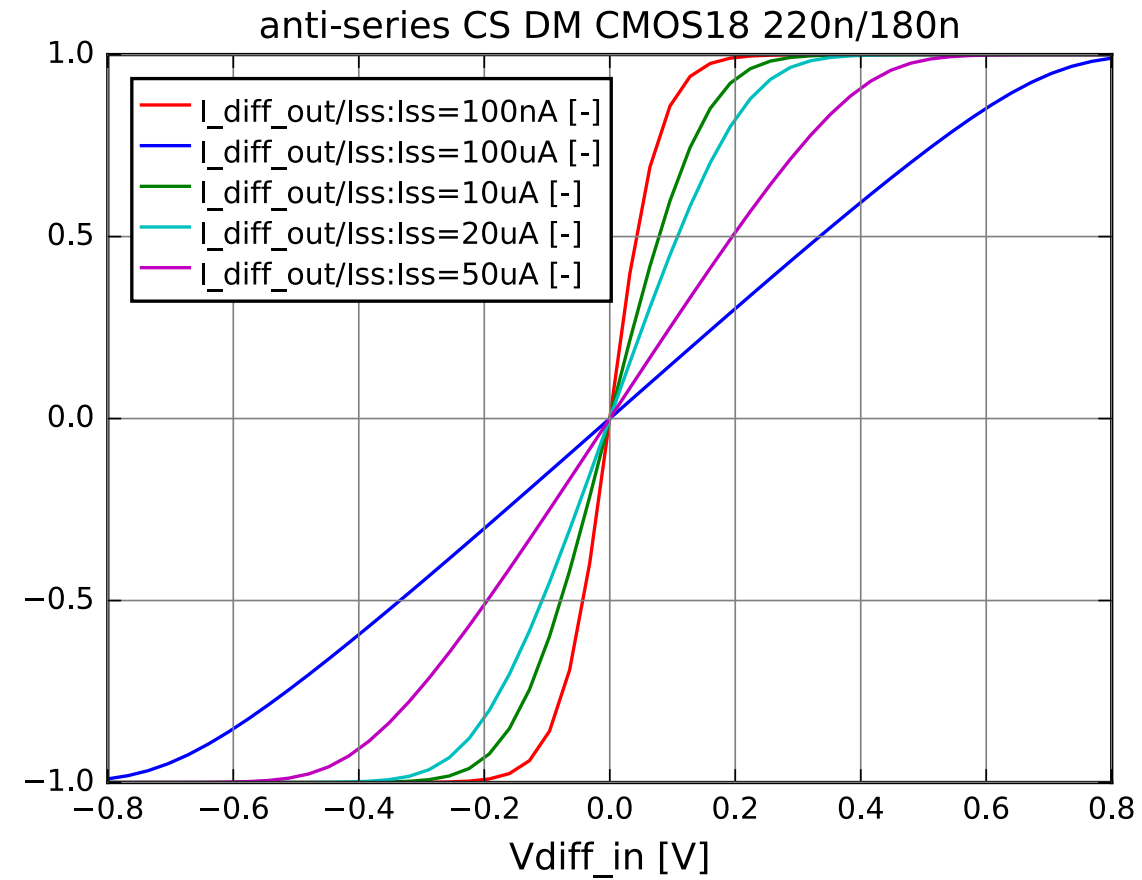


Common-mode source voltage

Differential pair V-I transfer



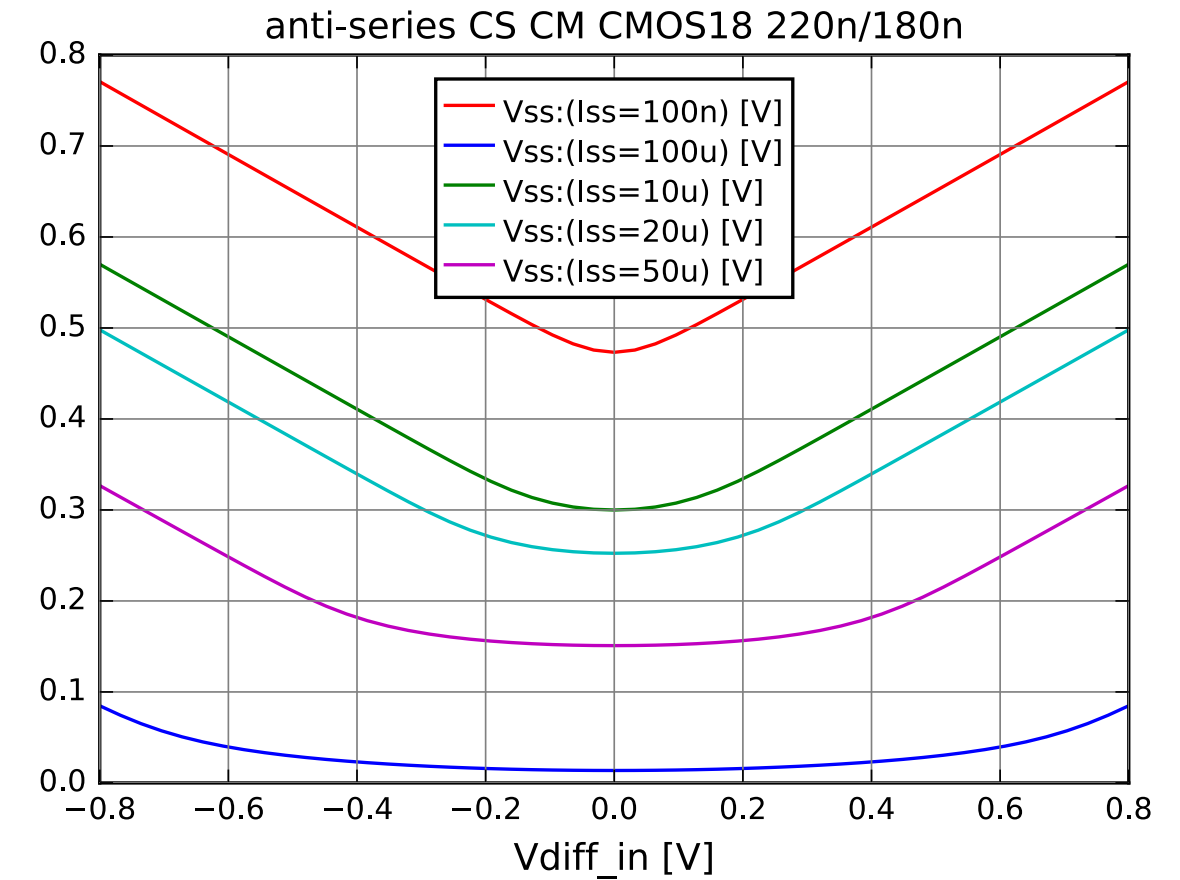
Common-mode voltages fixed by V1 and V2



Relative differential output current

Odd characteristic

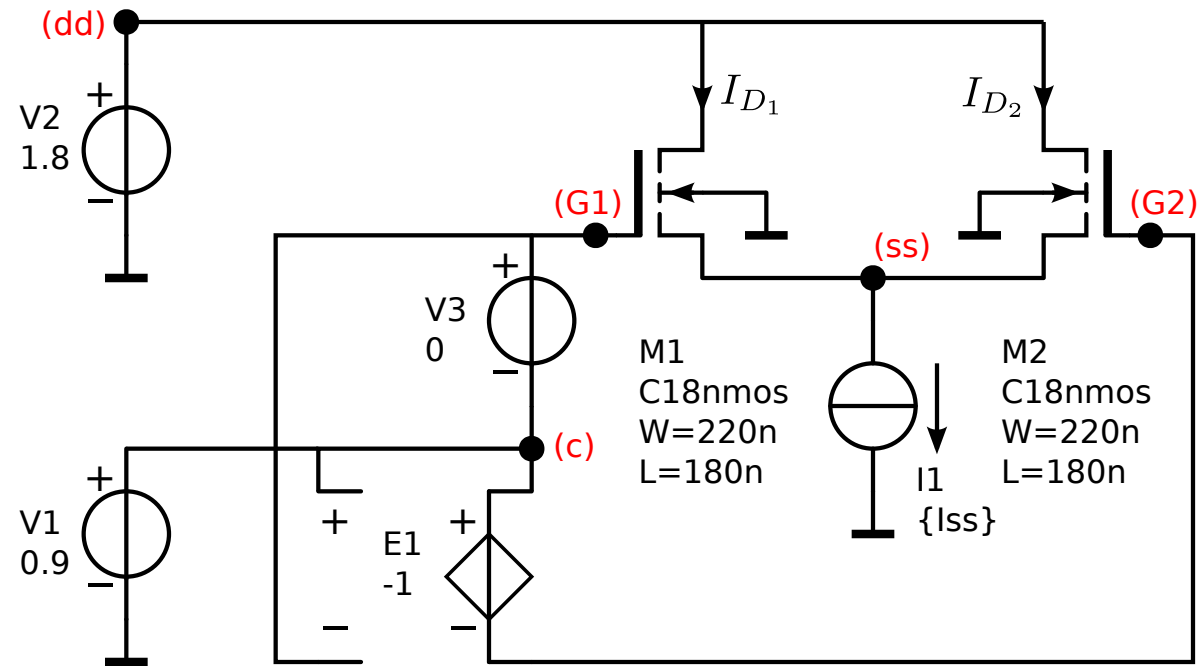
Increasing linearity with inversion coefficient



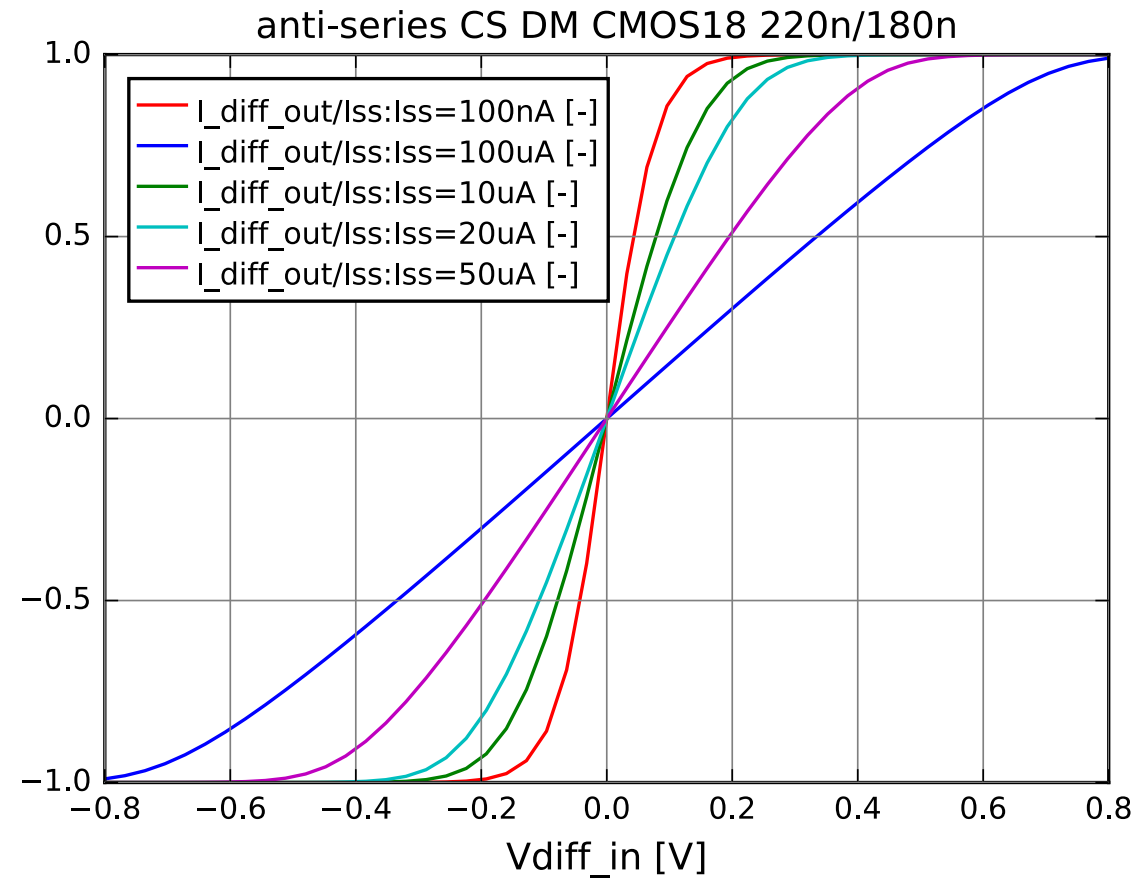
Common-mode source voltage

Even characteristic

Differential pair V-I transfer



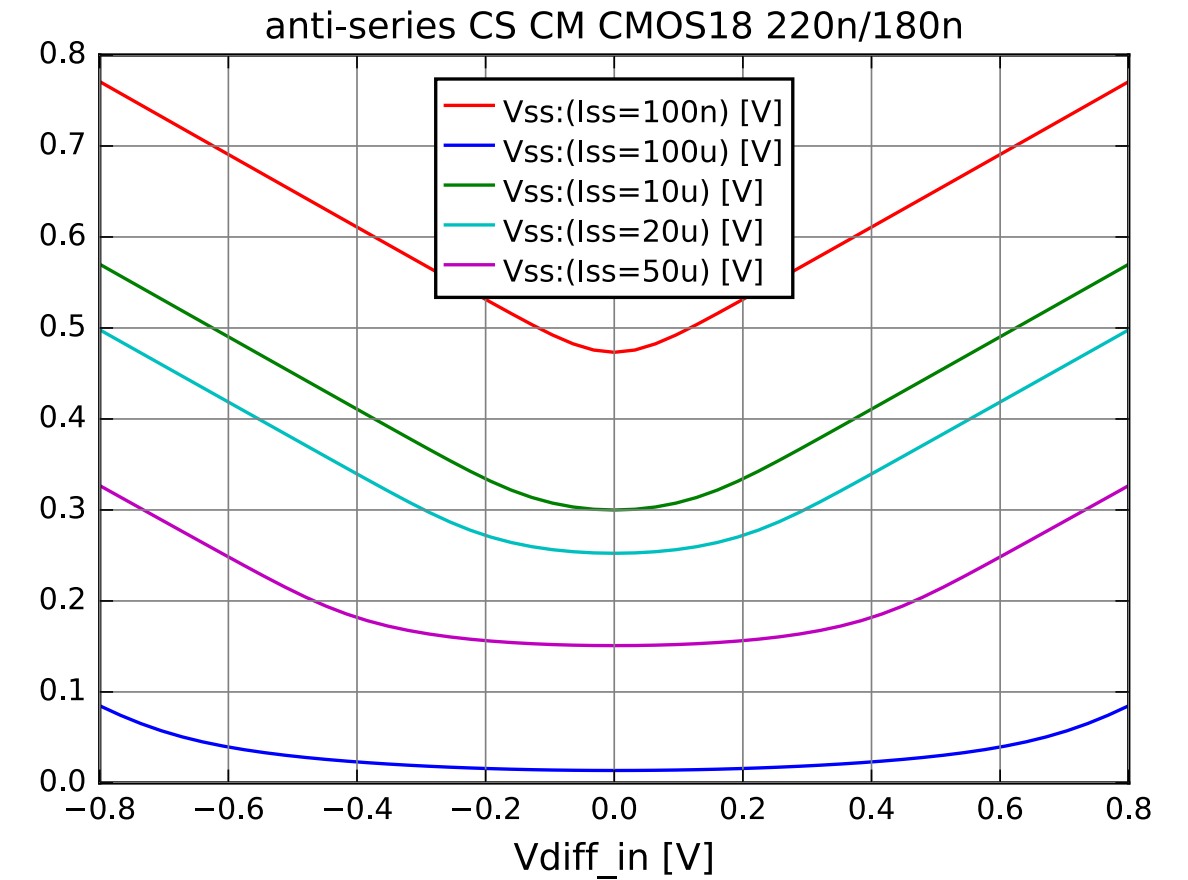
Common-mode voltages fixed by V1 and V2



Relative differential output current

Odd characteristic

Increasing linearity with inversion coefficient



Common-mode source voltage

Even characteristic

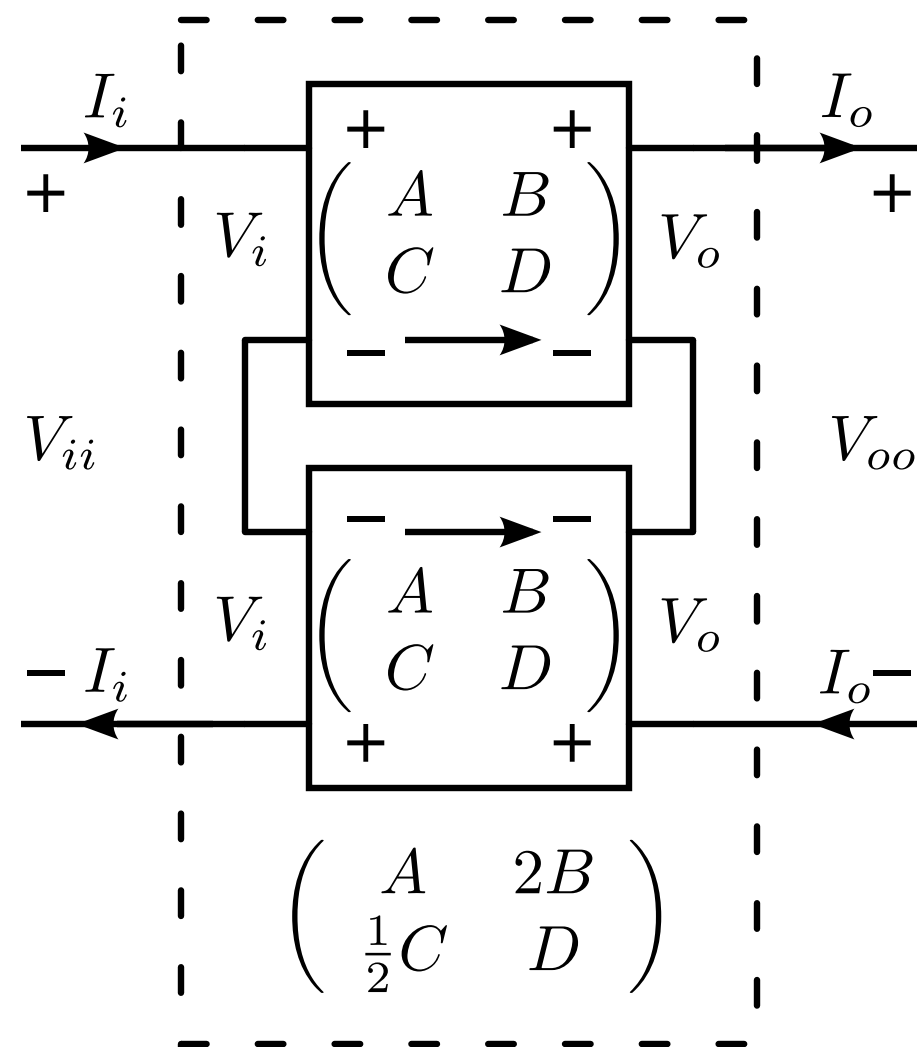
Differential pair small-signal transfer

Differential pair small-signal transfer

Behavioral modifications
resulting from (anti)-
series connection of linear
two-ports

Differential pair small-signal transfer

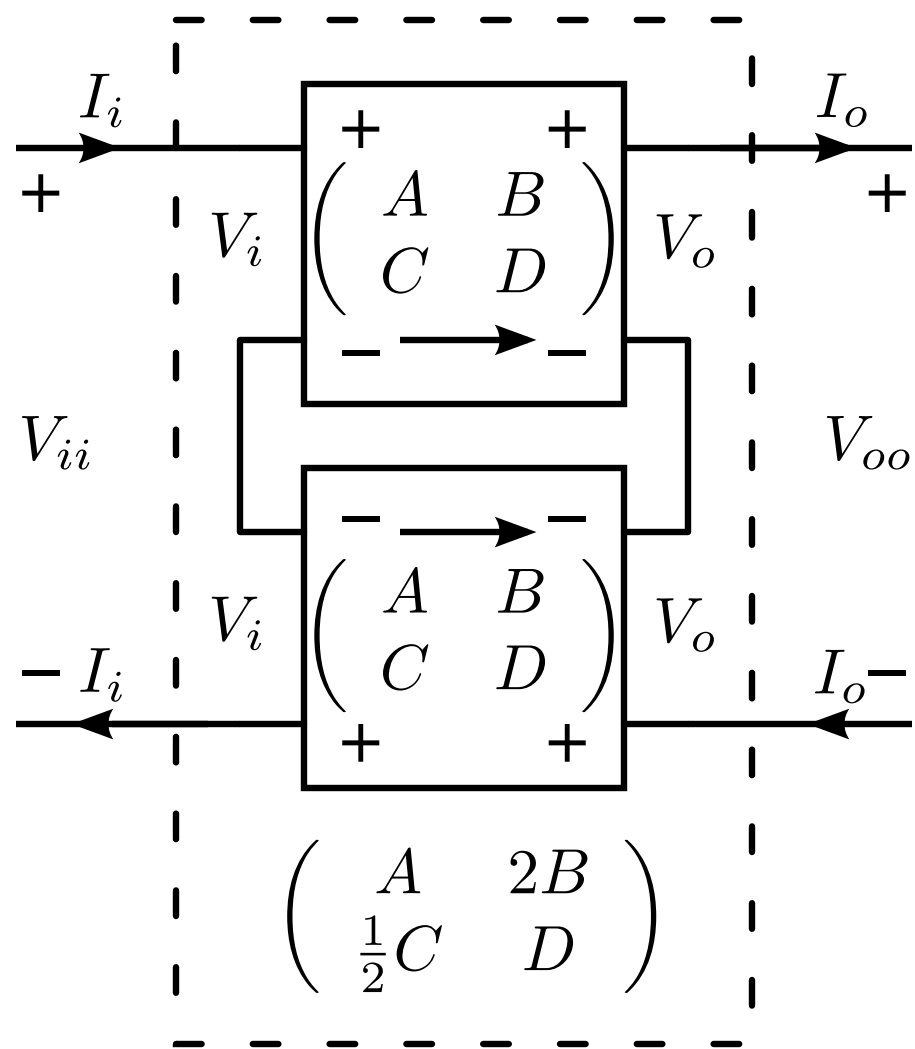
Behavioral modifications
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Differential pair small-signal transfer

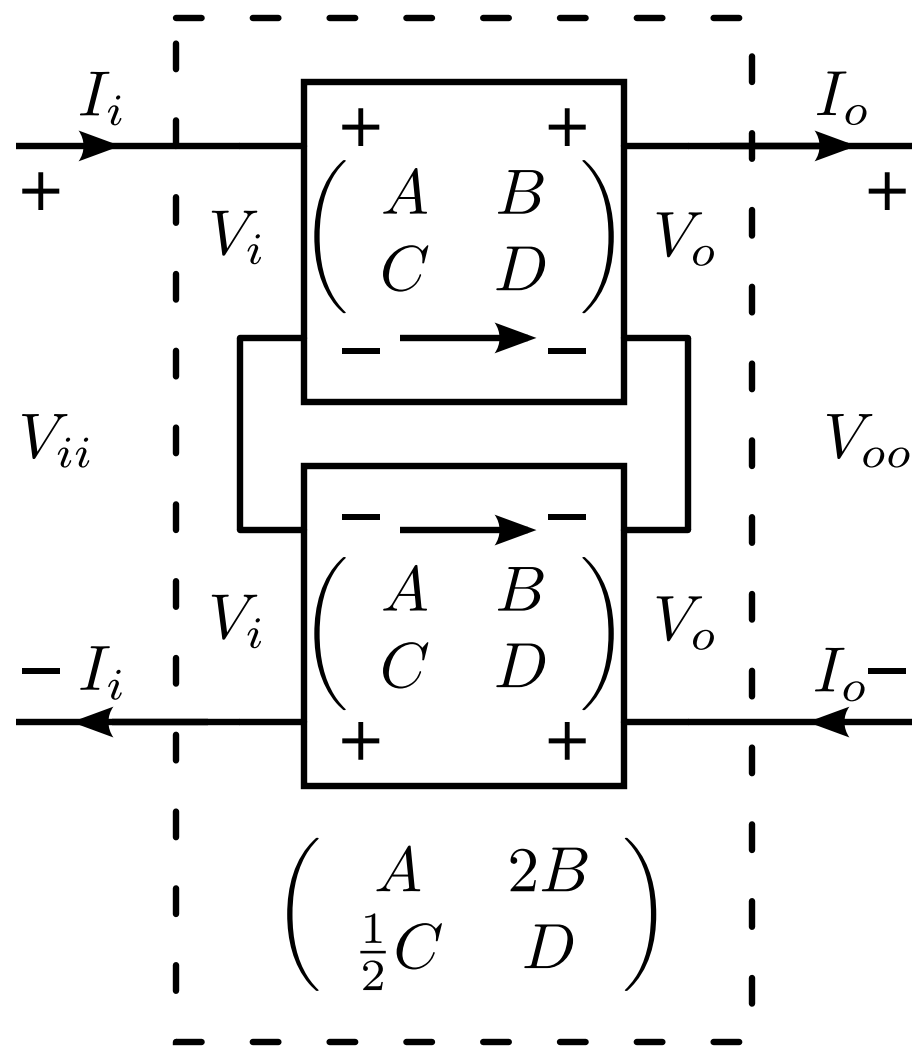
Behavioral modifications
resulting from (anti)-
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two-ports

Small-signal diagram
differential pair

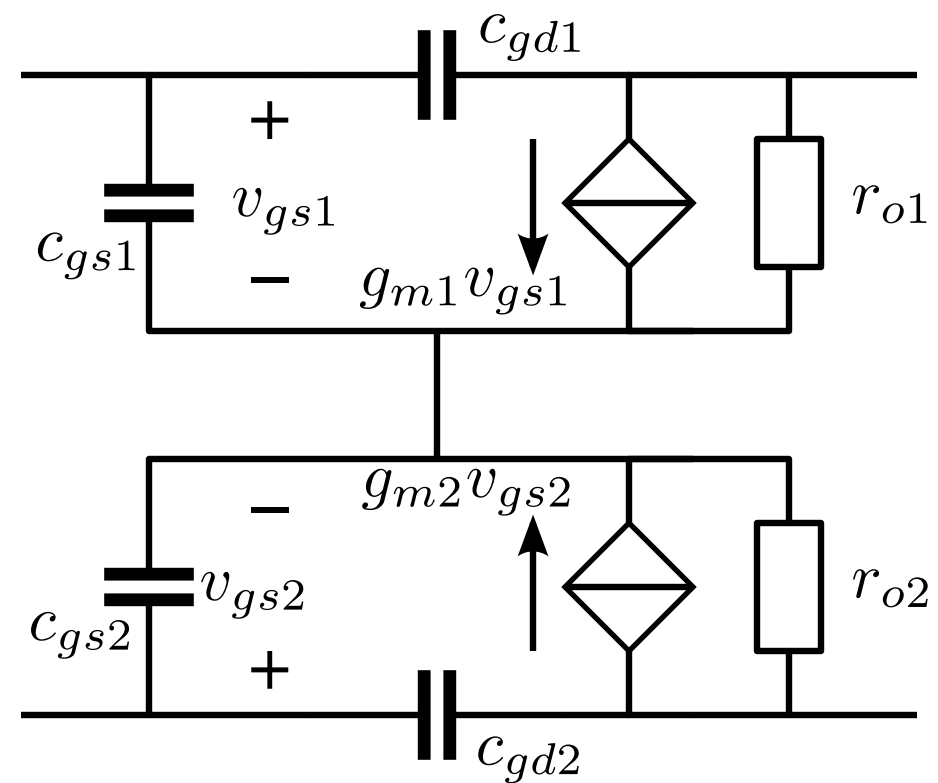


Differential pair small-signal transfer

Behavioral modifications
resulting from (anti)-
series connection of linear
two-ports

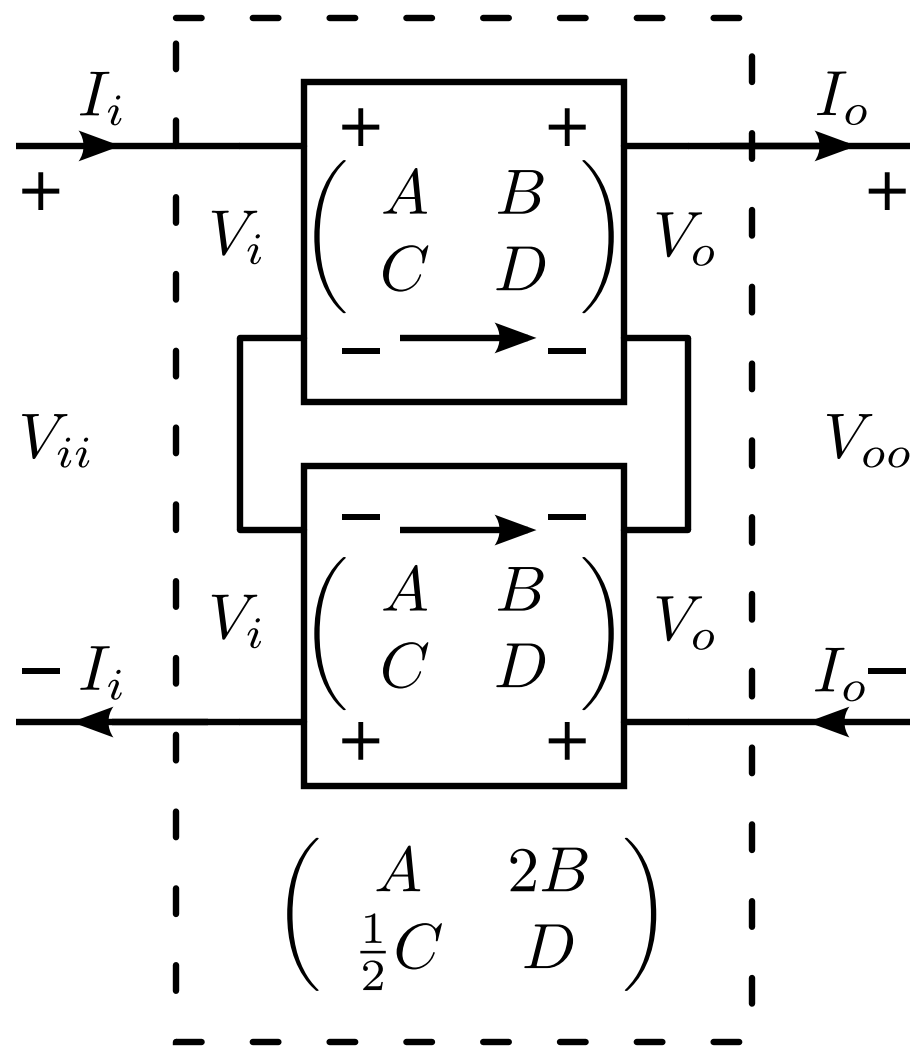


Small-signal diagram
differential pair

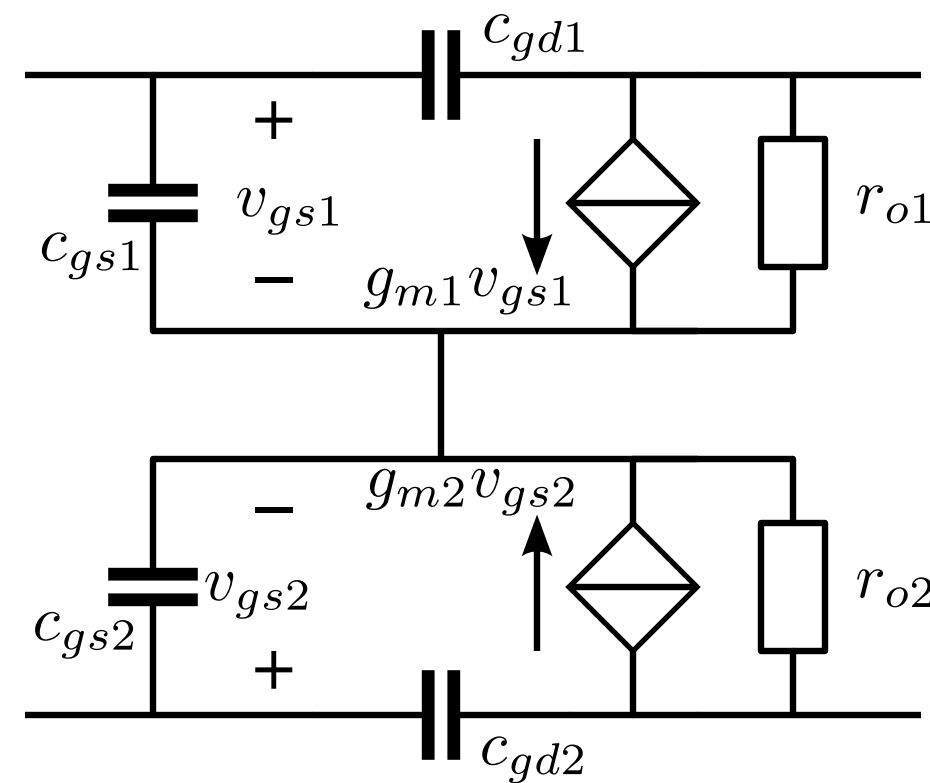


Differential pair small-signal transfer

Behavioral modifications
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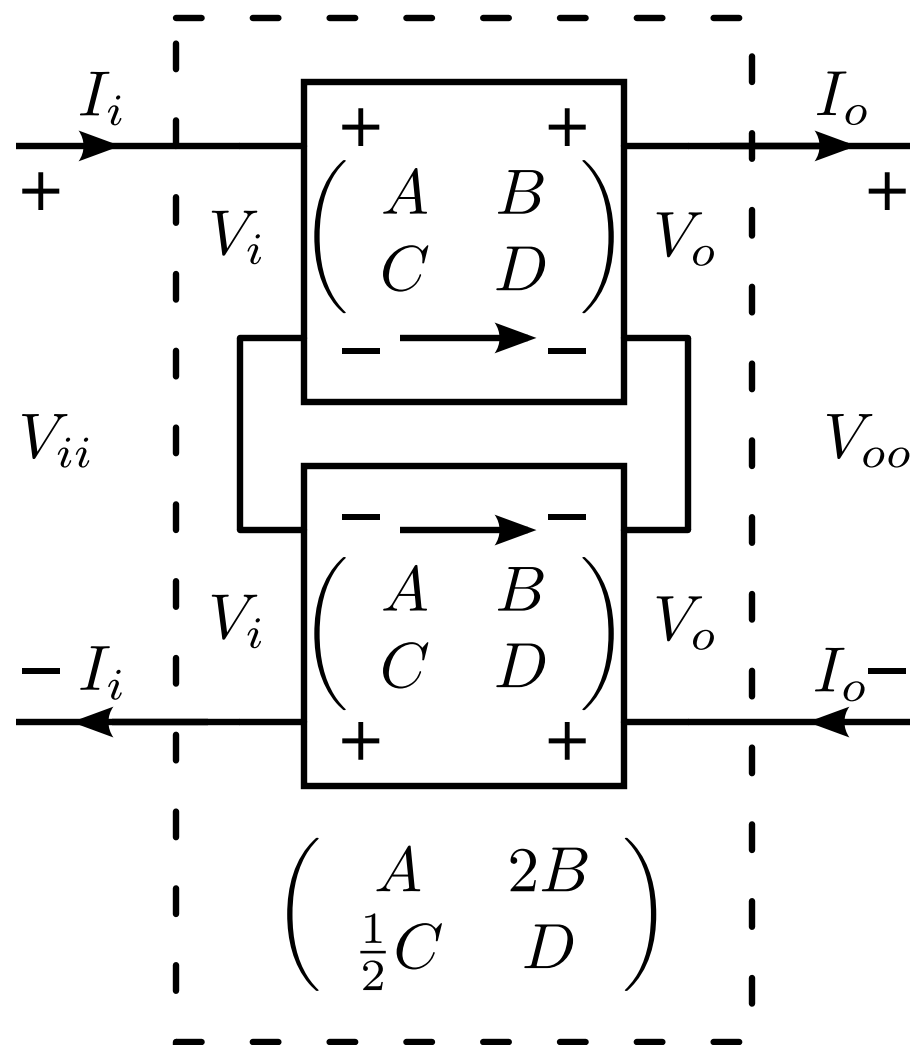
Small-signal diagram
differential pair



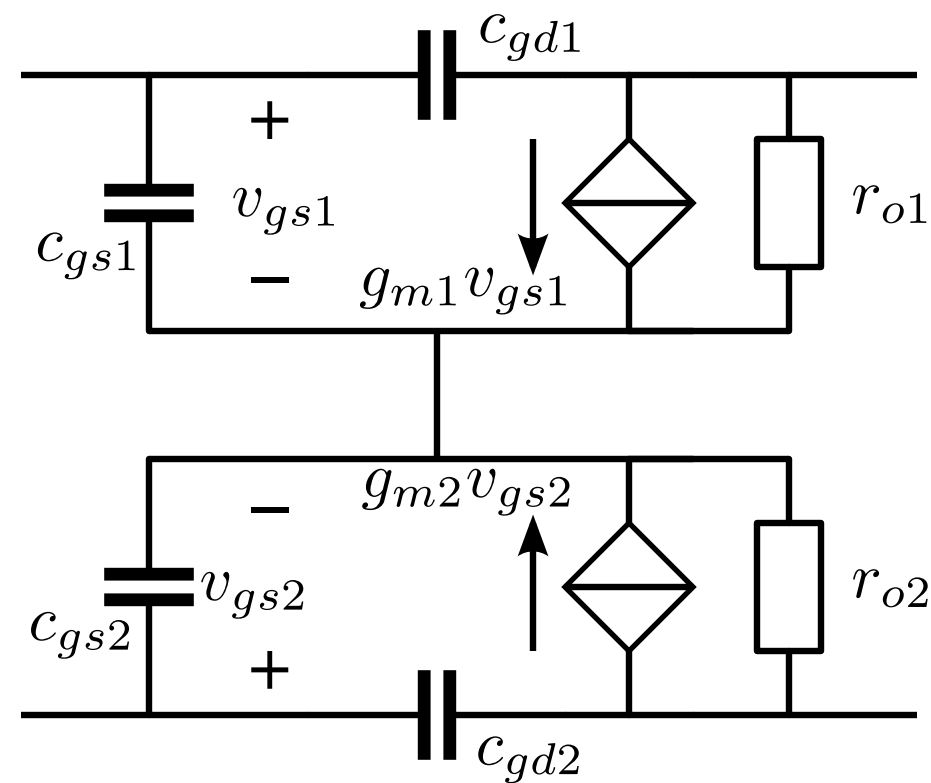
Equivalent small-signal diagram
in quiescent operating point

Differential pair small-signal transfer

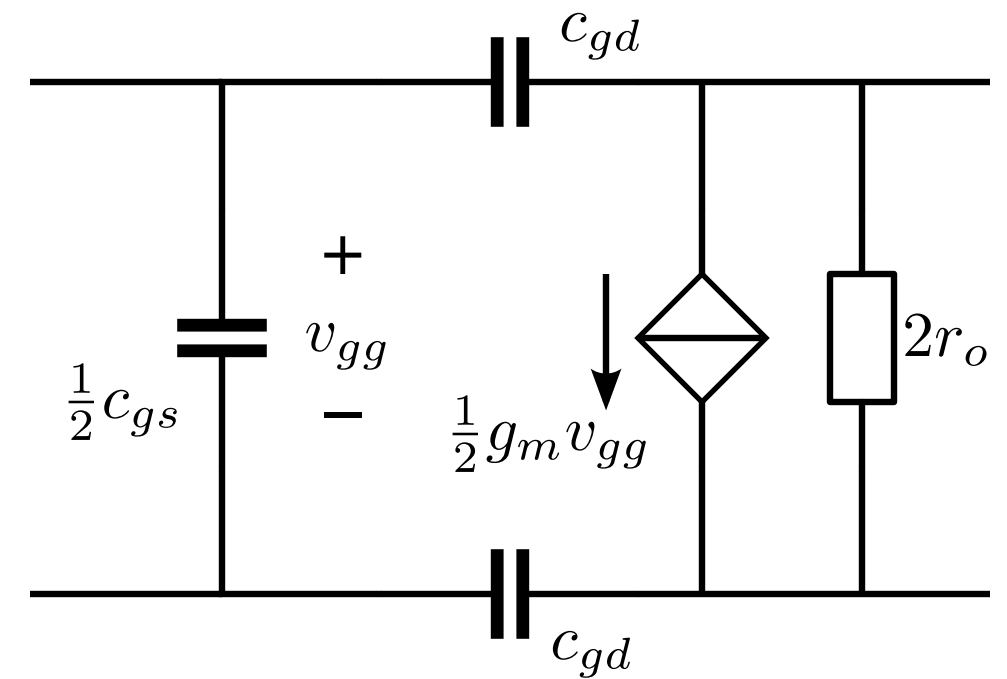
Behavioral modifications
resulting from (anti)-
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Small-signal diagram
differential pair

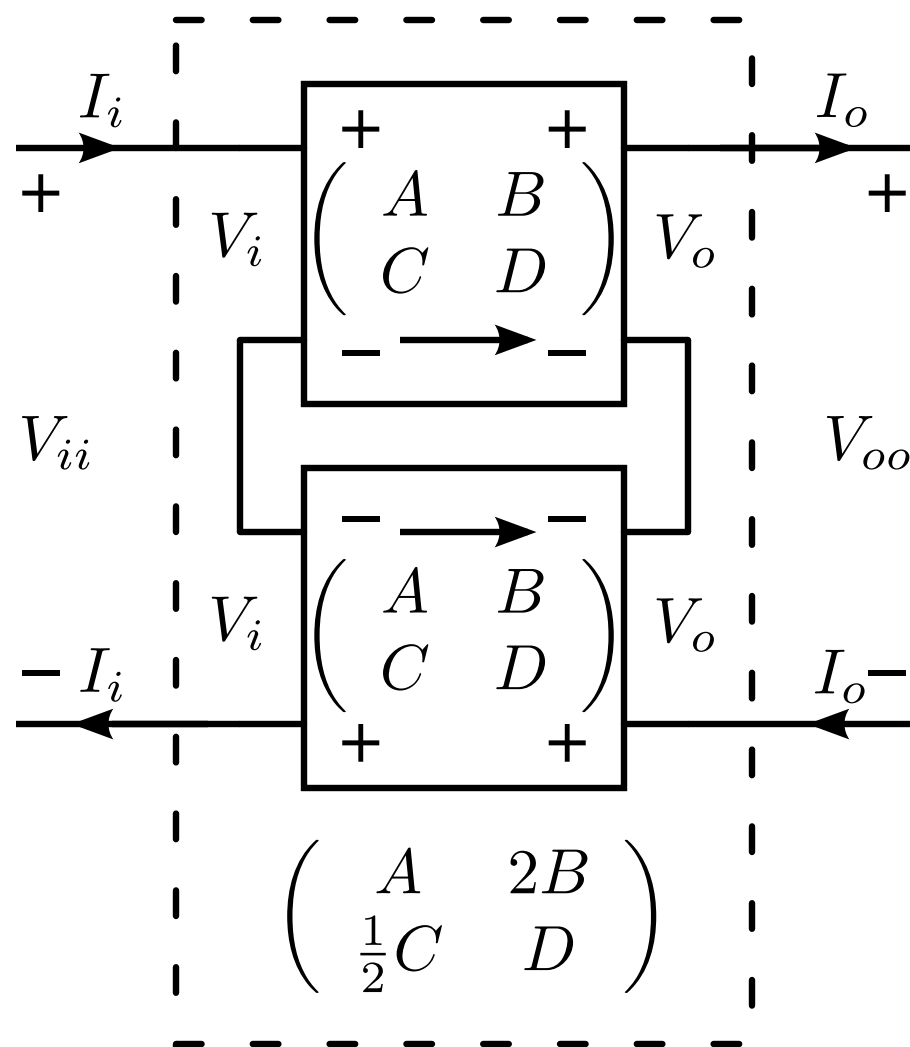


Equivalent small-signal diagram
in quiescent operating point

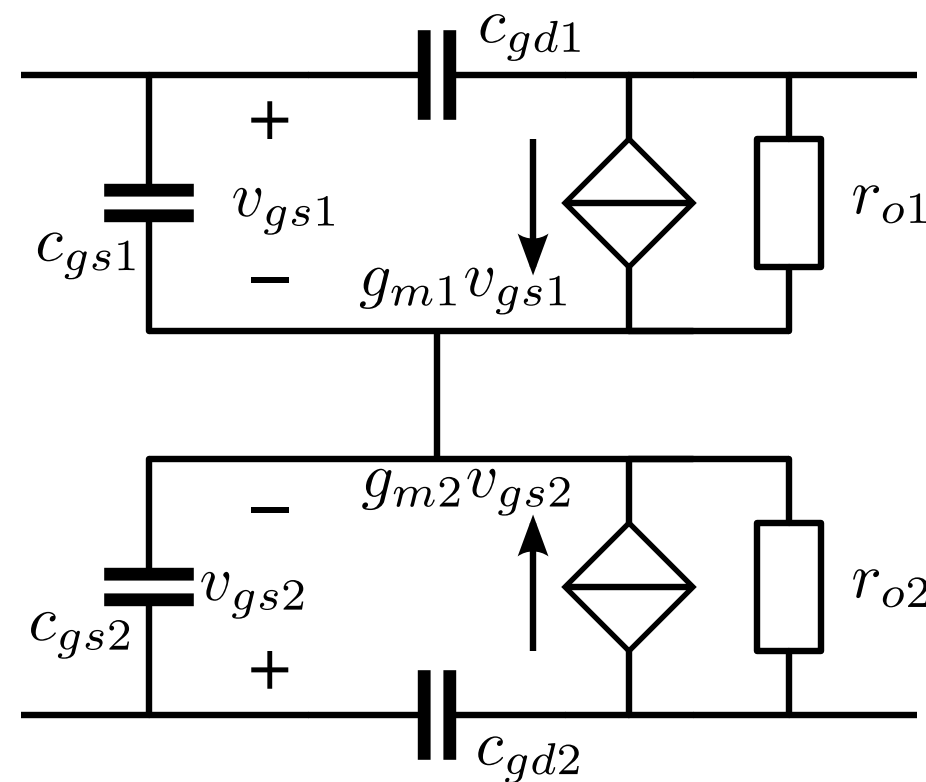


Differential pair small-signal transfer

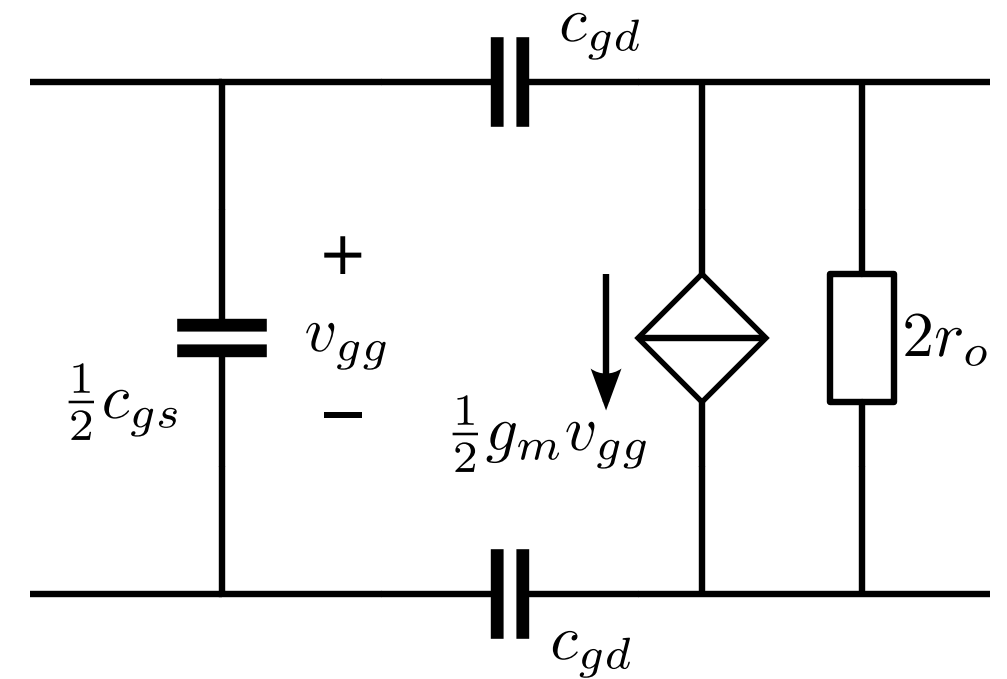
Behavioral modifications resulting from (anti)-series connection of linear two-ports



Small-signal diagram differential pair



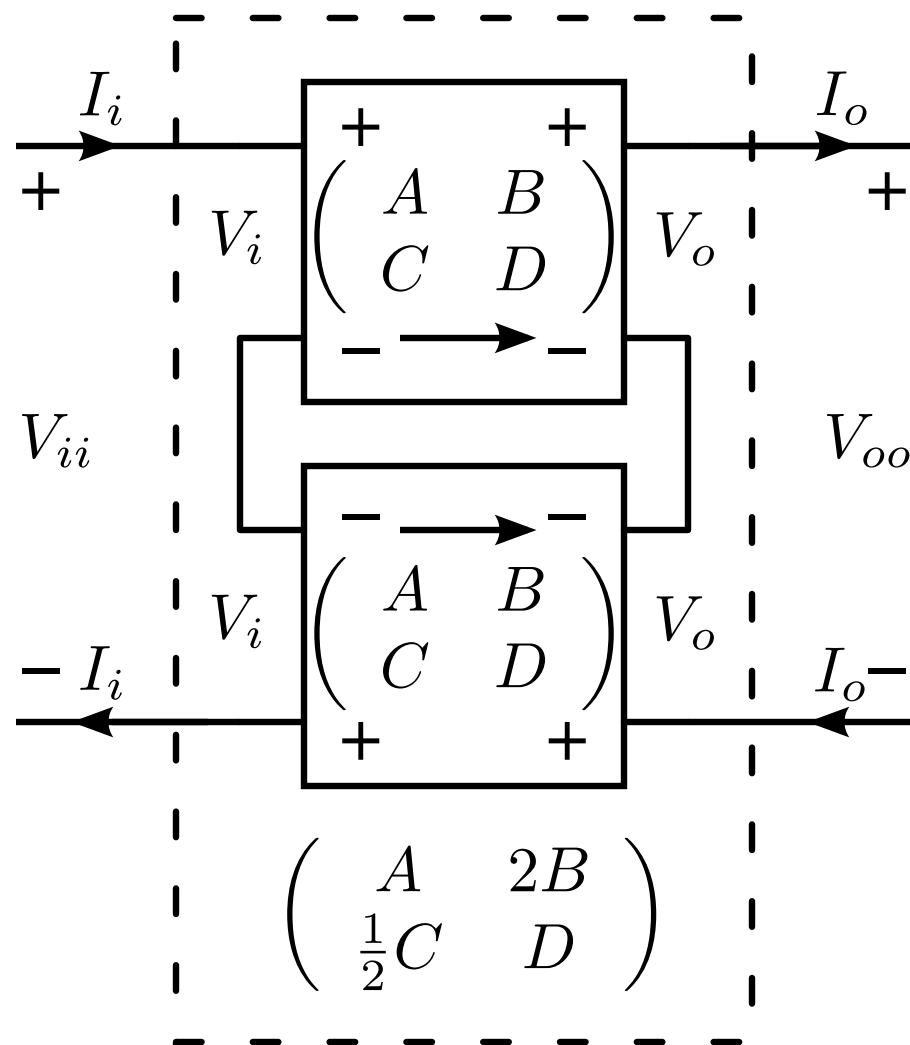
Equivalent small-signal diagram in quiescent operating point



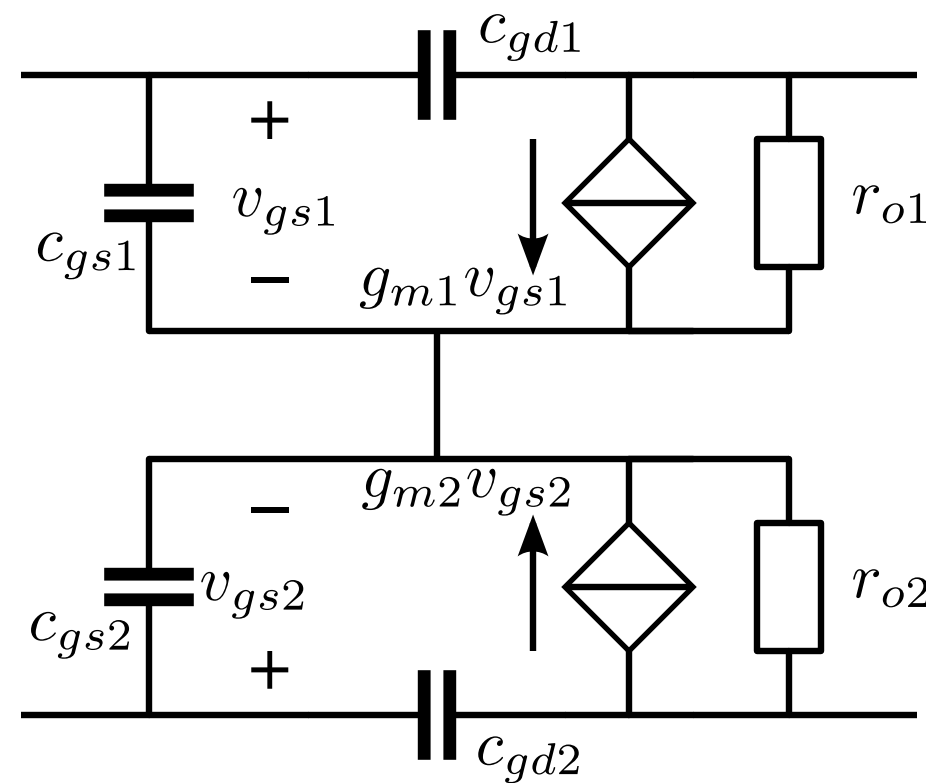
C_{gs} , C_{gd} , g_m and r_o are the small-signal parameters of the CS stage.

Differential pair small-signal transfer

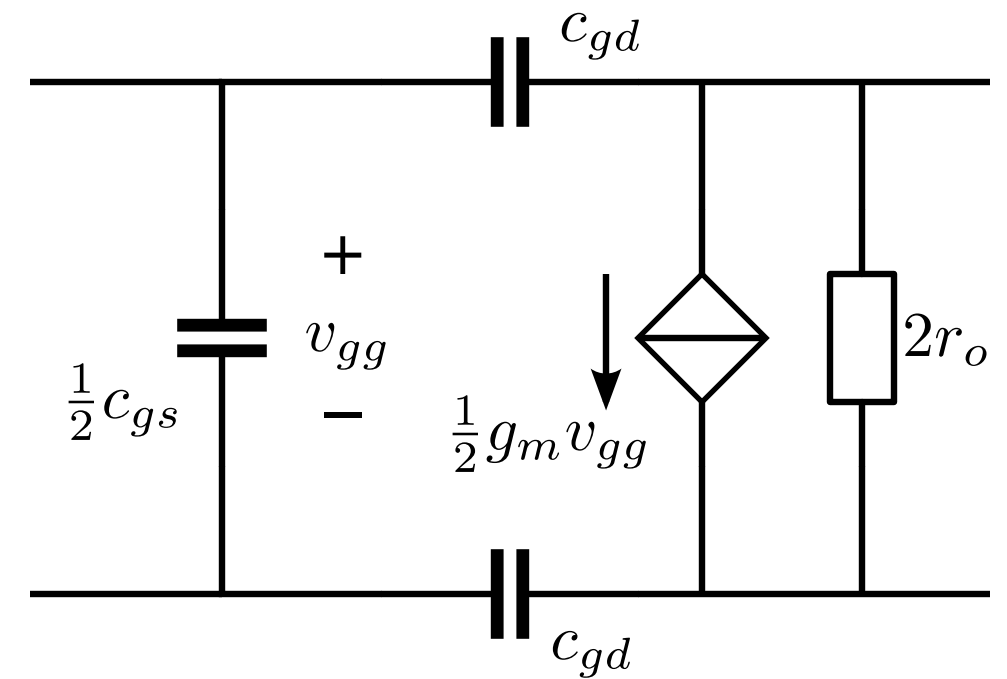
Behavioral modifications resulting from (anti)-series connection of linear two-ports



Small-signal diagram differential pair



Equivalent small-signal diagram in quiescent operating point



C_{gs} , C_{gd} , g_m and r_o are the small-signal parameters of the CS stage.

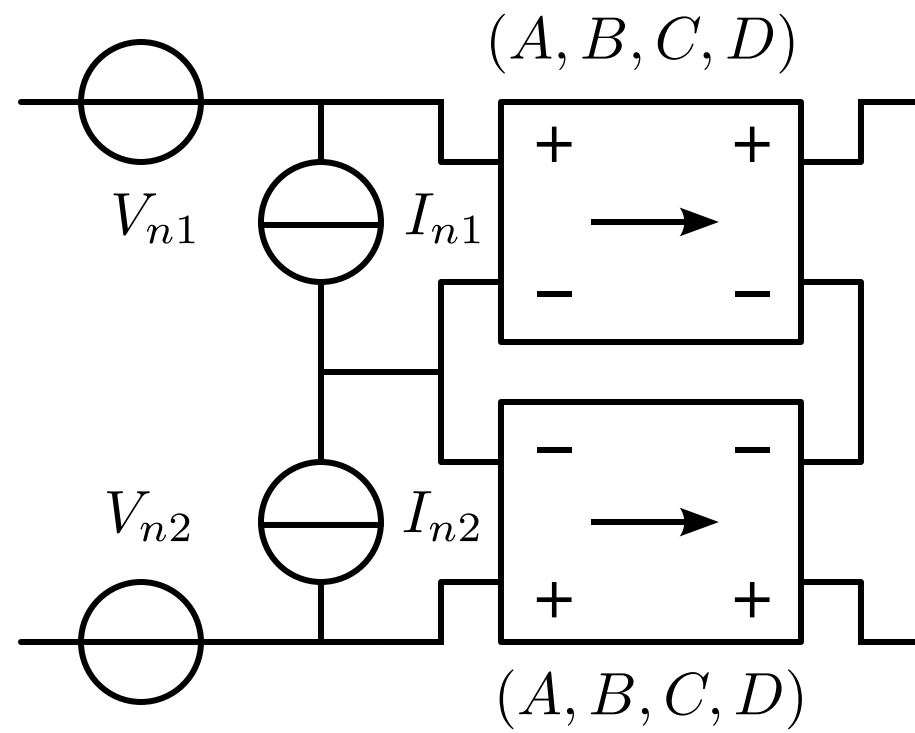
Differential pair stationary noise

Differential pair stationary noise

Behavioral modifications resulting from (anti)-series connection of linear two-ports

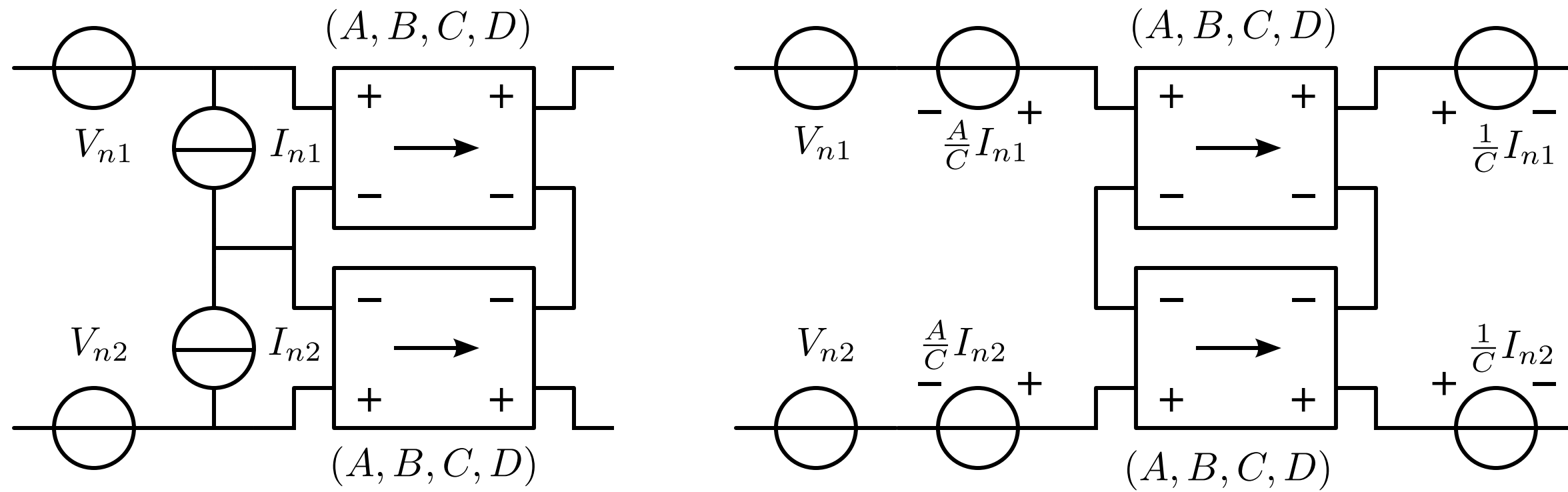
Differential pair stationary noise

Behavioral modifications resulting from (anti)-series connection of linear two-ports



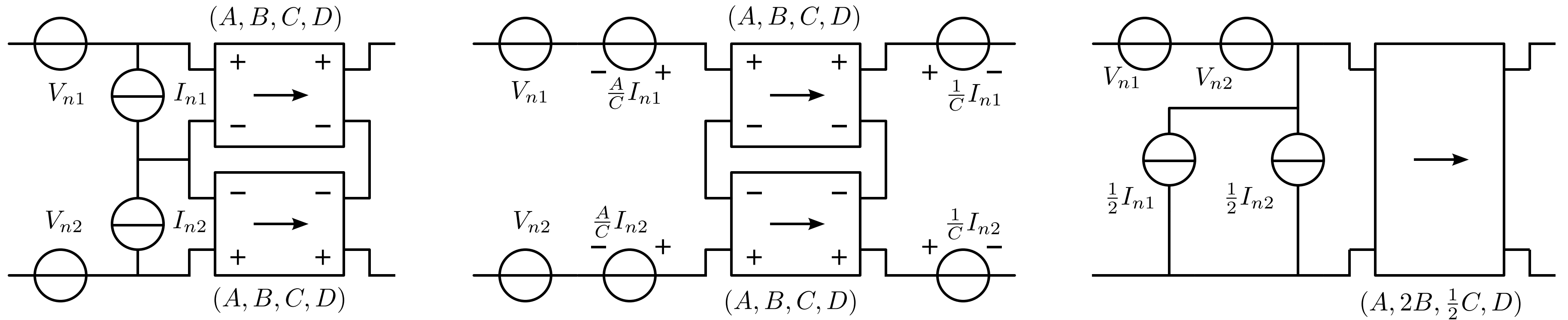
Differential pair stationary noise

Behavioral modifications resulting from (anti)-series connection of linear two-ports



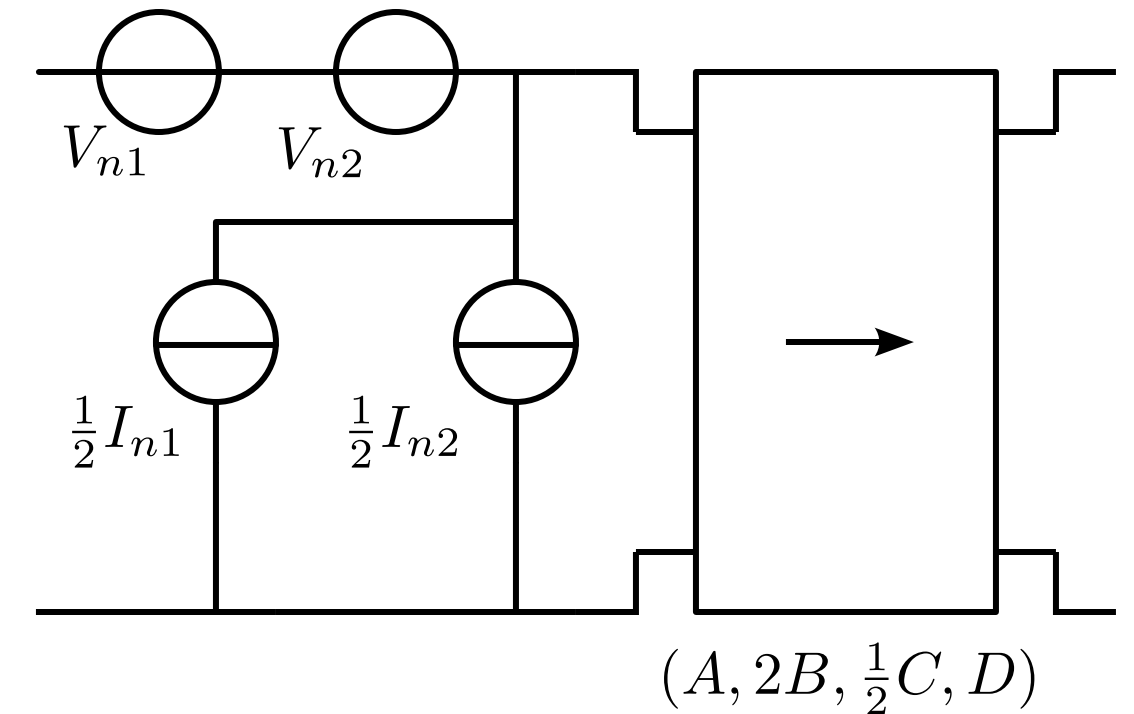
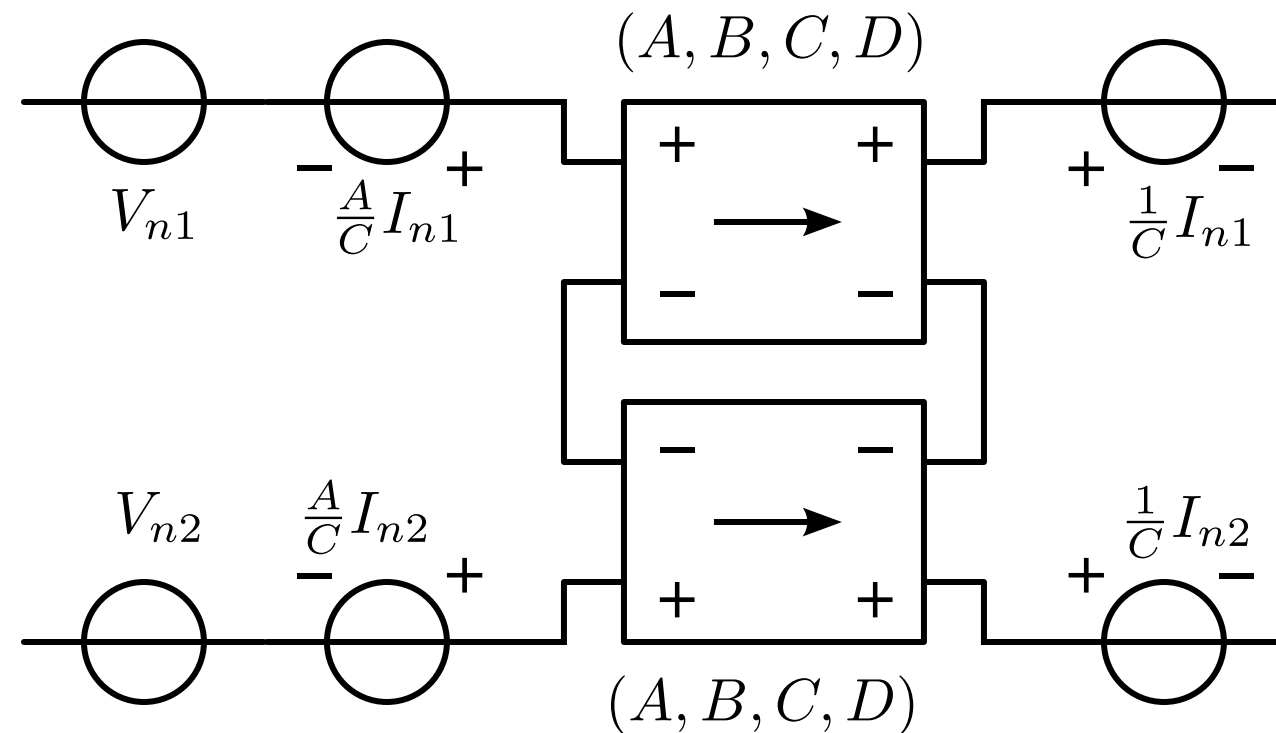
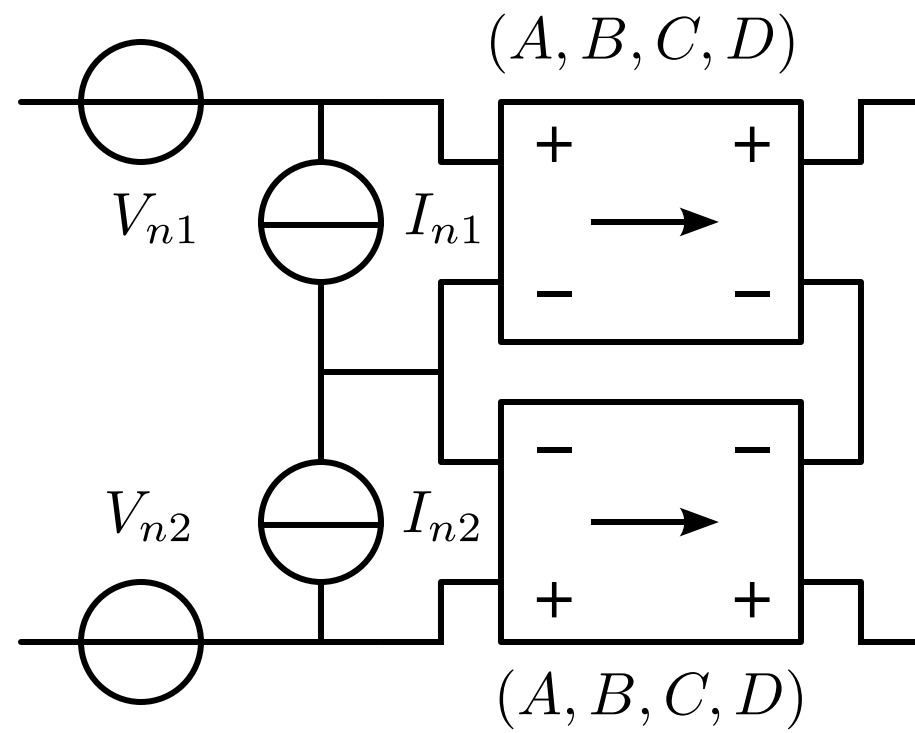
Differential pair stationary noise

Behavioral modifications resulting from (anti)-series connection of linear two-ports



Differential pair stationary noise

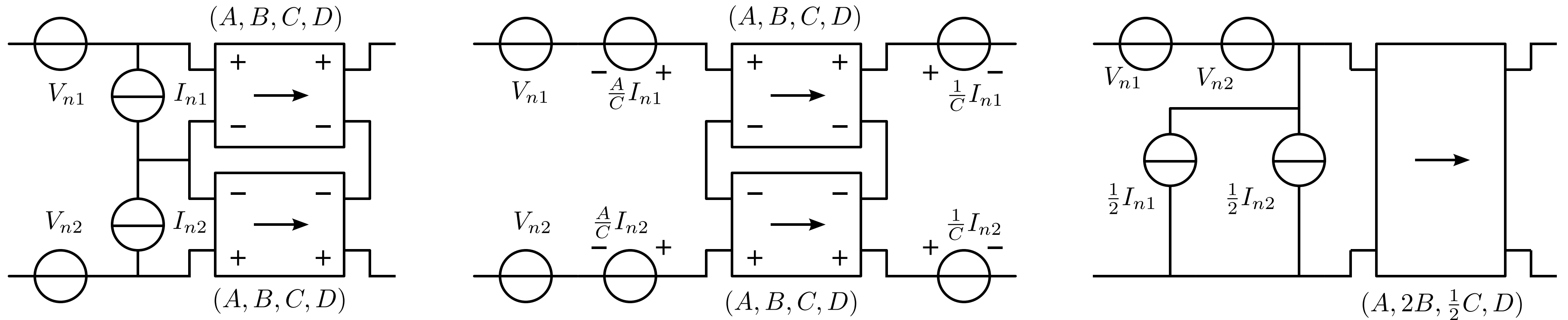
Behavioral modifications resulting from (anti)-series connection of linear two-ports



Result:

Differential pair stationary noise

Behavioral modifications resulting from (anti)-series connection of linear two-ports

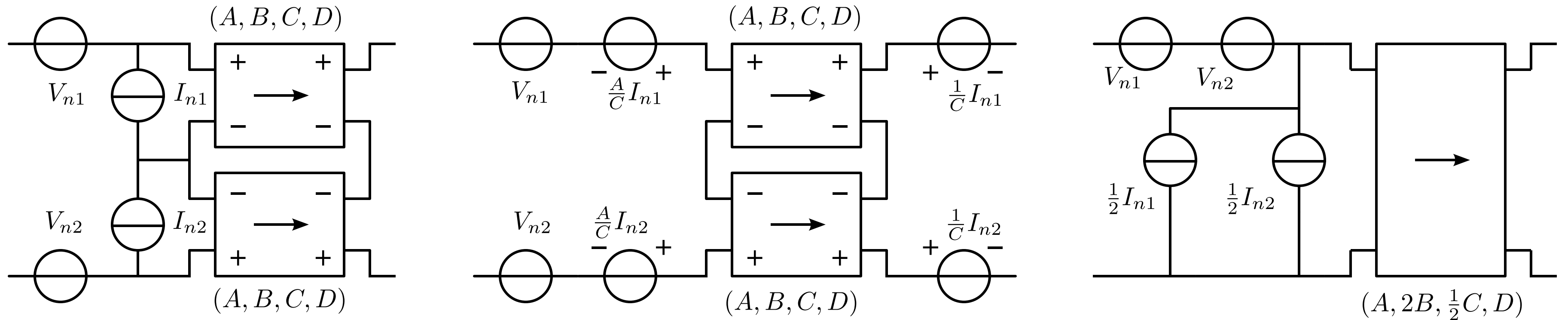


Result:

$$S_v = S_{V_{n1}} + S_{V_{n2}}$$

Differential pair stationary noise

Behavioral modifications resulting from (anti)-series connection of linear two-ports



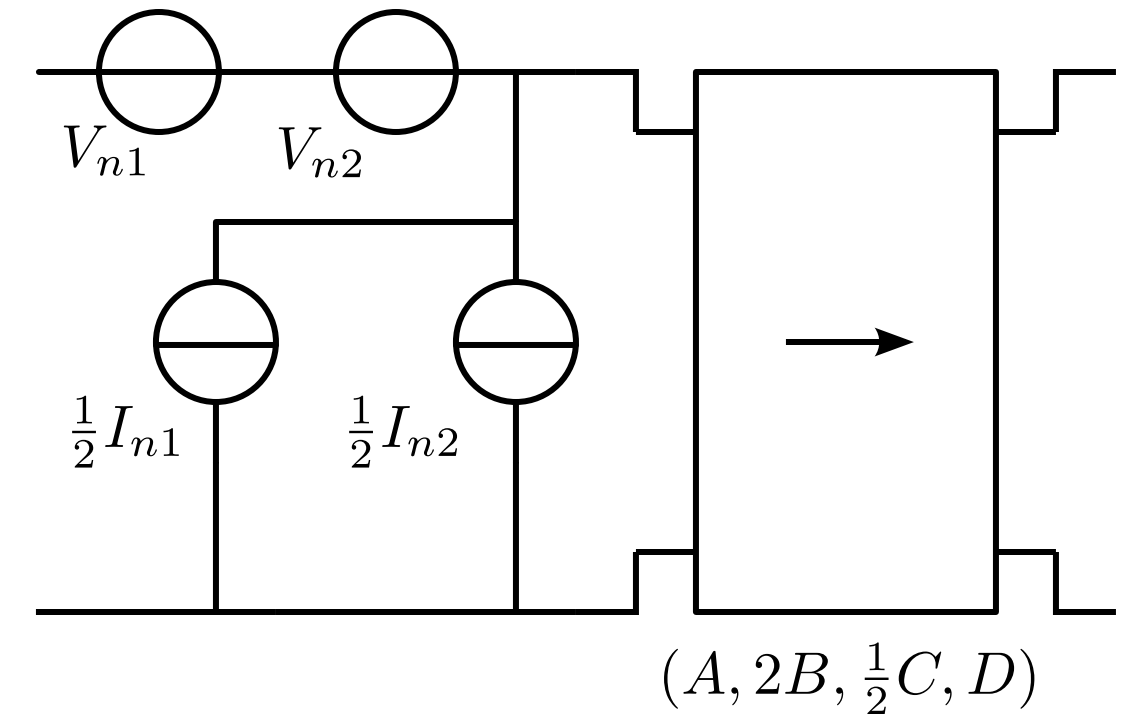
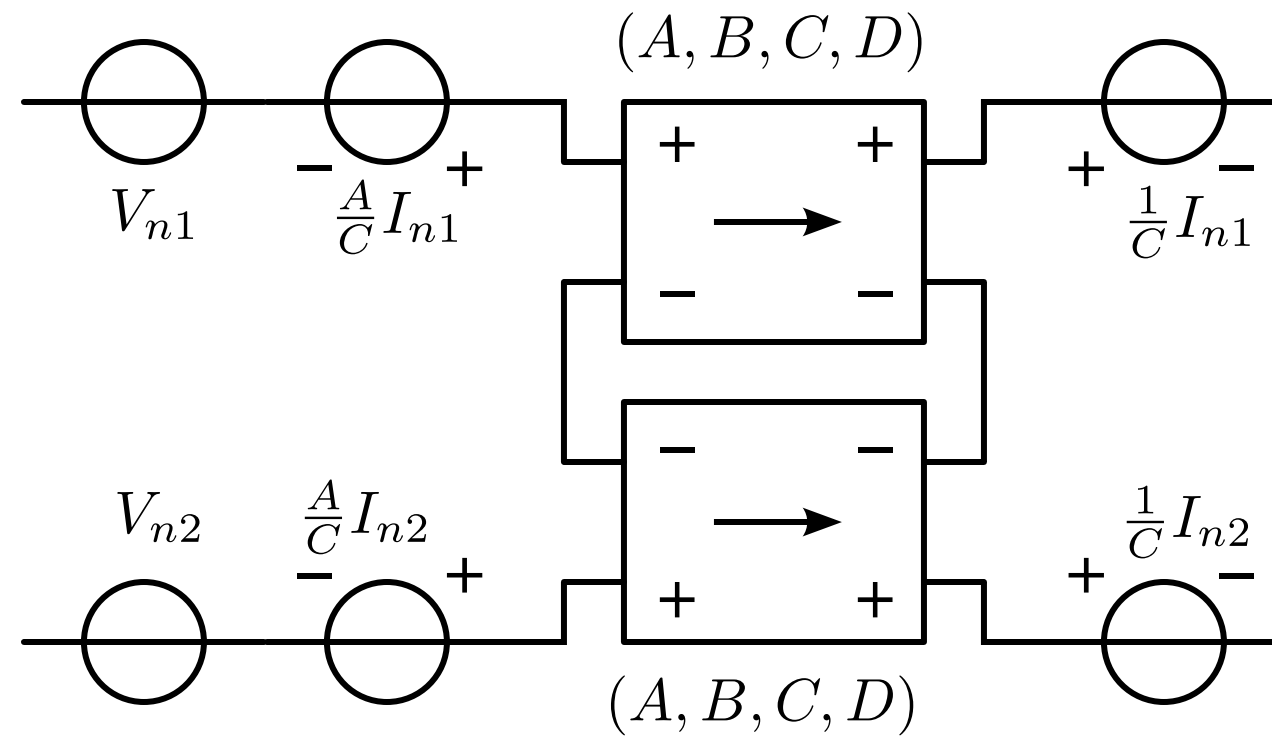
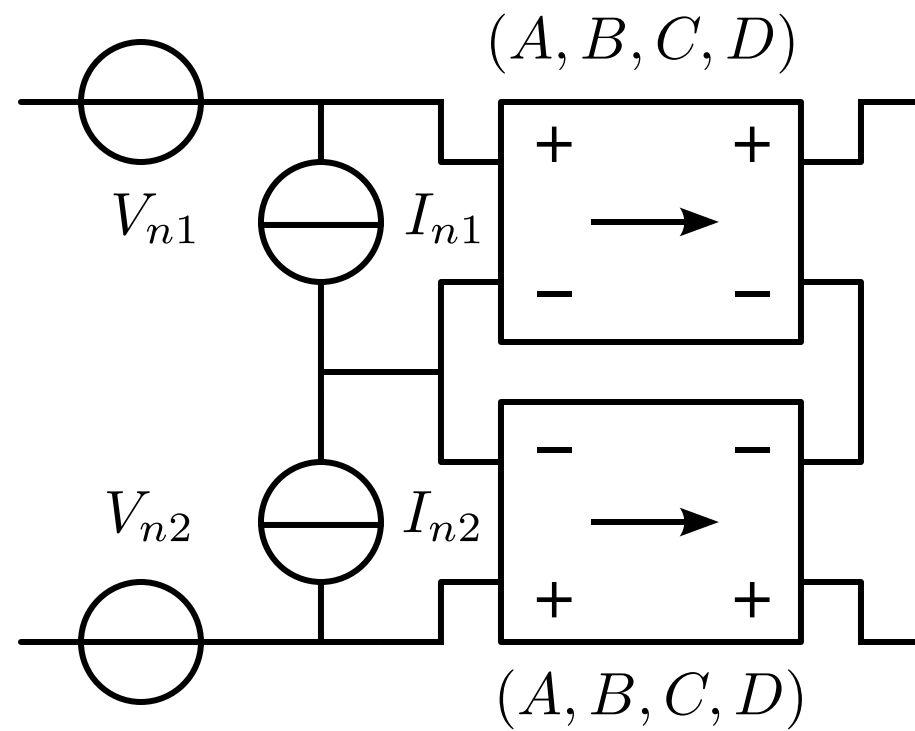
Result:

$$S_v = S_{V_{n1}} + S_{V_{n2}}$$

$$S_i = \frac{1}{4} (S_{I_{n1}} + S_{I_{n2}})$$

Differential pair stationary noise

Behavioral modifications resulting from (anti)-series connection of linear two-ports



Result:

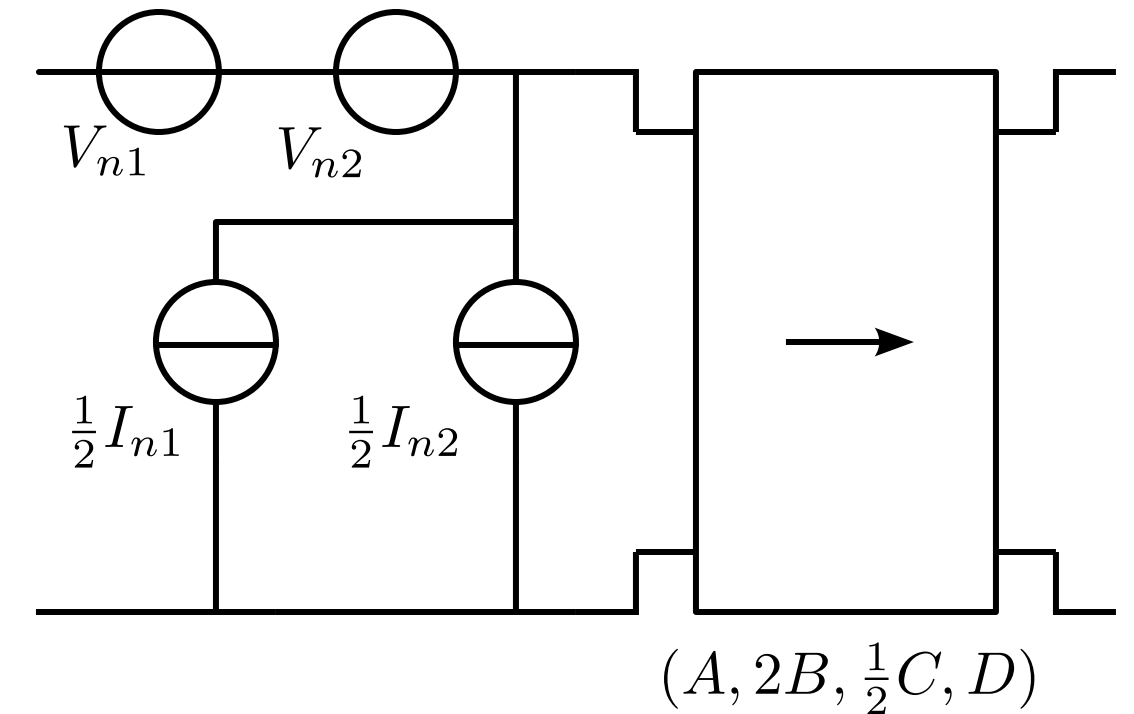
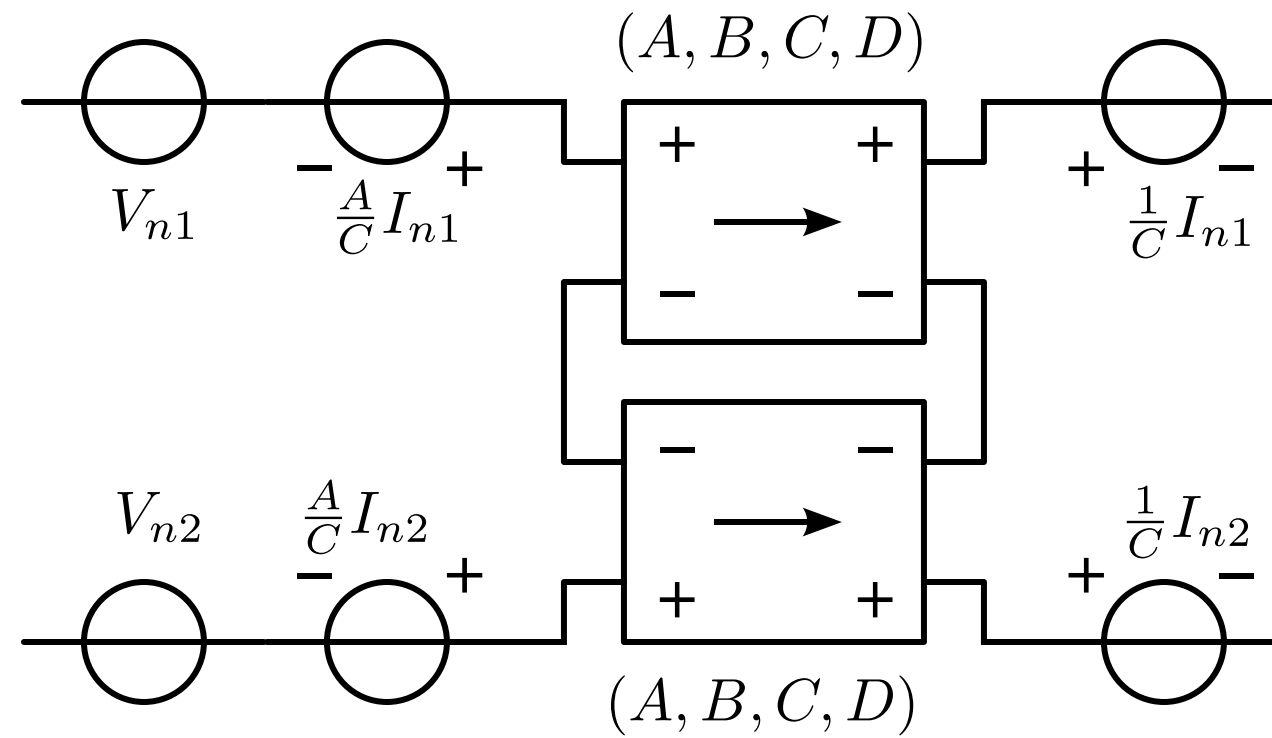
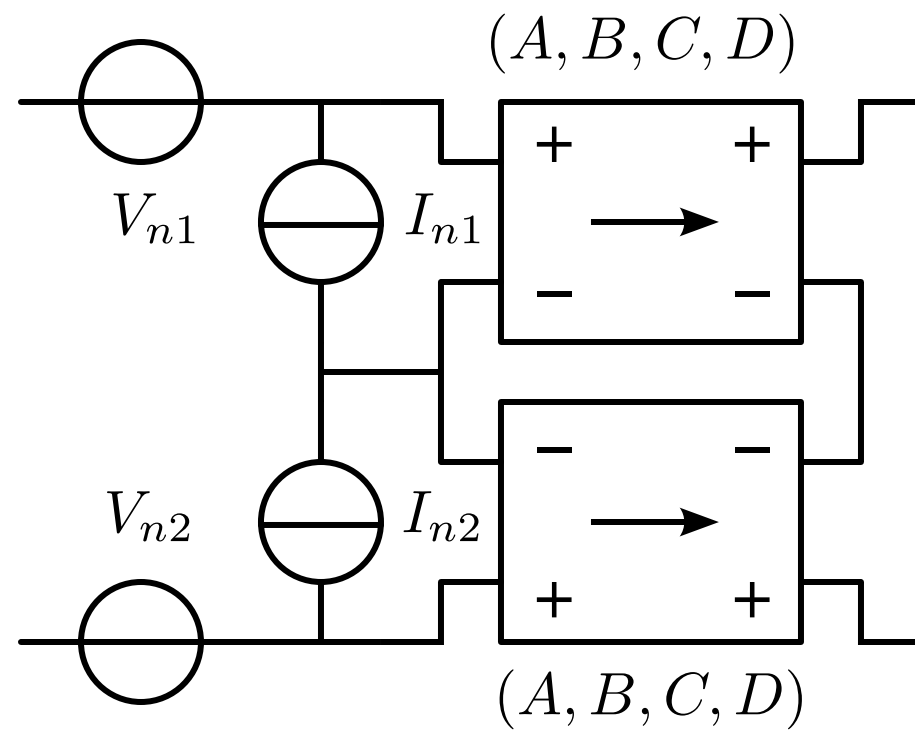
$$S_v = S_{V_{n1}} + S_{V_{n2}}$$

$$S_i = \frac{1}{4} (S_{I_{n1}} + S_{I_{n2}})$$

Conclusion:

Differential pair stationary noise

Behavioral modifications resulting from (anti)-series connection of linear two-ports



Result:

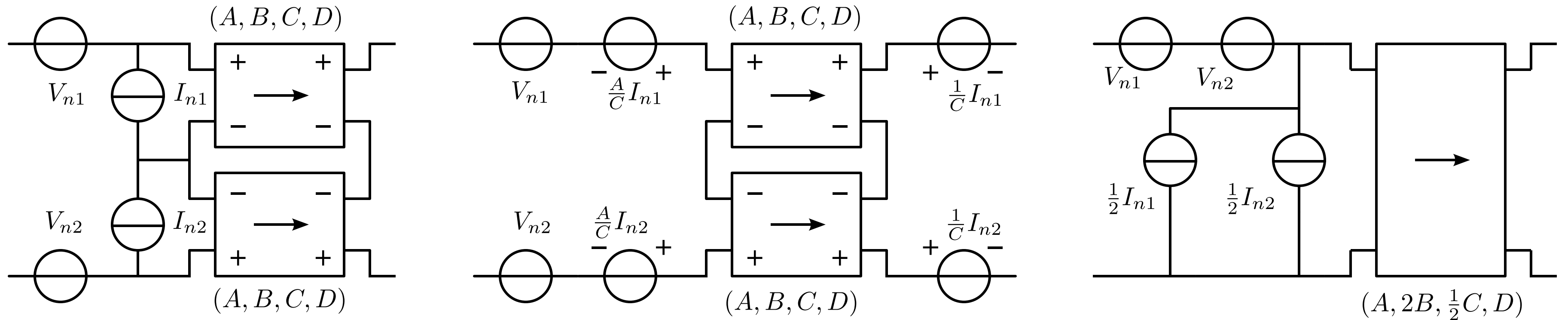
$$S_v = S_{V_{n1}} + S_{V_{n2}}$$

$$S_i = \frac{1}{4} (S_{I_{n1}} + S_{I_{n2}})$$

Conclusion: Equivalent input noise sources of a differential pair equal those of a single CS stage if:

Differential pair stationary noise

Behavioral modifications resulting from (anti)-series connection of linear two-ports



Result:

$$S_v = S_{V_{n1}} + S_{V_{n2}}$$

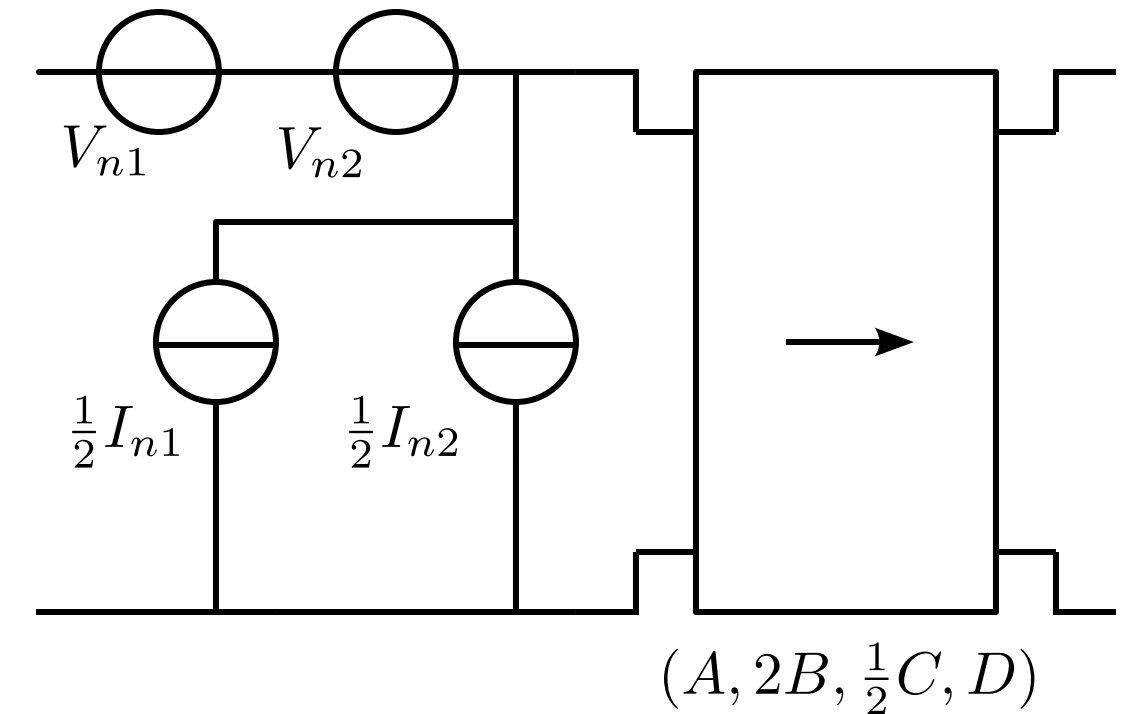
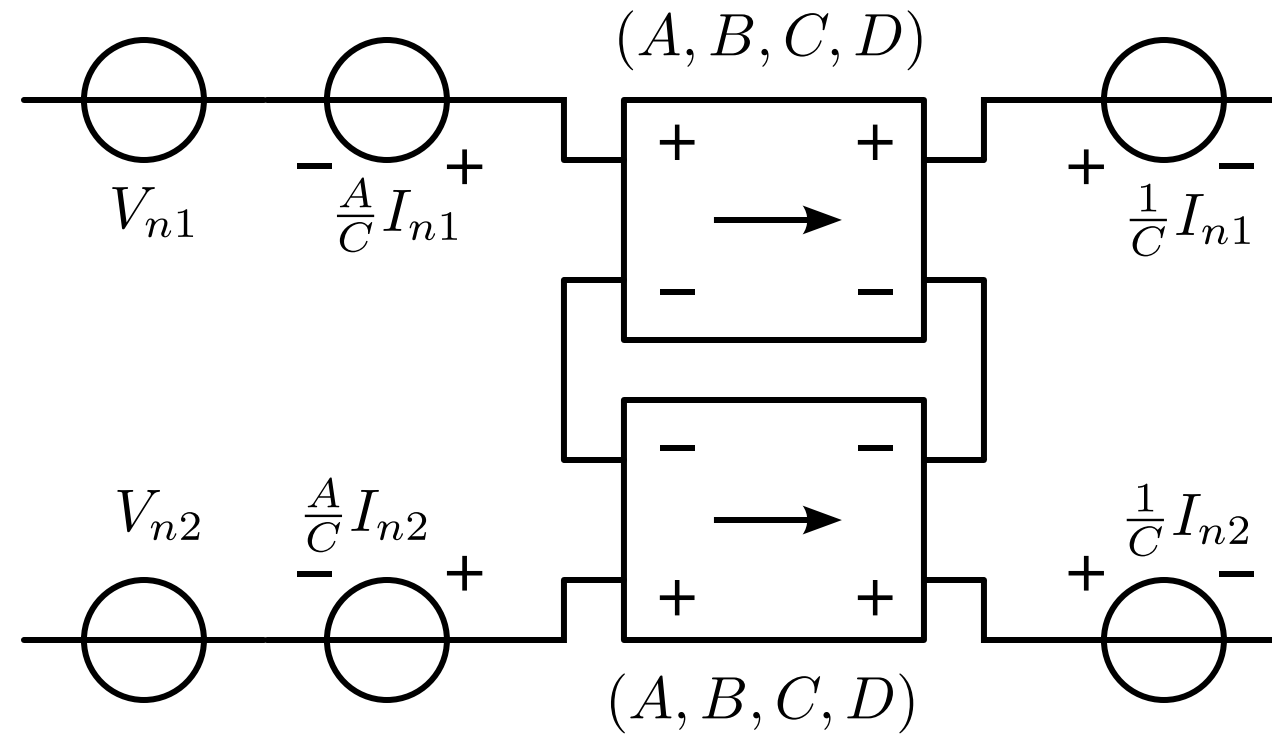
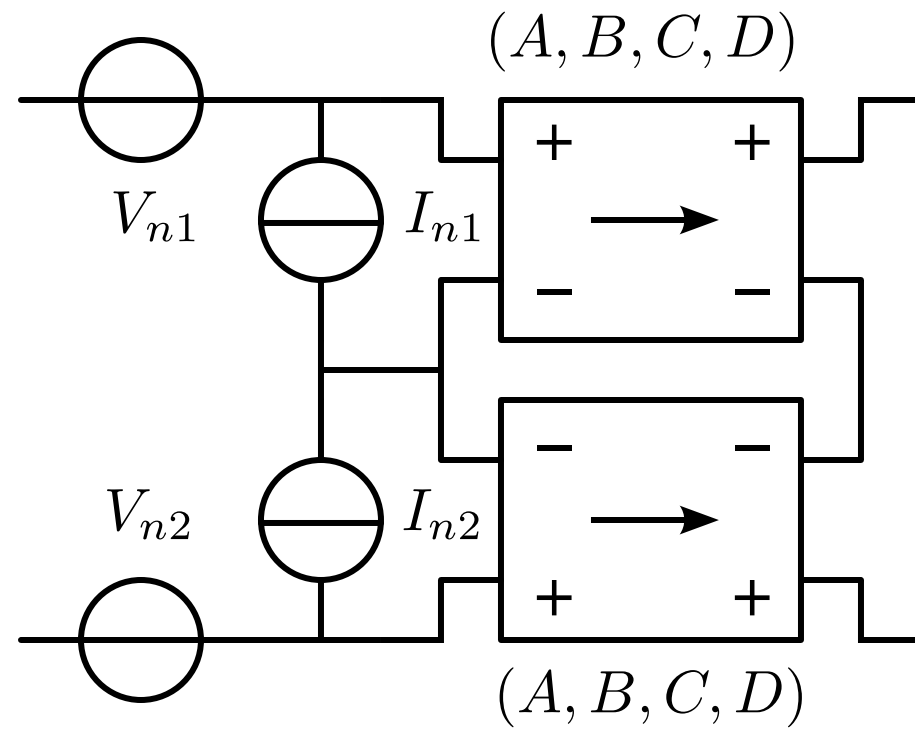
$$S_i = \frac{1}{4} (S_{I_{n1}} + S_{I_{n2}})$$

Conclusion: Equivalent input noise sources of a differential pair equal those of a single CS stage if:

Width and drain current of the transistors of the differential pair are twice as large as those of the single CS stage

Differential pair stationary noise

Behavioral modifications resulting from (anti)-series connection of linear two-ports



Result:

$$S_v = S_{V_{n1}} + S_{V_{n2}}$$

$$S_i = \frac{1}{4} (S_{I_{n1}} + S_{I_{n2}})$$

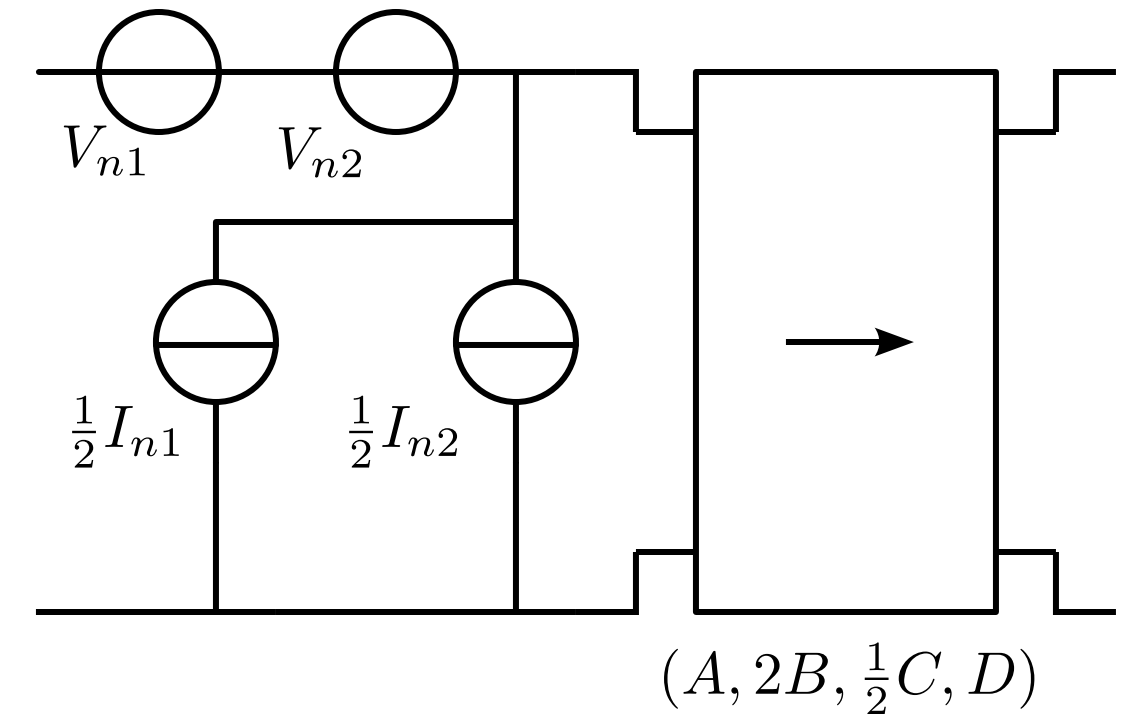
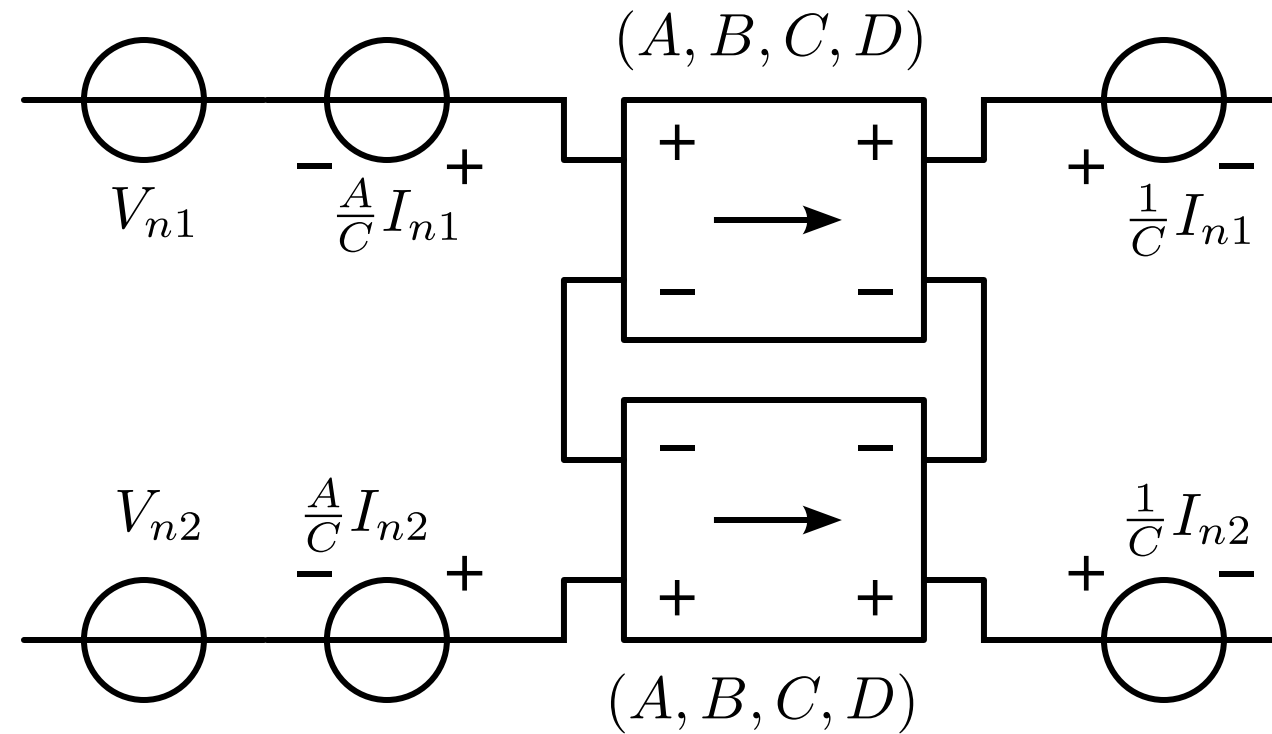
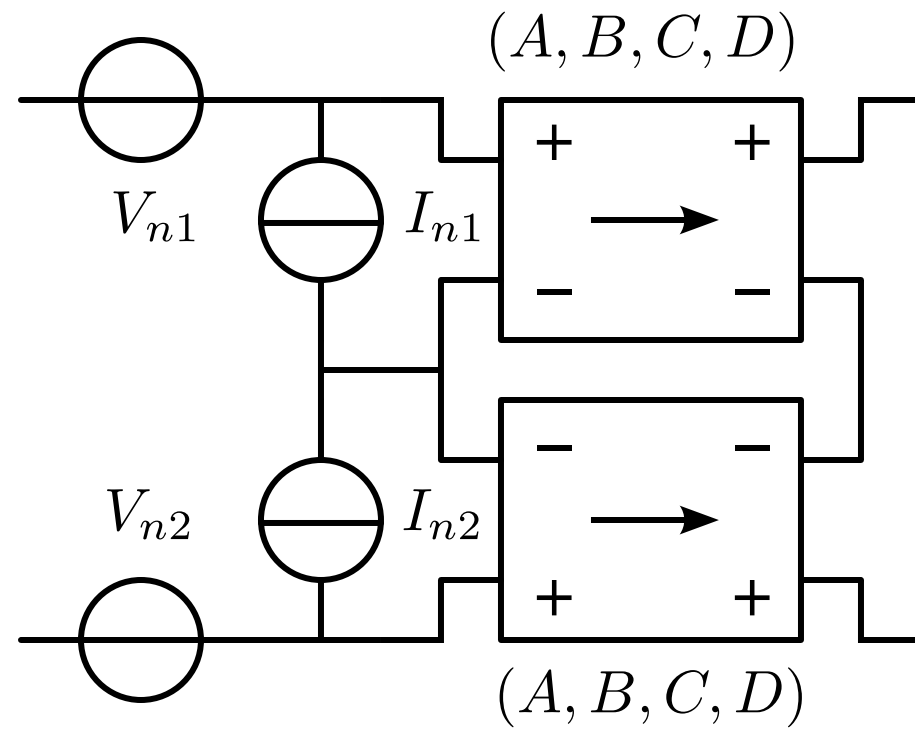
Conclusion: Equivalent input noise sources of a differential pair equal those of a single CS stage if:

Width and drain current of the transistors of the differential pair are twice as large as those of the single CS stage

Same performance: 4x more area, 4x more current

Differential pair stationary noise

Behavioral modifications resulting from (anti)-series connection of linear two-ports



Result:

$$S_v = S_{V_{n1}} + S_{V_{n2}}$$

$$S_i = \frac{1}{4} (S_{I_{n1}} + S_{I_{n2}})$$

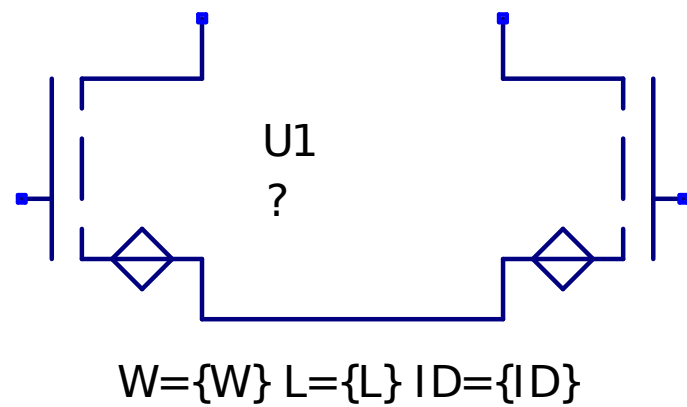
Conclusion: Equivalent input noise sources of a differential pair equal those of a single CS stage if:

Width and drain current of the transistors of the differential pair are twice as large as those of the single CS stage

Same performance: 4x more area, 4x more current

Differential pair SLiCAP model

LTspice symbol:
SLXMD

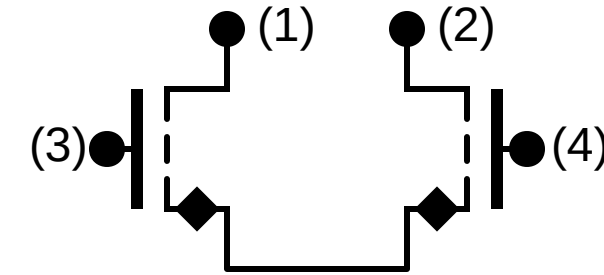


W, L and ID of the
constituting transistors

SLiCAP subcircuits for this symbol:
CMOS18ND
CMOS18PD

differential-pair MOSFET

```
Mx D1 D2 G1 G2 myMOS
.model myMOS MD
+ gm={gm}
+ go={go}
+ cgg={cgg}
+ cdg={cdg}
+ cdd={cdd}
```



Model: MD

