Structured Electronic Design

Balancing: push-pull stage

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Complementary-parallel biased CS stages



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Common-mode currents are defined by the bias voltages and the device characteristics



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(VgsN) (3) (4) + E2 (4) V2 (4) V2 (10) I12 (10) I2 (10)

































Class A operation:

Sink and source devices conduct during push and pull phase











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Class B operation:

Sink device conducts during pull phase Source device conducts during push phase











Class A operation:

Class B operation:

Class AB operation:

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Between A and B: overlap



- Sink device conducts during pull phase Source device conducts during push phase









Class B operation:

Class AB operation:

Class C operation:

Sink and source devices conduct during push and pull phase

Between A and B: overlap

Dead zone



- Sink device conducts during pull phase Source device conducts during push phase









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Class B operation:	Sink de Source
Class AB operation:	Betwee

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Behavioral modifications resulting from (anti)parallel connection of linear two-ports

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Small-signal diagram push-pull stage



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Push-pull stage SLiCAP model

SLiCAP subcircuit for this symbol: CMOS18PN