Structured Electronic Design

Intrinsic CS stage:
Equivalent-input noise sources
SLiCAP model

Anton J.M. Montagne

SLiCAP MOS noise model

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LTspice symbol: SLM_noise

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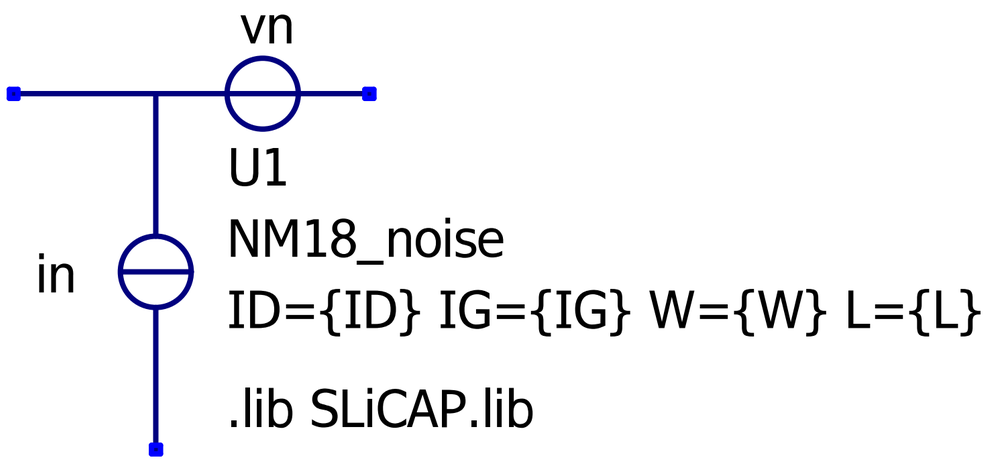
SLiCAP subcircuit NMOS18 noise model: NM18_noise

SLiCAP MOS noise model

LTspice symbol: SLM_noise



SLiCAP subcircuit NMOS18 noise model: NM18_noise

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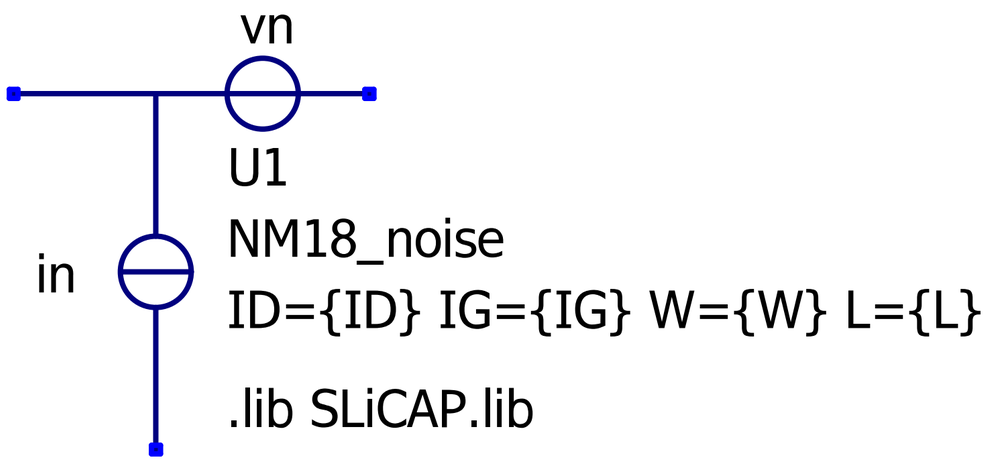
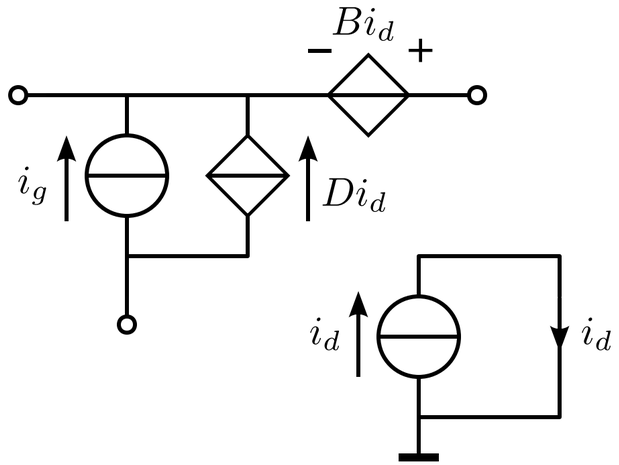


SLiCAP subcircuit NMOS18 noise model: NM18_noise



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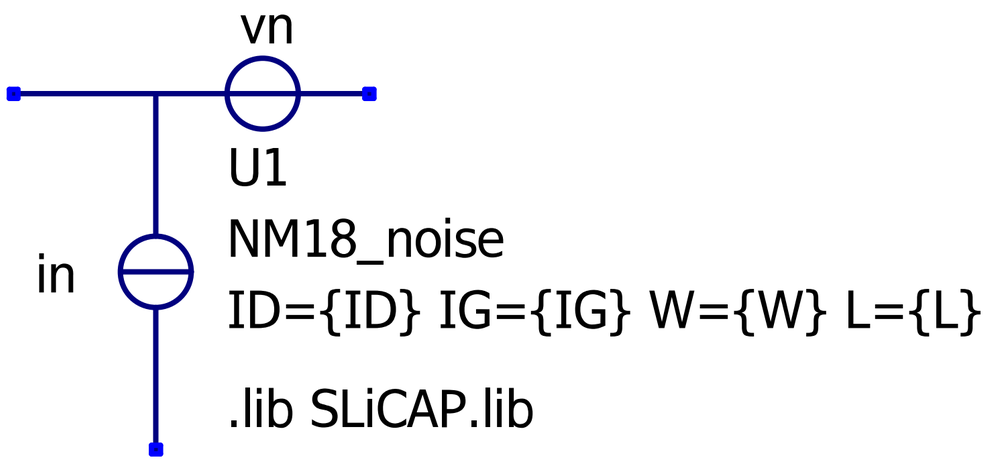
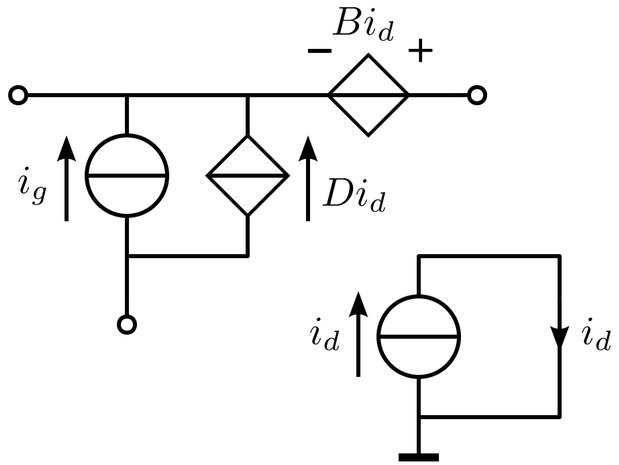


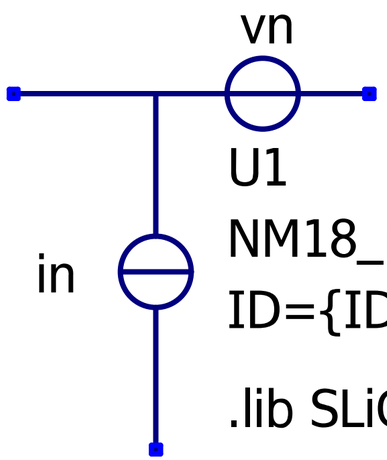
SLiCAP subcircuit NMOS18 noise model: NM18_noise

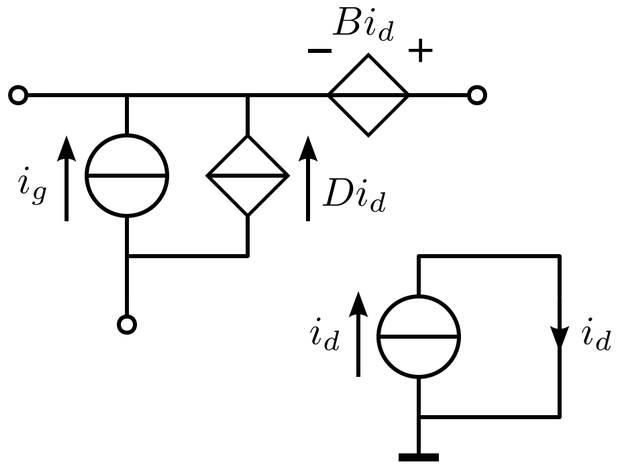
EKV model parameters saturation region



SLiCAP MOS noise model

LTspice symbol: SLM_noise





SLiCAP subcircuit NMOS18 noise model: NM18_noise

EKV model parameters saturation region

```
.subckt NM18_noise ext comm int ID={ID} IG={IG} W={W} L={L}
* intrinsic noise sources, gate resistance should be added externally
* CMOS18 N device: copy and modify this model for other devices
I1 0 1 I value=0 noise={4*k*T/R_N*(1+f_ell/f)} ; channel noise current
H1 ext int 1 10 {1/g_m}                        ; equivalent-input voltage noise
F1 ext comm 10 0 {s/2/pi/f_T}                  ; gate-induced noise
I2 ext comm I value=0 noise={2*q*IG}           ; gate shot noise
.param
* device equations MKV model saturated region
+ R_N     = {(1+IC)/(1/2 + 2/3*IC)/N_s_N18/g_m}
+ IC_CRIT = {1/((4*N_s_N18*U_T)*(Theta_N18+1/L/E_CRIT_N18))^2}
+ g_m     = {ID/(N_s_N18*U_T*sqrt(IC*(1+IC/IC_CRIT)+0.5*sqrt(IC*(1+IC/IC_CRIT))+1))}
+ c_gs    = {2/3*W*L*C_OX_N18 + CGSO_N18*W}
+ c_dg    = {CGSO_N18*W}
+ c_gb    = {CGBO_N18*2*L+(N_s_N18-1)/N_s_N18*C_OX_N18*W*L/3}
+ c_db    = {CJB0_N18*W*LDS_N18}
+ f_T     = {g_m/2/pi/c_iss}
+ c_iss   = {c_gs+c_dg+c_gb}
+ IC      = {ID*L/W/I_0_N18}
+ f_ell   = {g_m^2*R_N*KF_N18/(4*k*T*W*L*C_OX_N18)}
.ends
```