

# Structured Electronic Design Controller Design

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Input stage

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Performance aspect: noise

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Stage type: CS or balanced (best nullor-like)

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minimizes noise contributions of other stages

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Determine design limits for  $W$ ,  $L$ ,  $W/L$  and  $I_D$

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Performance aspects: VI-drive capability and power efficiency

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Stage type: complementary parallel CS

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Determine design limits for  $W$ ,  $L$ ,  $W/L$  and  $I_D$

## Output stage

Performance aspects: VI-drive capability and power efficiency

Stage type: complementary parallel CS

nullor like: minimizes distortion contributions of other stages

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Determine design limits for  $W$ ,  $L$ ,  $W/L$  and  $I_D$

## Output stage

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nullor like: minimizes distortion contributions of other stages

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Determine design limits for  $W$ ,  $L$ ,  $W/L$  and  $I_D$

## Output stage

Performance aspects: VI-drive capability and power efficiency

Stage type: complementary parallel CS

nullor like: minimizes distortion contributions of other stages

complementary parallel: high power efficiency

Determine design limits for  $W_P$  and  $W_N$  and  $I_{DQ}$

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Number of stages

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Determine design limits for  $W_P$  and  $W_N$  and  $I_{DQ}$

## Number of stages

1

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Determine design limits for  $W_P$  and  $W_N$  and  $I_{DQ}$

Number of stages

1

2

# Controller design

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Number of stages

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$n > 2$

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Noise and VI-drive can be met with single stage

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Loop gain-poles product OK?

Diff. error to loop gain ratio OK?

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noise performance can be met

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Noise and VI-drive can be met with single stage

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Diff. error to loop gain ratio OK?

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noise performance can be met  
1-st stage can drive 2-nd stage

$n > 2$

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noise performance can be met  
*i-1-th stage can drive i-th stage*

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 $i-1$ -th stage can drive  $i$ -th stage

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