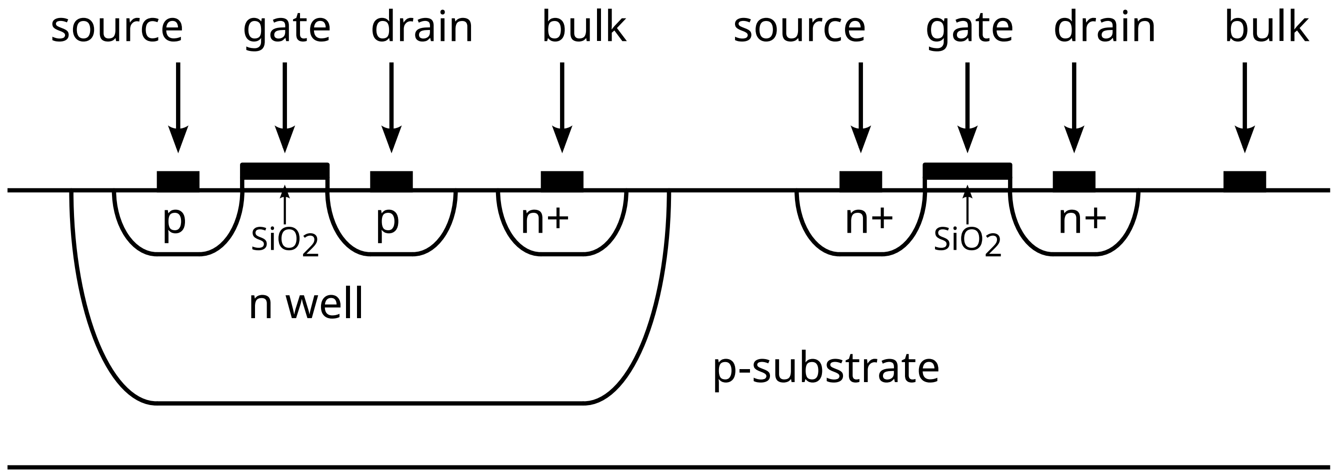
Structured Electronic Design

MOS EKV model

Anton J.M. Montagne

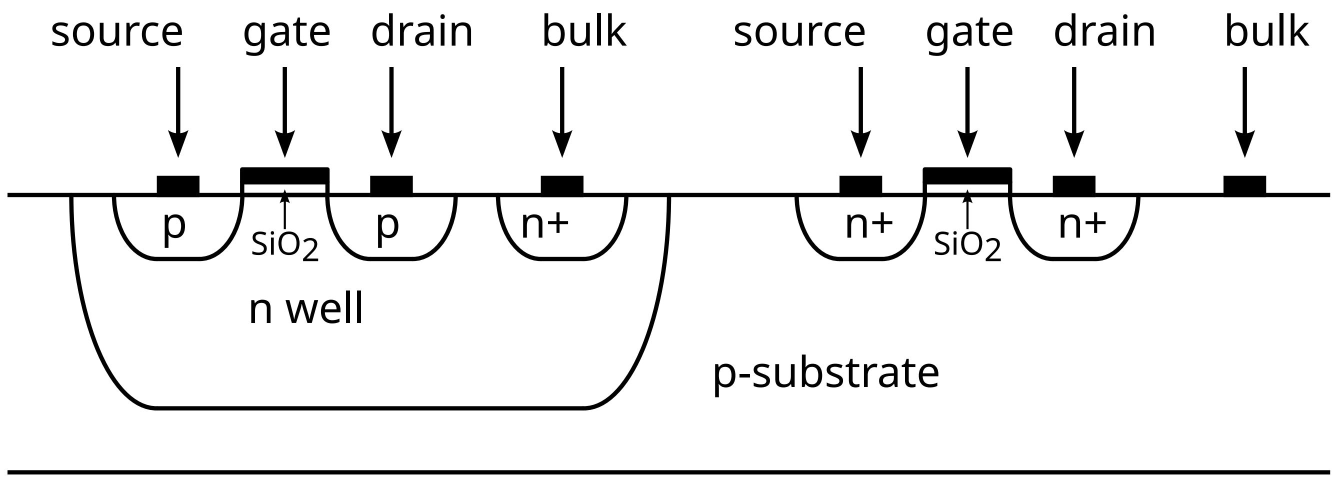
MOS operation

MOS operation

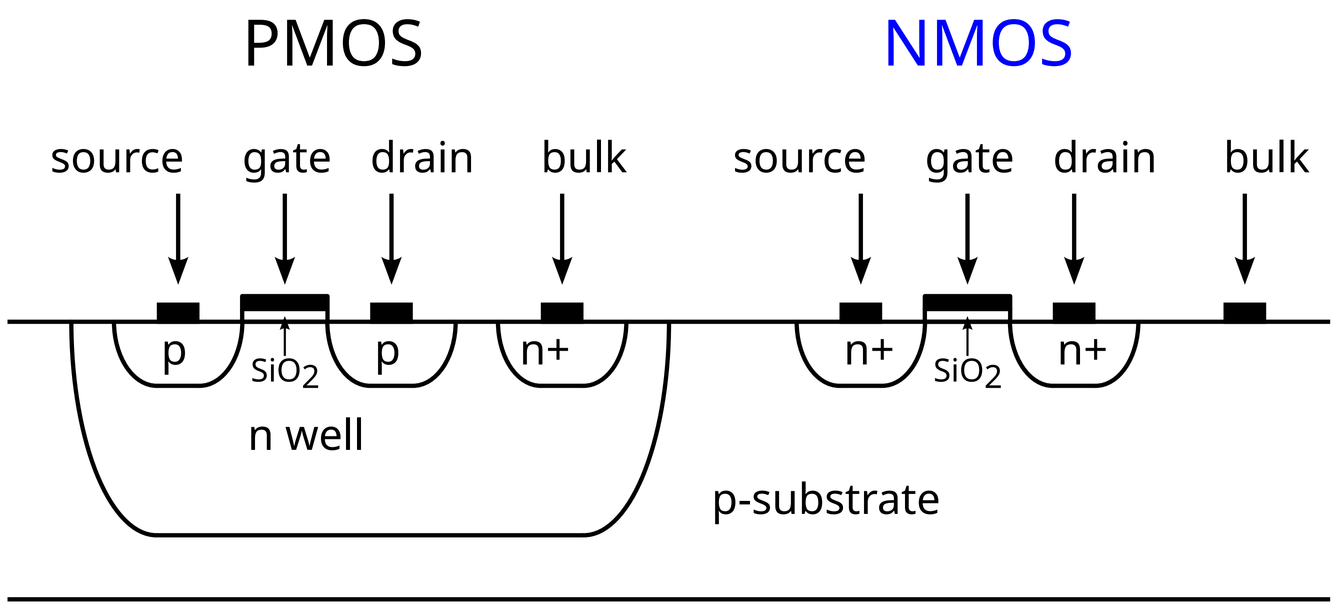


MOS operation

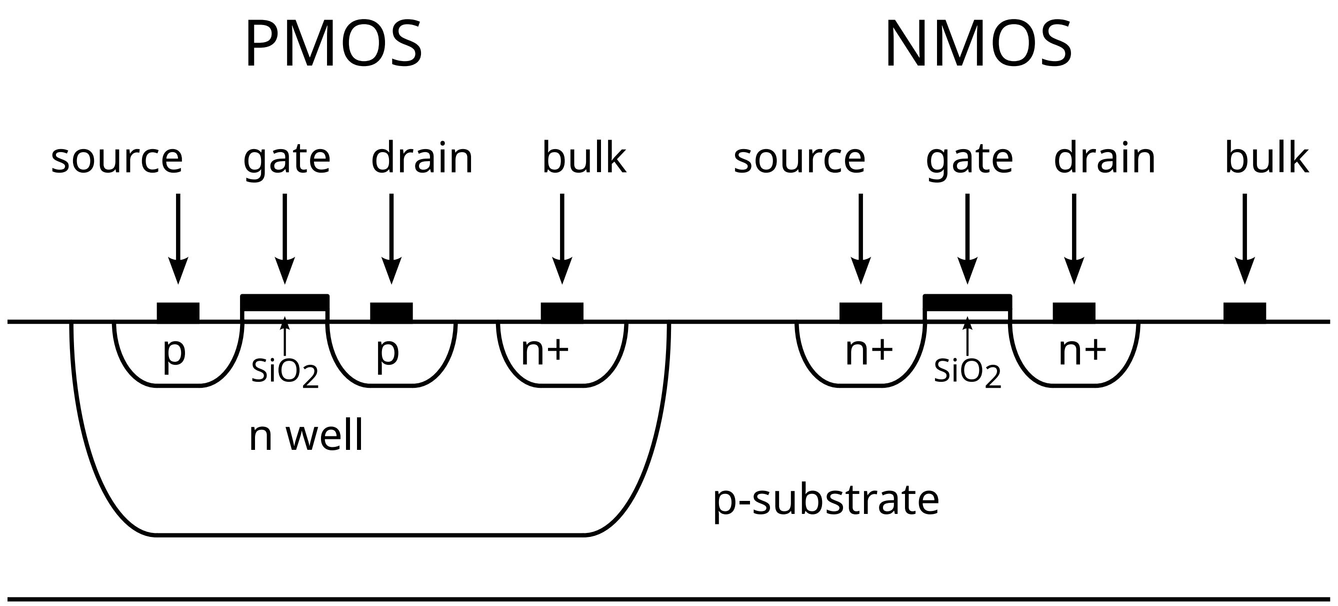
PMOS

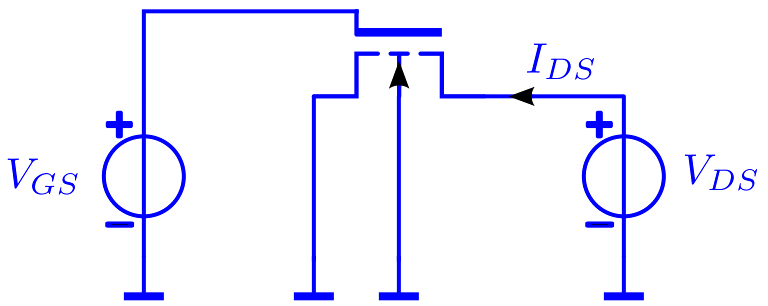


MOS operation

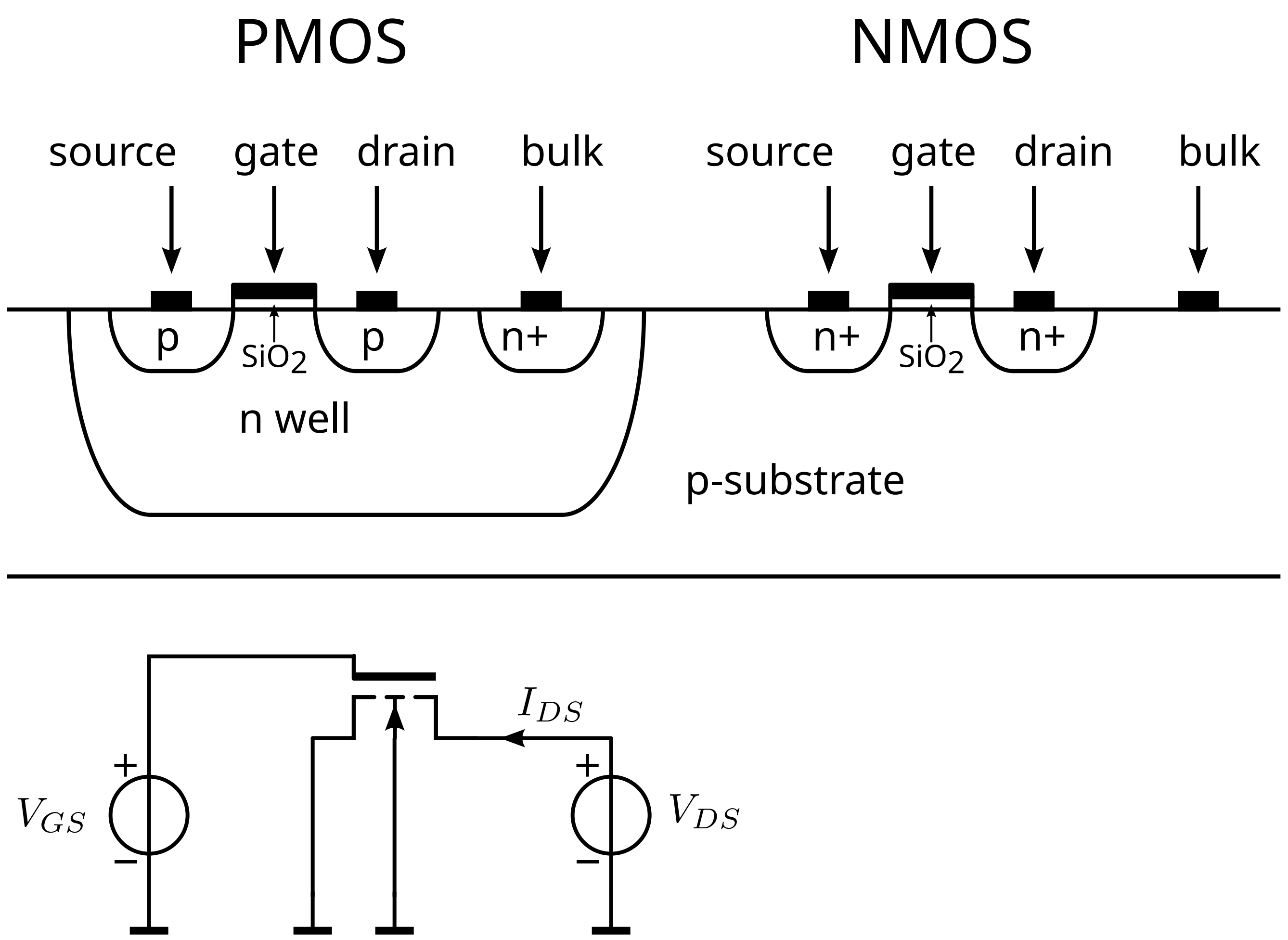


MOS operation





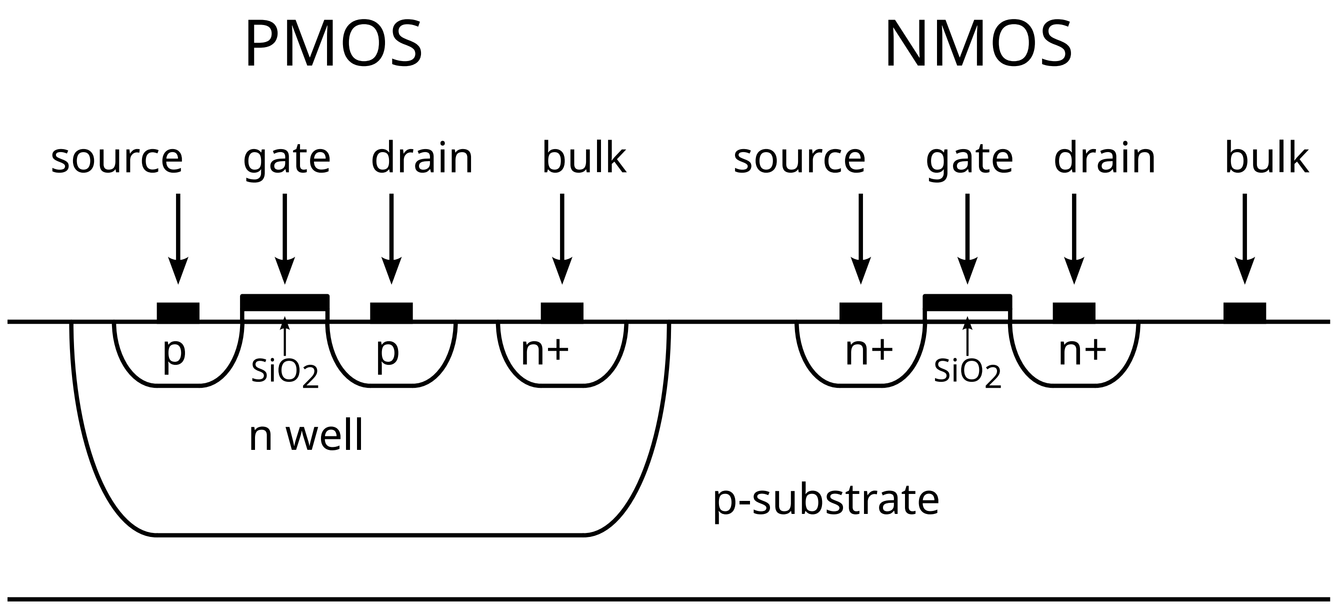
MOS operation

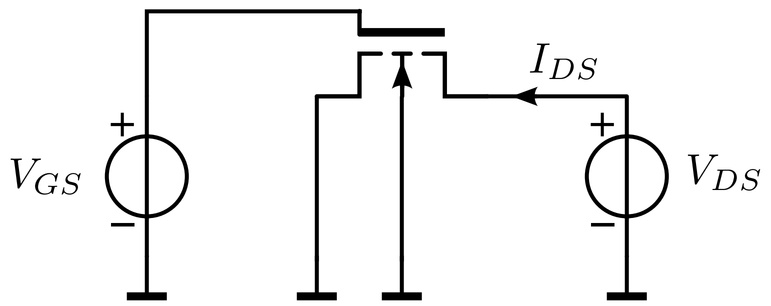


$$V_{GS} = 0,\ V_{DS} > 0$$

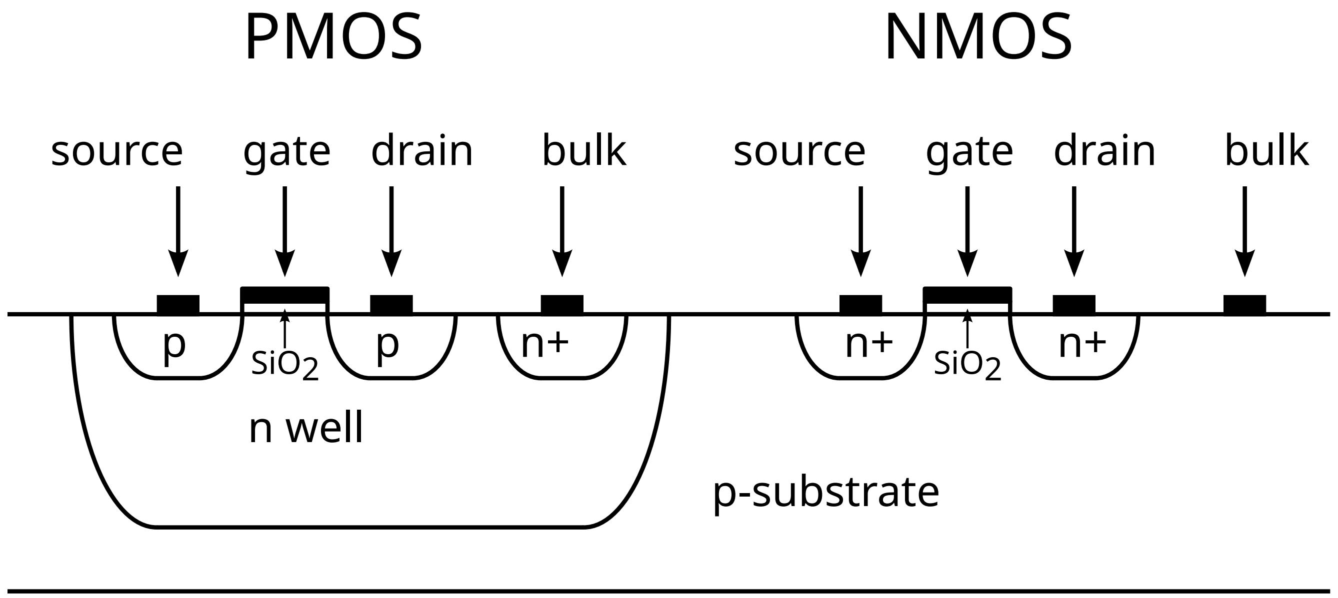
MOS operation

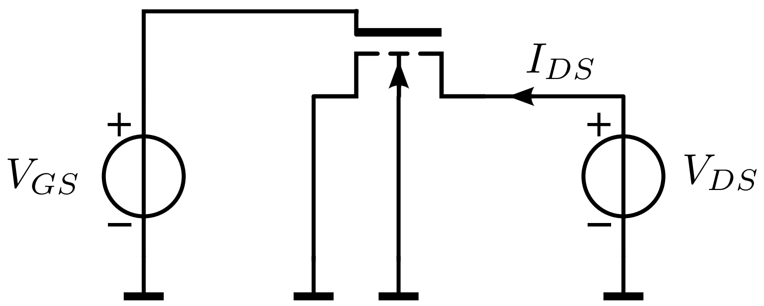
$V_{GS} = 0,\, V_{DS} > 0$ No current flow





MOS operation

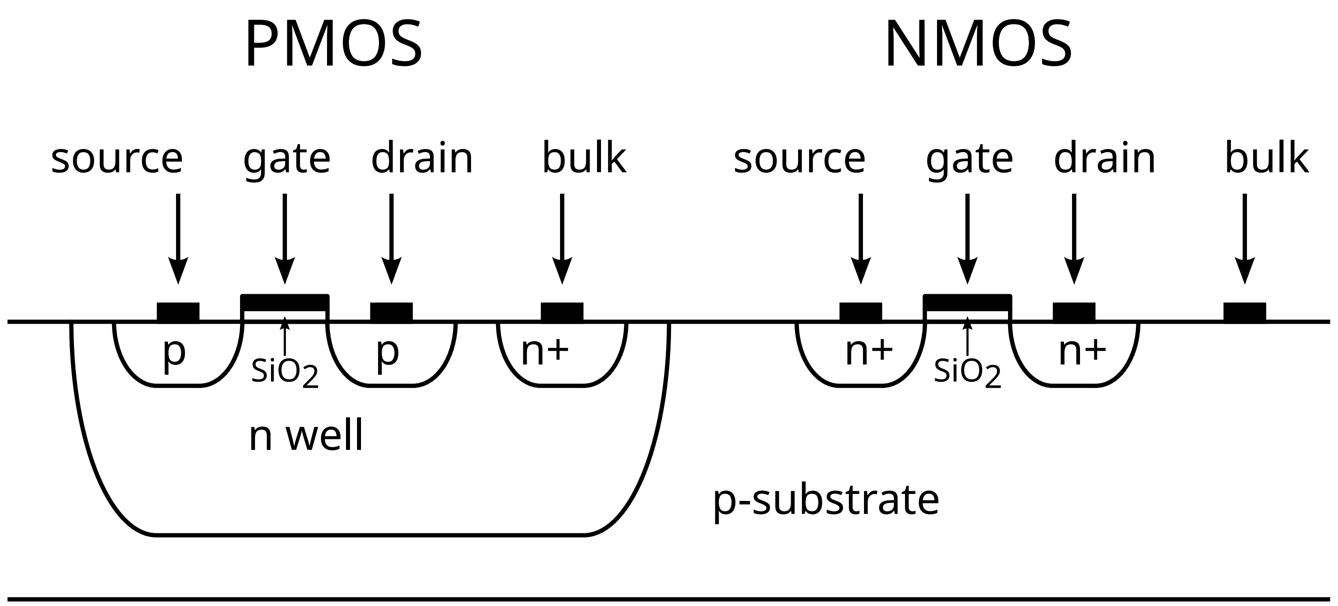


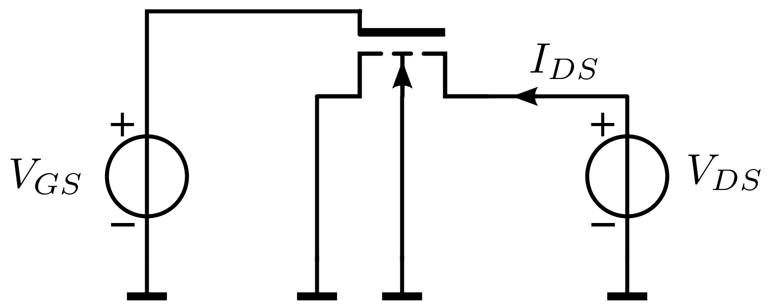


$V_{GS} = 0,\ V_{DS} > 0$ No current flow

$V_{GS} > 0,\ V_{DS} >> 0$

MOS operation



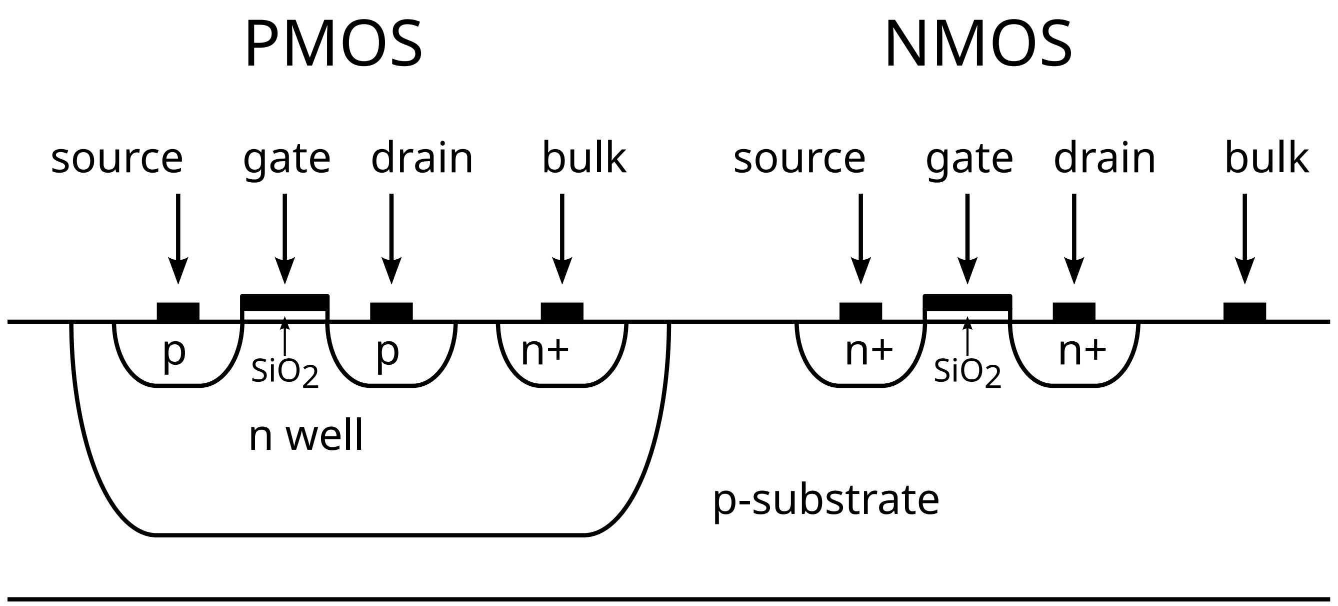


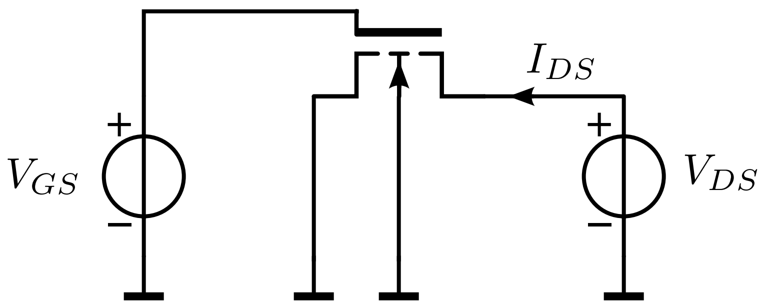
$V_{GS} = 0,\ V_{DS} > 0$ No current flow

$V_{GS} > 0,\ V_{DS} >> 0$

Surface potential at oxide-Si interface rises

MOS operation



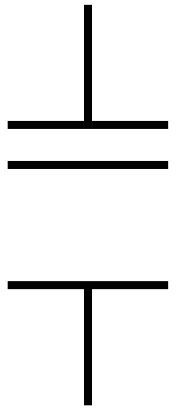


$V_{GS} = 0,\ V_{DS} > 0$ No current flow

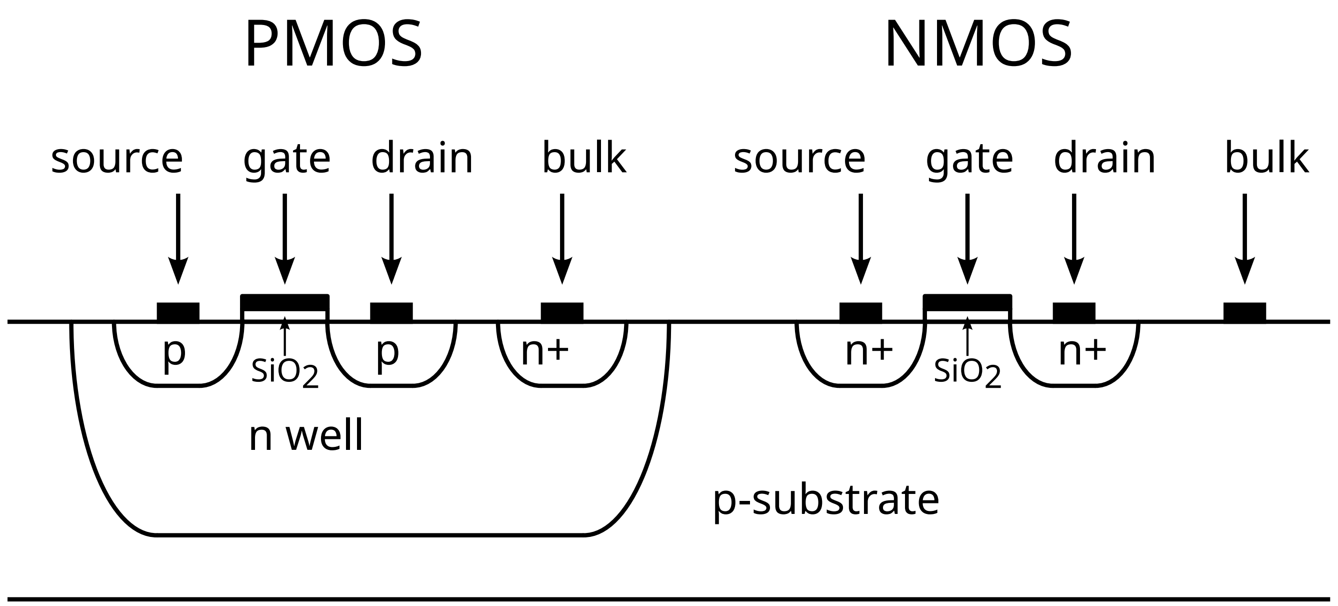
$V_{GS} > 0,\ V_{DS} >> 0$

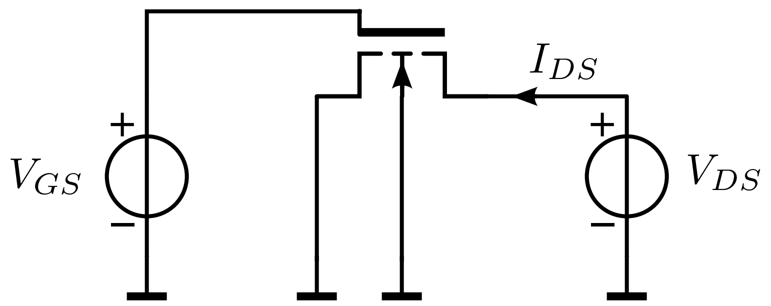
Surface potential at oxide-Si interface rises

capacitive coupling



MOS operation



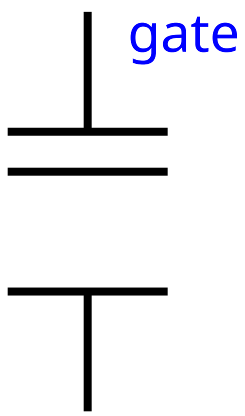


$V_{GS} = 0,\, V_{DS} > 0$ No current flow

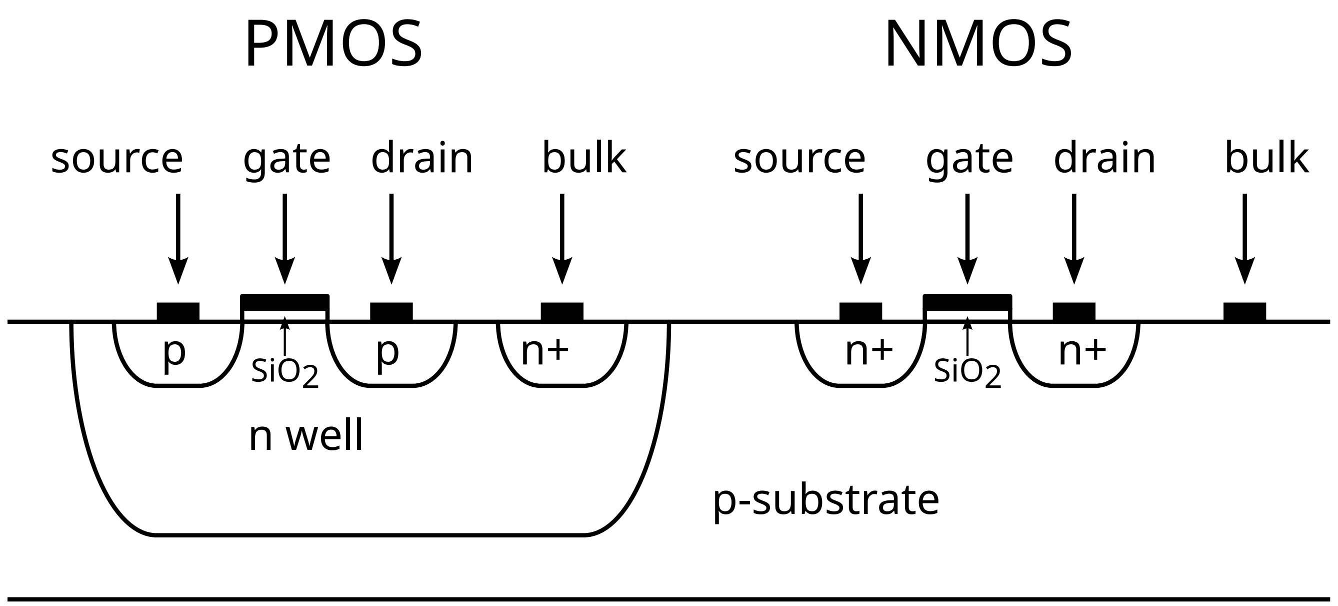
$V_{GS} > 0,\, V_{DS} >> 0$

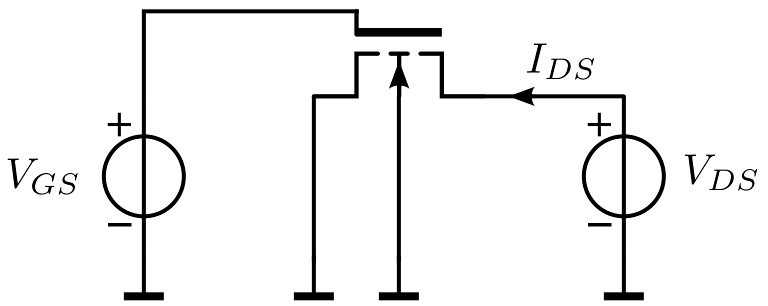
Surface potential at oxide-Si interface rises

capacitive coupling



MOS operation



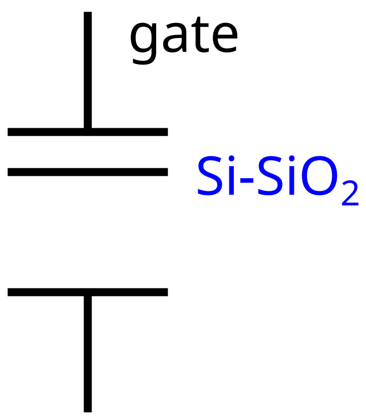


$V_{GS} = 0,\, V_{DS} > 0$ No current flow

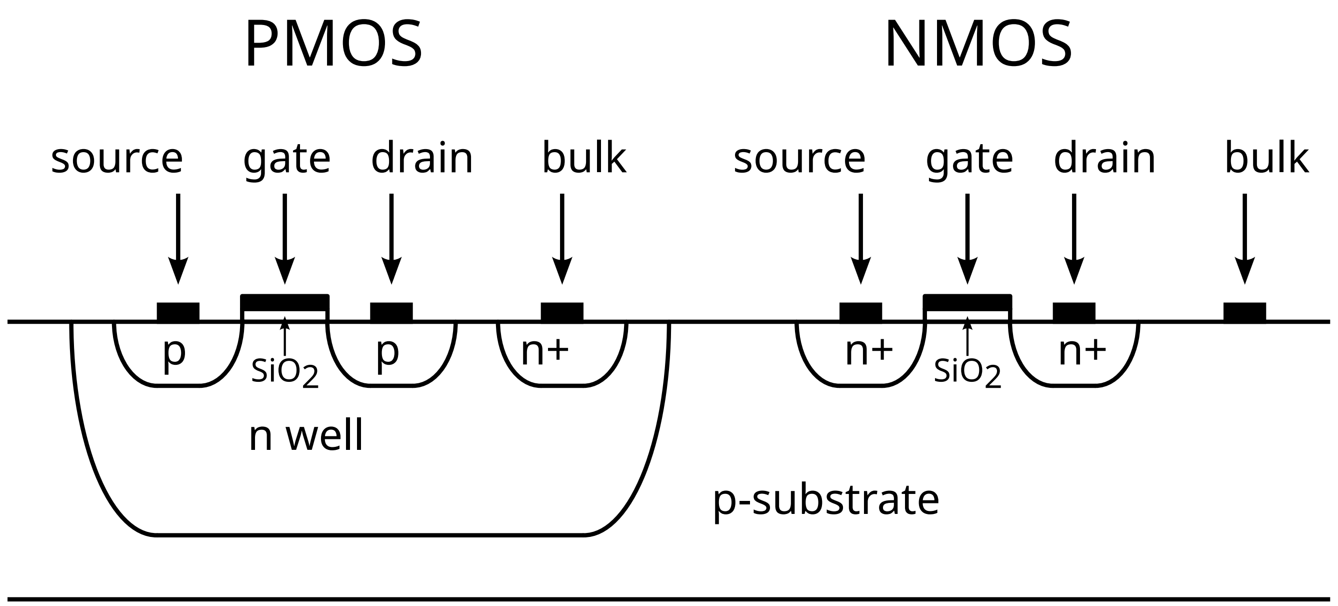
$V_{GS} > 0,\, V_{DS} >> 0$

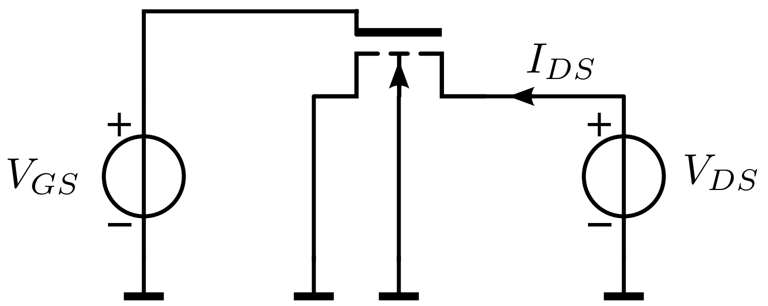
Surface potential at oxide-Si interface rises

capacitive coupling



MOS operation



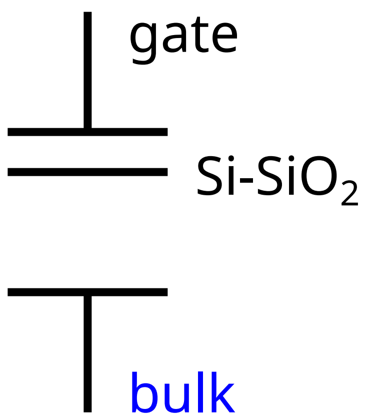


$V_{GS} = 0,\ V_{DS} > 0$ No current flow

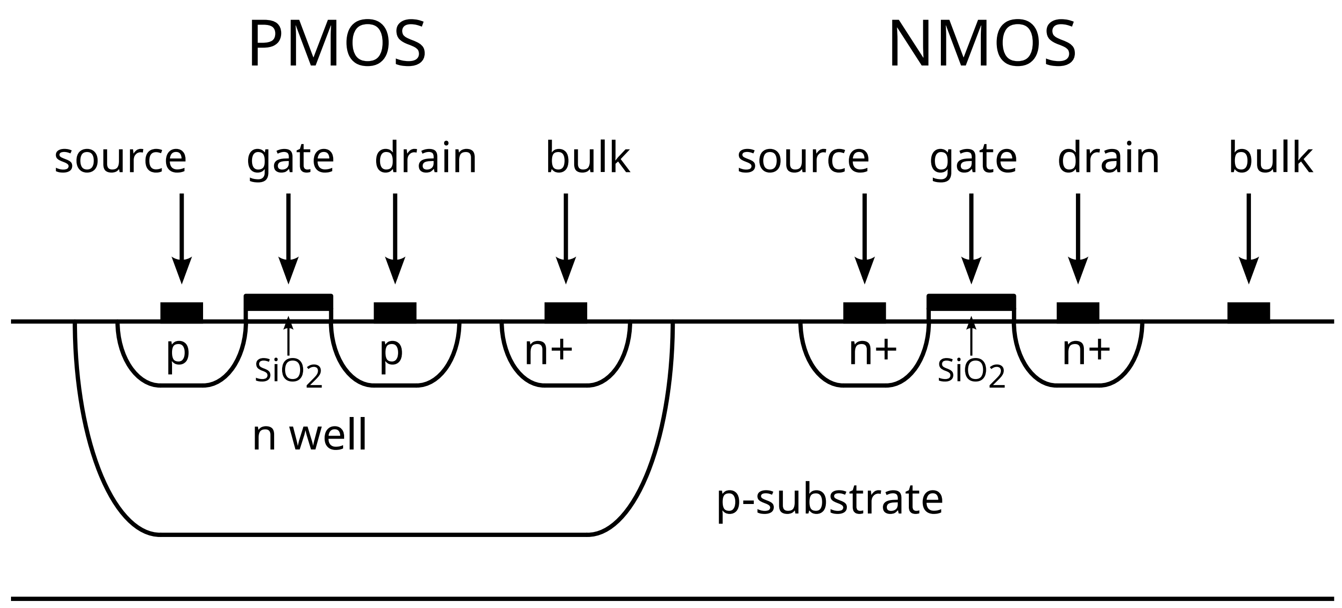
$V_{GS} > 0,\ V_{DS} >> 0$

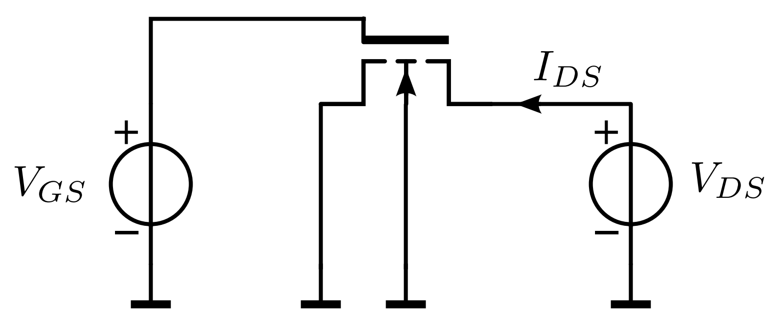
Surface potential at oxide-Si interface rises
Source injects electrons in p region

capacitive coupling



MOS operation



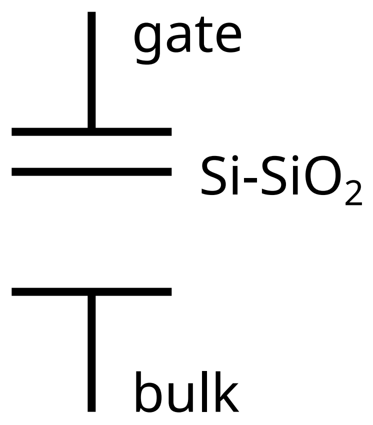


$V_{GS} = 0,\ V_{DS} > 0$ No current flow

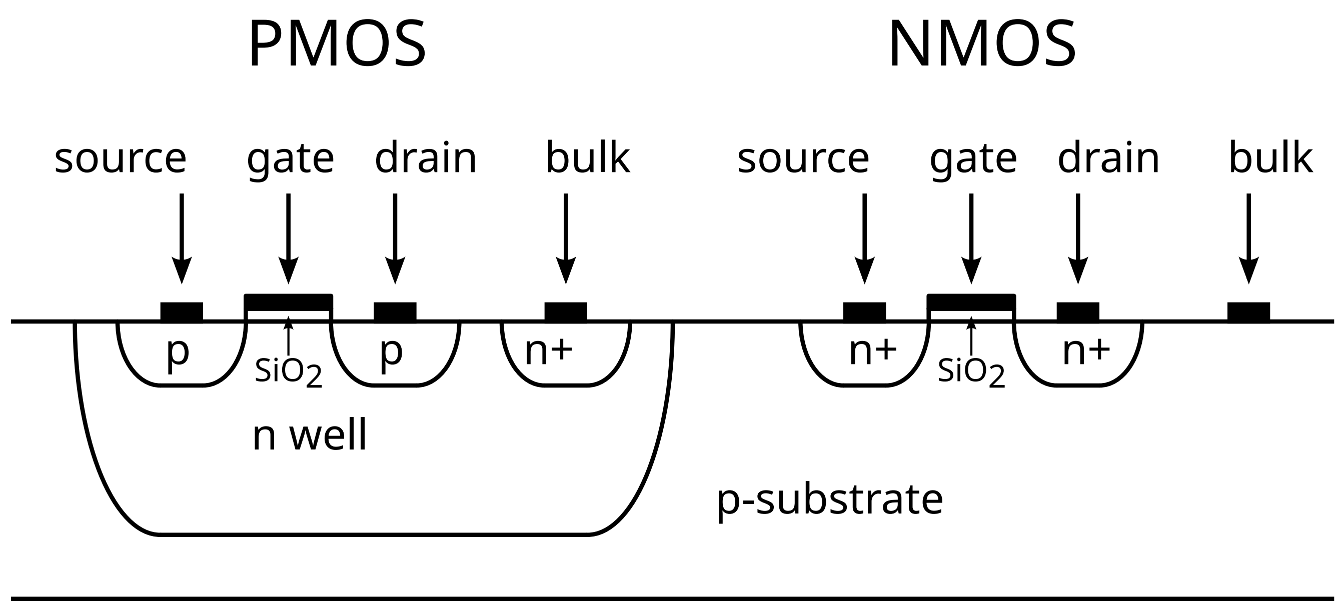
$V_{GS} > 0,\ V_{DS} >> 0$

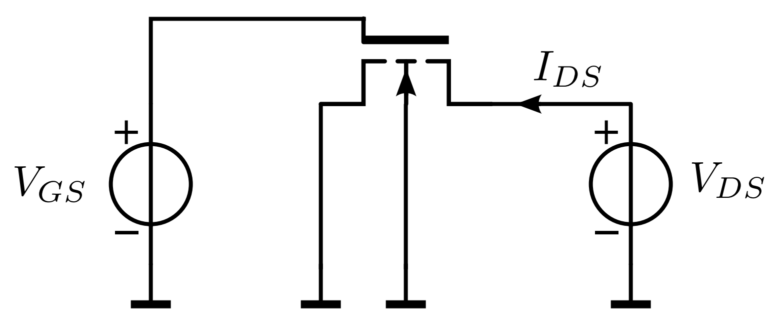
Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

capacitive coupling



MOS operation





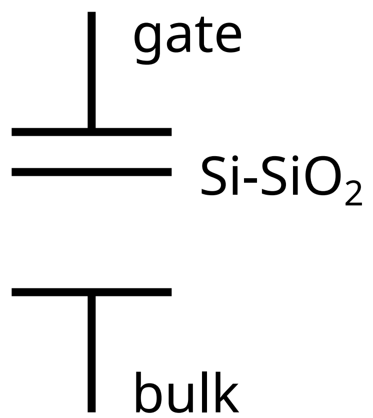
$V_{GS} = 0,\ V_{DS} > 0$ No current flow

$V_{GS} > 0,\ V_{DS} >> 0$

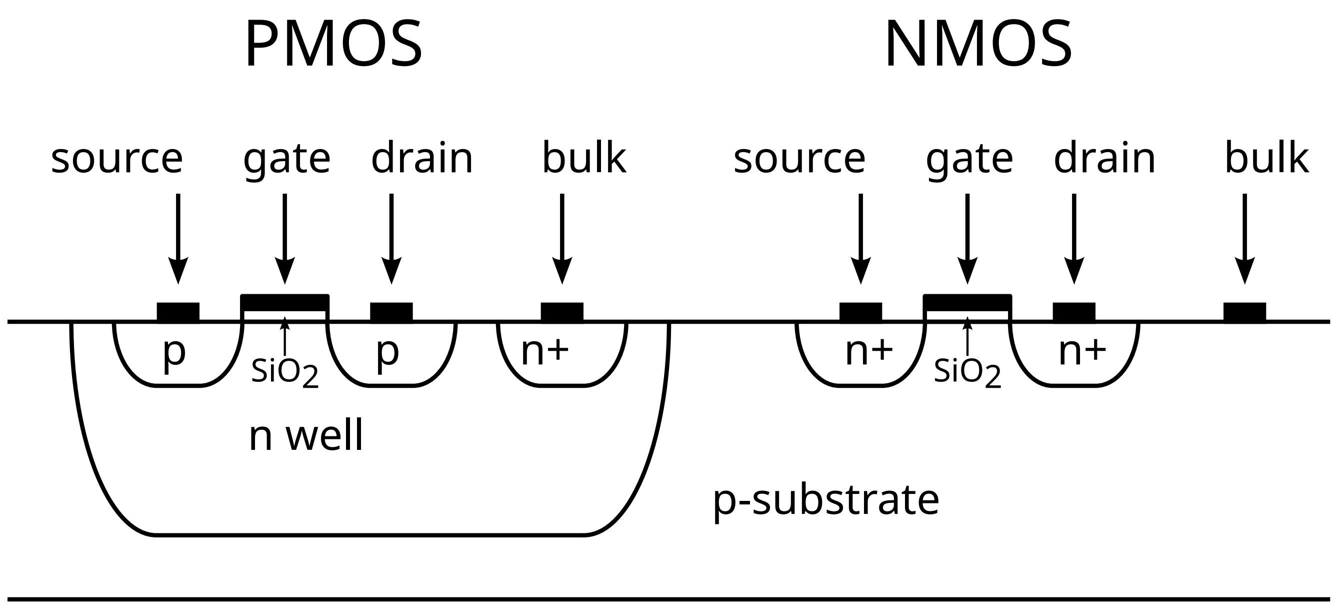
Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

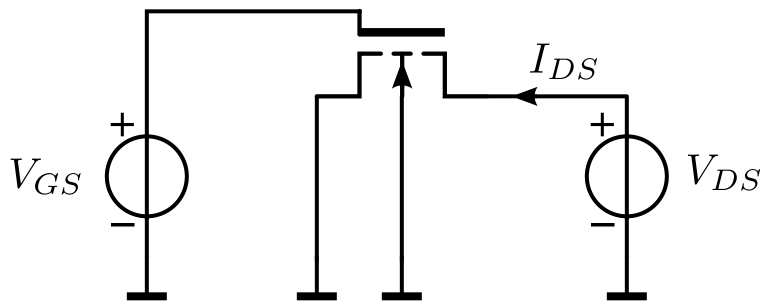
Drain current increases exponentially with the gate-source voltage

capacitive coupling



MOS operation





$V_{GS} = 0,\ V_{DS} > 0$ No current flow

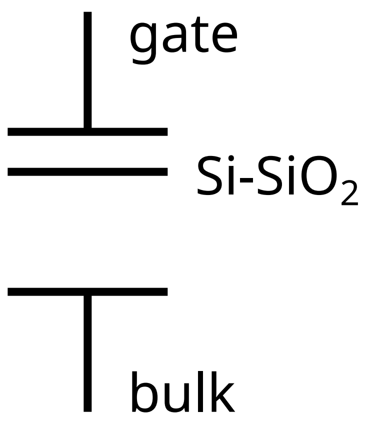
$V_{GS} > 0,\ V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

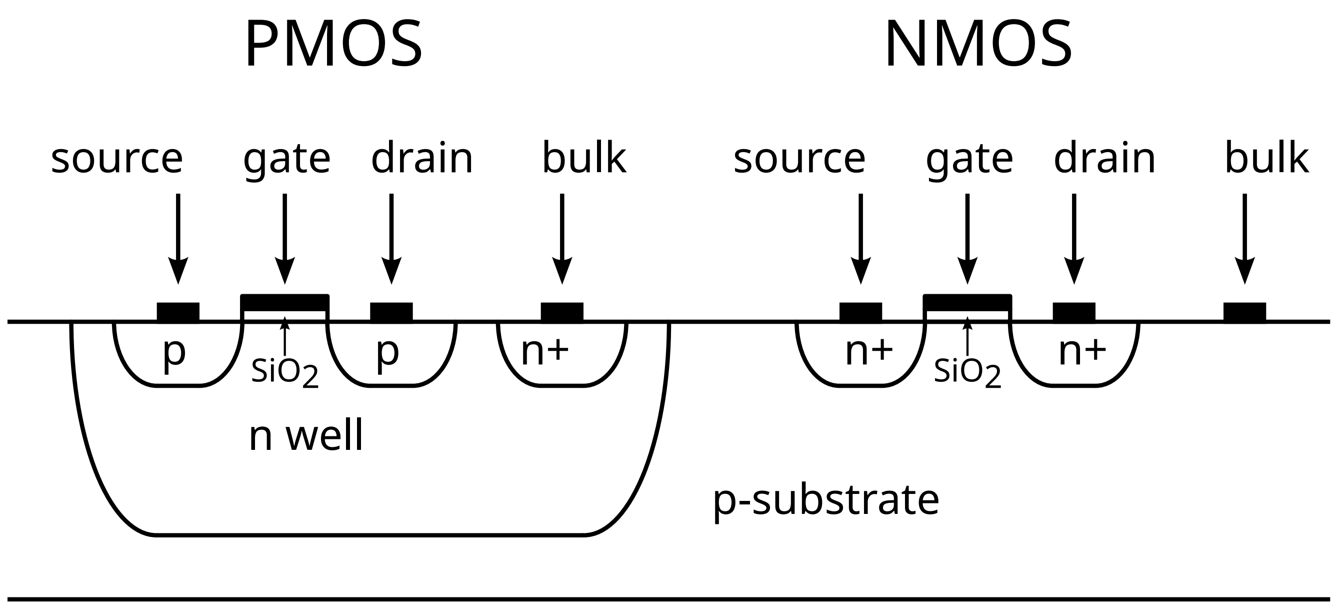
Drain current increases exponentially with the gate-source voltage

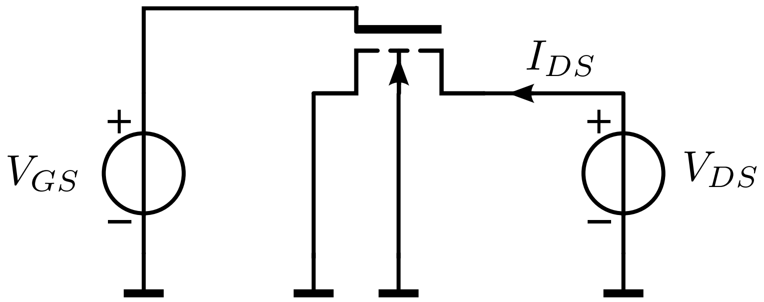
$V_{GS} > V_{th},\ V_{DS} > V_{GS} - V_{th}$

capacitive coupling

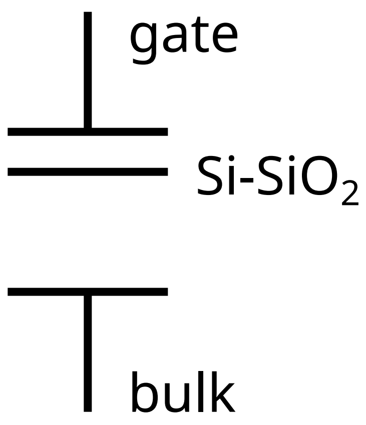


MOS operation





capacitive coupling



$V_{GS} = 0,\, V_{DS} > 0$ No current flow

$V_{GS} > 0,\, V_{DS} >> 0$

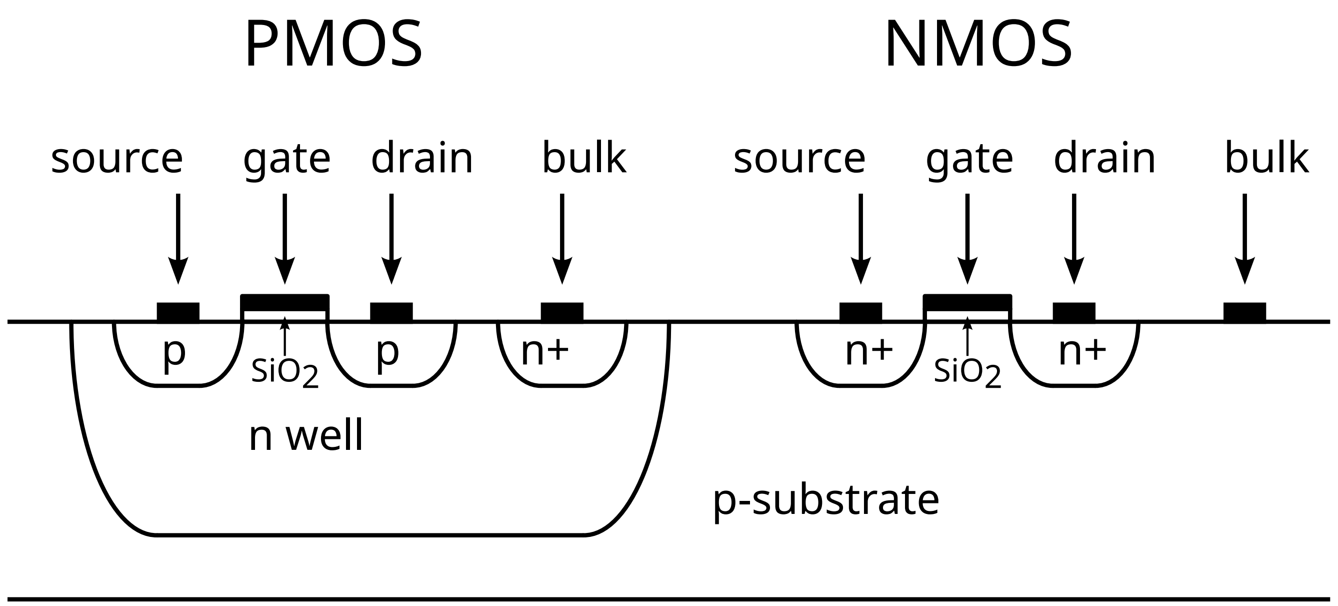
Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

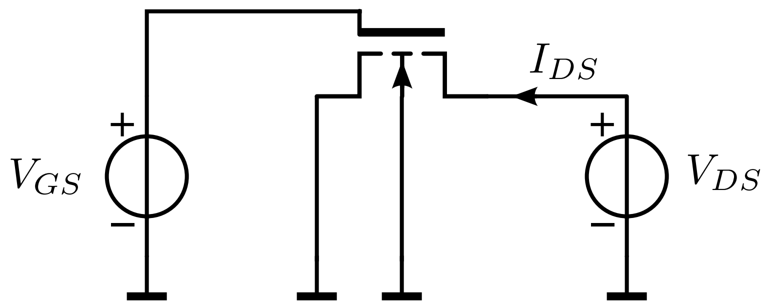
Drain current increases exponentially with the gate-source voltage

$V_{GS} > V_{th},\, V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

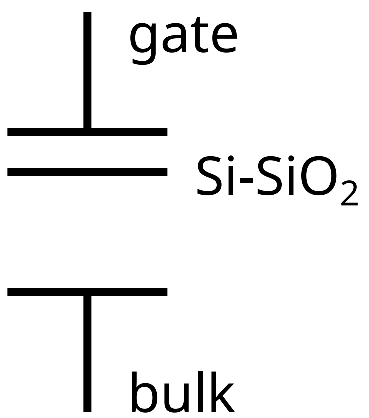
MOS operation





$V_{GS} = 0,\ V_{DS} > 0$ No current flow

capacitive coupling



$V_{GS} > 0,\ V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

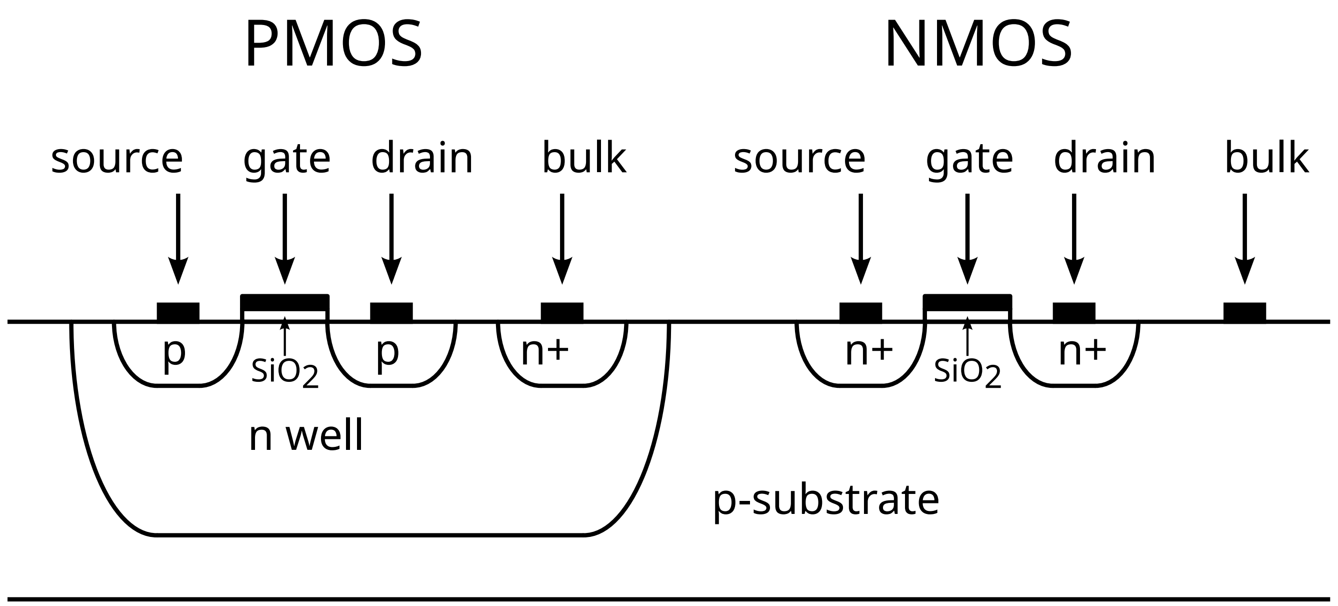
Drain current increases exponentially with the gate-source voltage

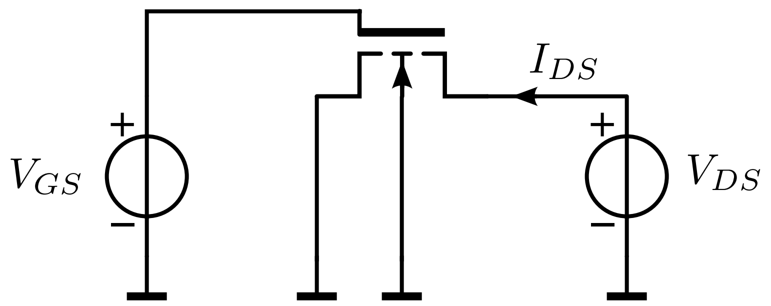
$V_{GS} > V_{th},\ V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

Drain current increases quadratically with the gate-source voltage

MOS operation





Drain-source voltage dependency

$V_{GS} = 0,\, V_{DS} > 0$ No current flow

$V_{GS} > 0,\, V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

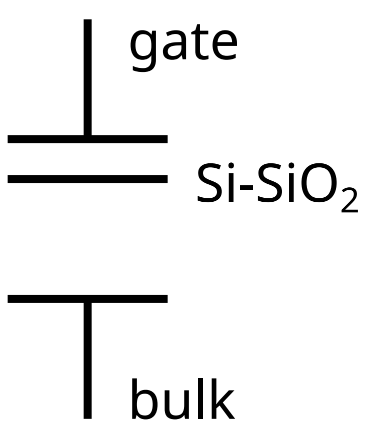
Drain current increases exponentially with the gate-source voltage

$V_{GS} > V_{th},\, V_{DS} > V_{GS} - V_{th}$

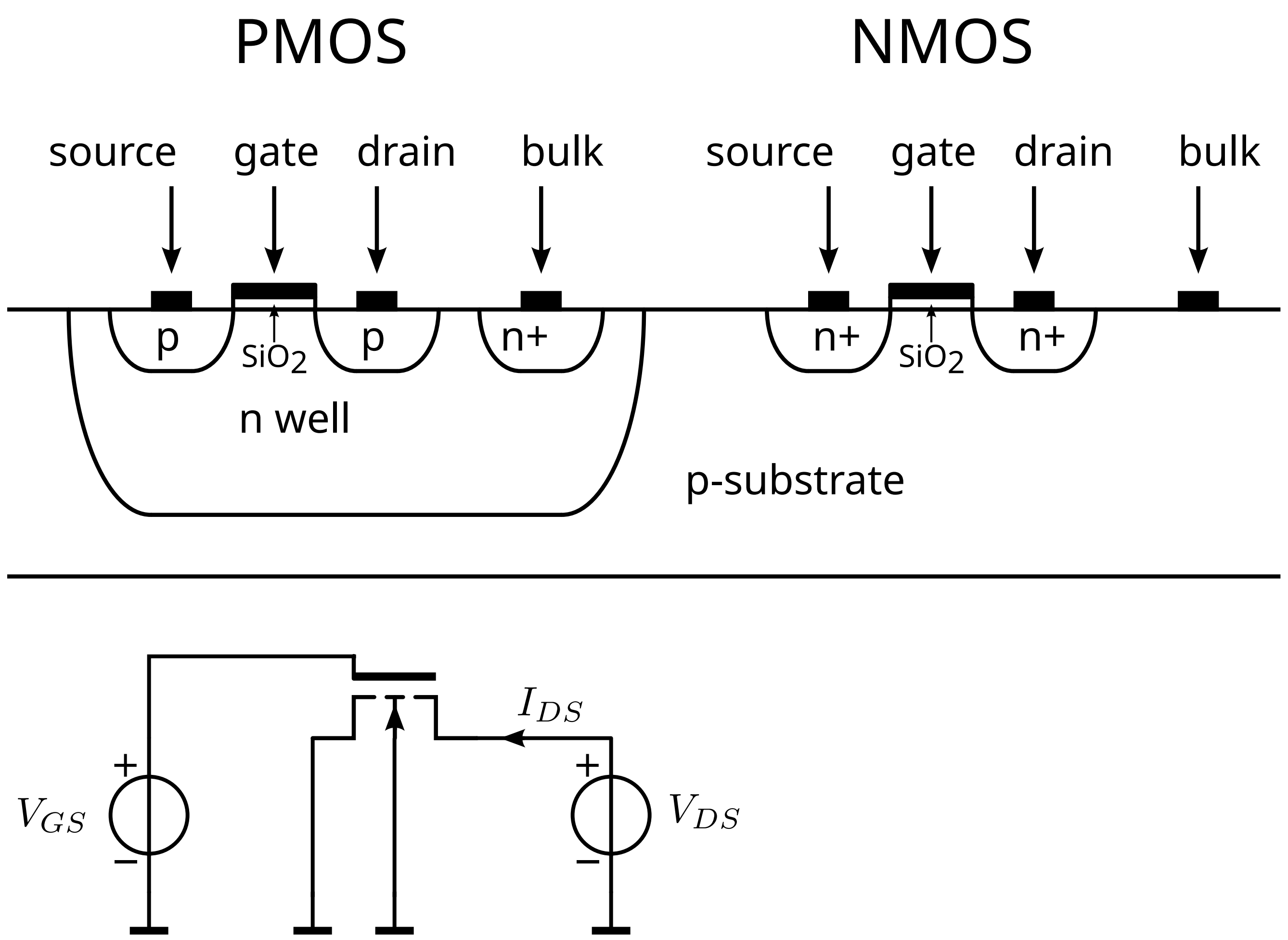
An n-channel is established between source and drain

Drain current increases quadratically with the gate-source voltage

capacitive coupling



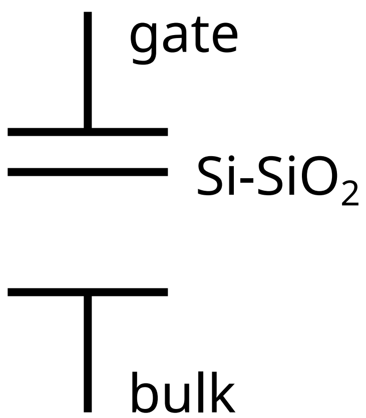
MOS operation



$V_{GS} = 0,\, V_{DS} > 0$ No current flow

$V_{GS} > 0,\, V_{DS} >> 0$

capacitive coupling



Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

Drain current increases exponentially with the gate-source voltage

$V_{GS} > V_{th},\, V_{DS} > V_{GS} - V_{th}$

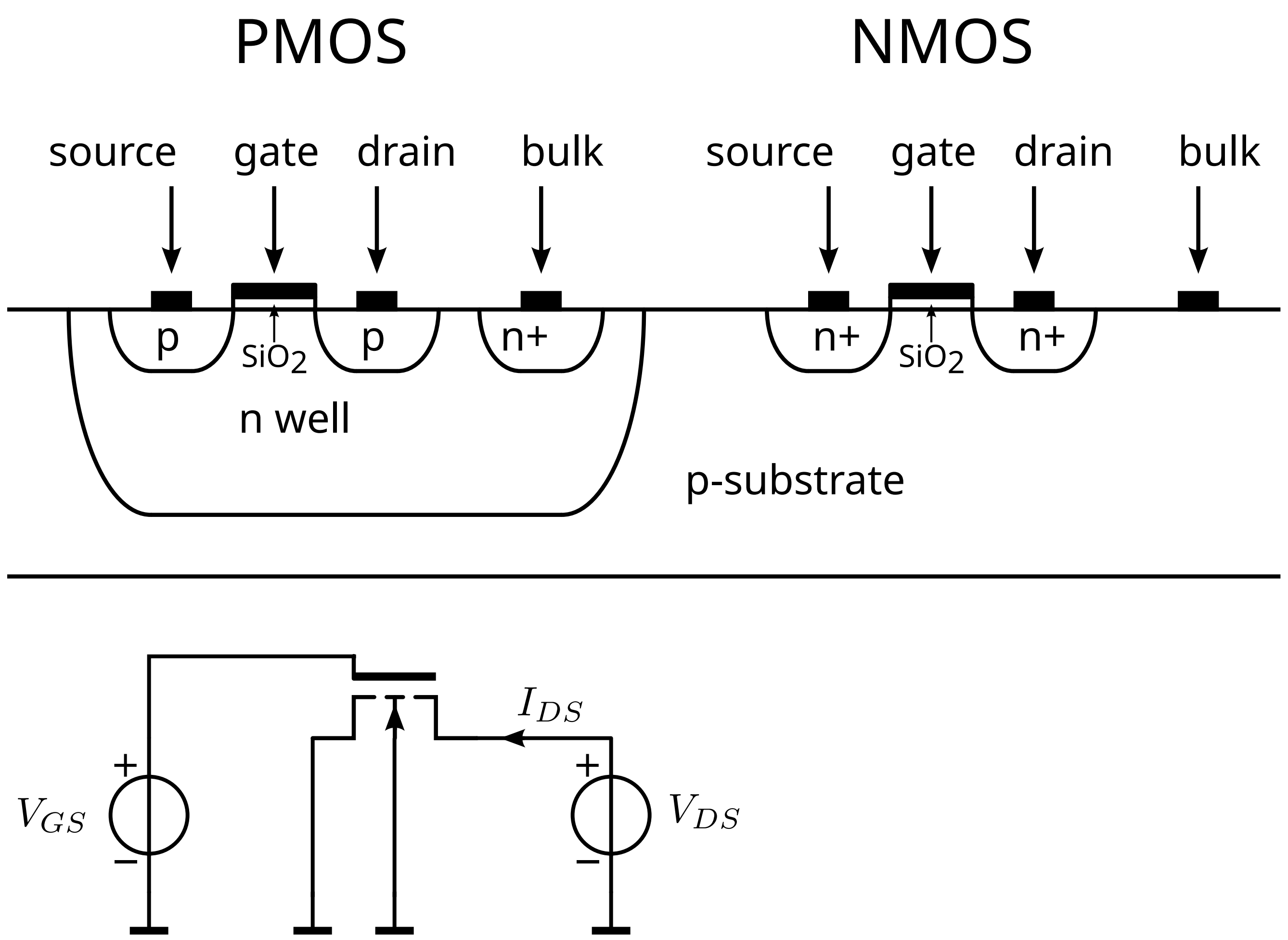
An n-channel is established between source and drain

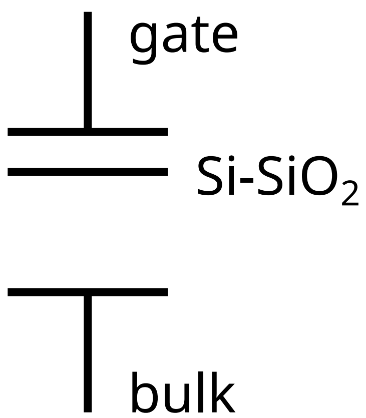
Drain current increases quadratically with the gate-source voltage

Drain-source voltage dependency

Channel length modulation (CLM)

MOS operation





$V_{GS} = 0,\ V_{DS} > 0$ No current flow

$V_{GS} > 0,\ V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

Drain current increases exponentially with the gate-source voltage

$V_{GS} > V_{th},\ V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

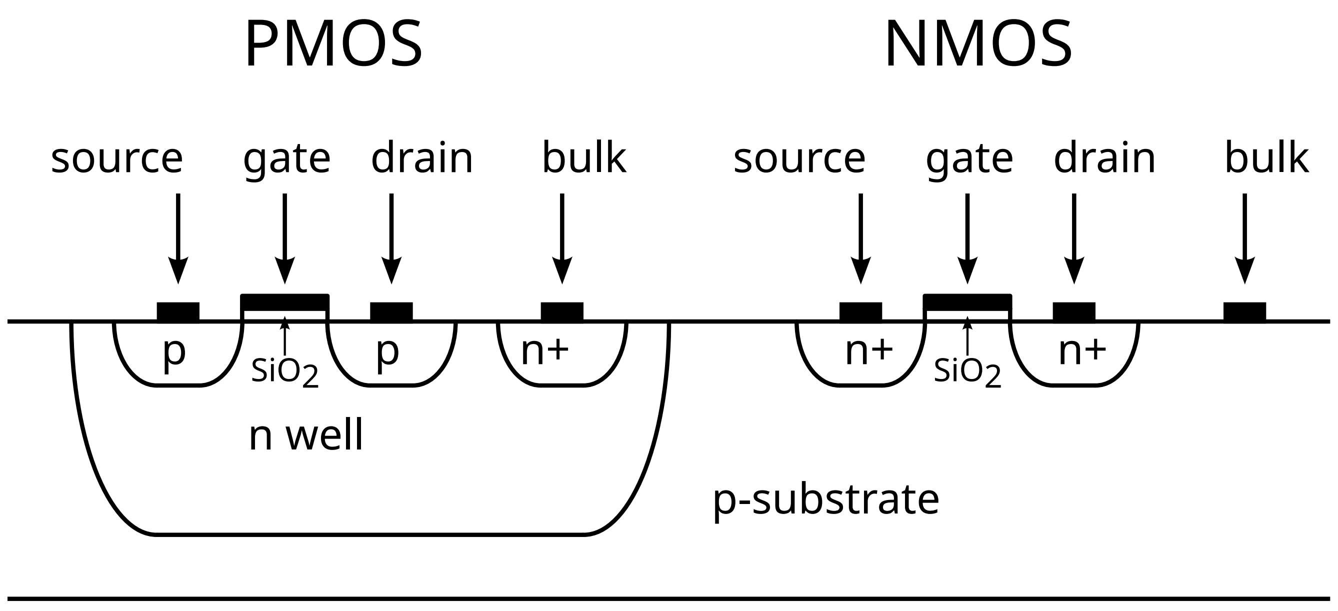
Drain current increases quadratically with the gate-source voltage

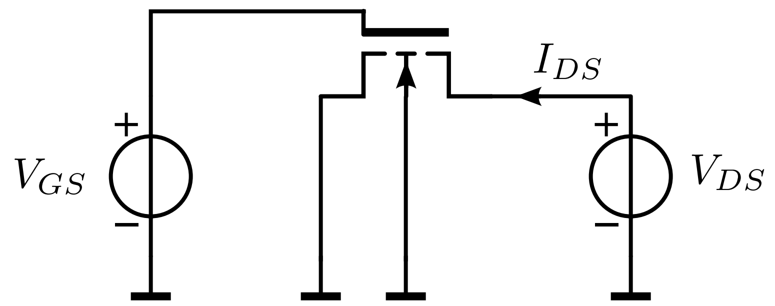
Drain-source voltage dependency

Channel length modulation (CLM)

Drain current increases with drain-source voltage

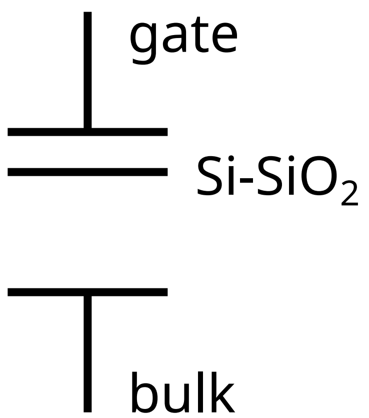
MOS operation





$V_{GS} = 0,\, V_{DS} > 0$ No current flow

capacitive
coupling



$V_{GS} > 0,\, V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

Drain current increases exponentially with the gate-source voltage

$V_{GS} > V_{th},\, V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

Drain current increases quadratically with the gate-source voltage

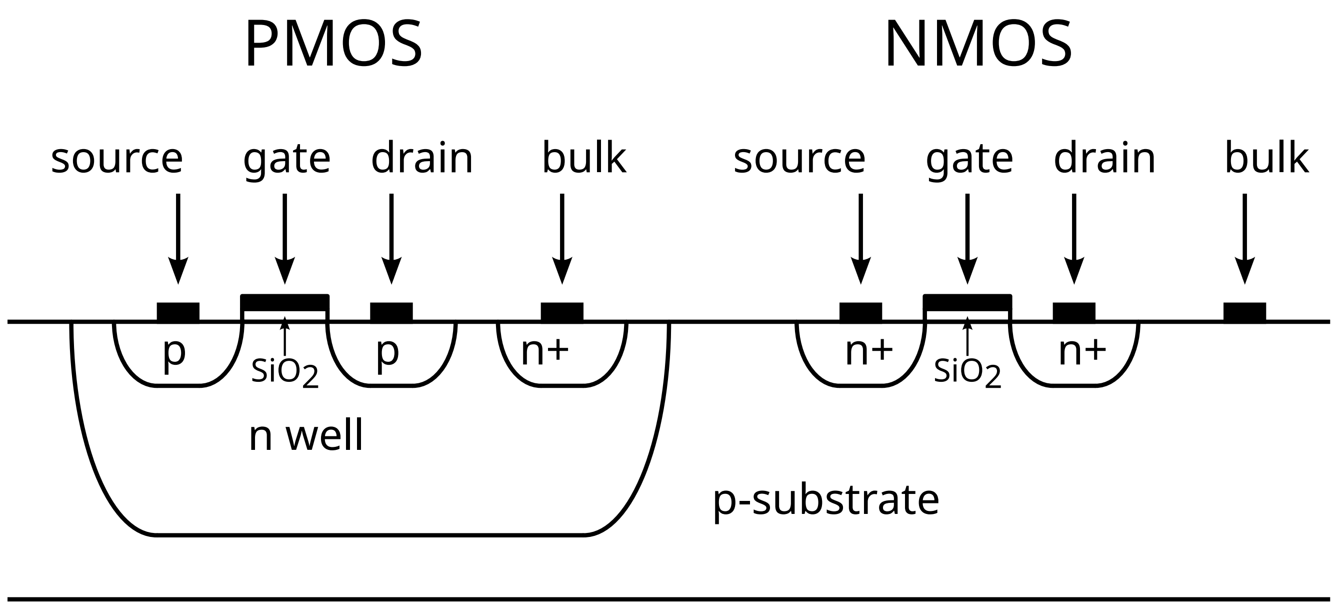
Drain-source voltage dependency

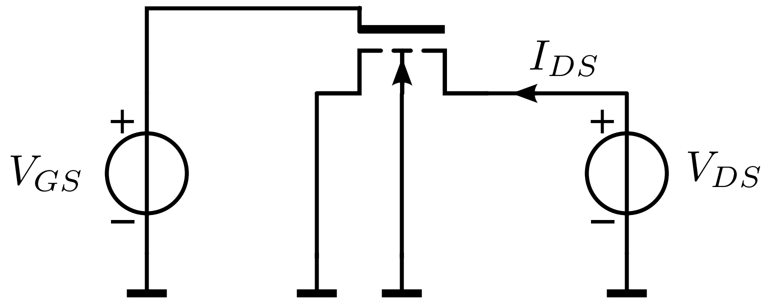
Channel length modulation (CLM)

Drain current increases with drain-source voltage

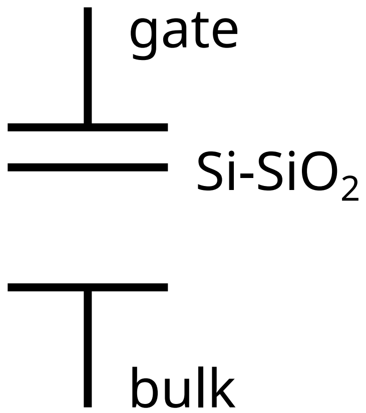
Breakdown

MOS operation





capacitive coupling



$V_{GS} = 0,\, V_{DS} > 0$ No current flow

$V_{GS} > 0,\, V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

Drain current increases exponentially with the gate-source voltage

$V_{GS} > V_{th},\, V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

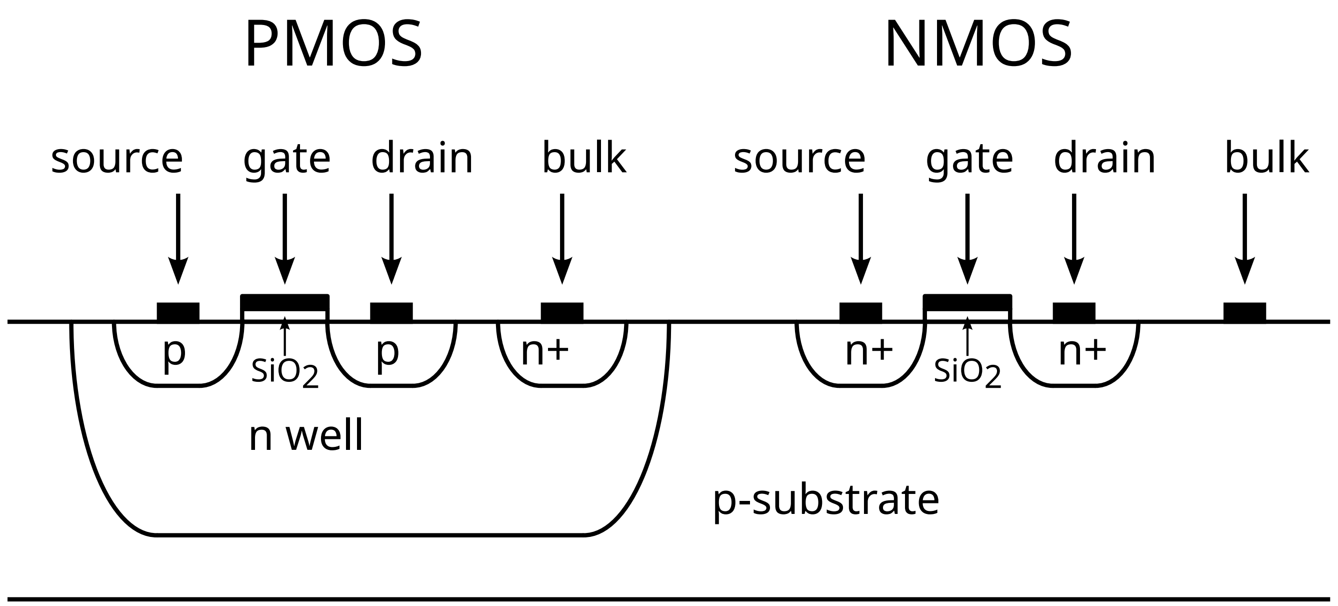
Drain current increases quadratically with the gate-source voltage

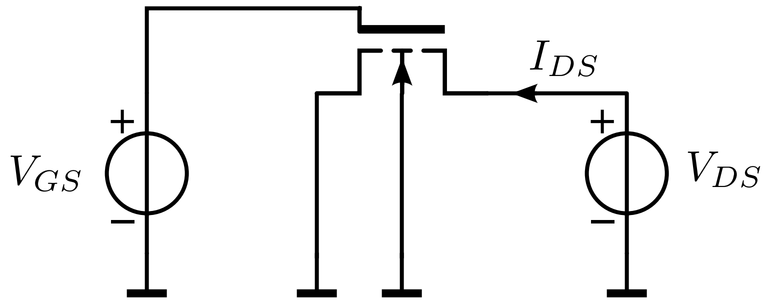
Drain-source voltage dependency

- Channel length modulation (CLM)
  - Drain current increases with drain-source voltage
- Breakdown

Short channel effects

MOS operation





$V_{GS} = 0,\, V_{DS} > 0$ No current flow

$V_{GS} > 0,\, V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

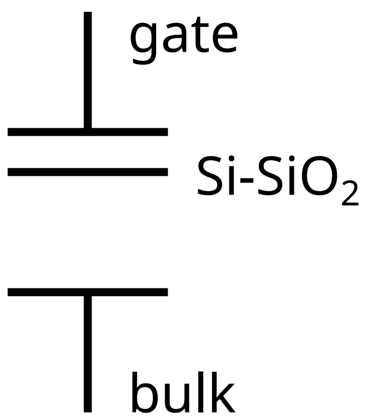
Drain current increases exponentially with the gate-source voltage

$V_{GS} > V_{th},\, V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

Drain current increases quadratically with the gate-source voltage

capacitive coupling



Drain-source voltage dependency

Channel length modulation (CLM)

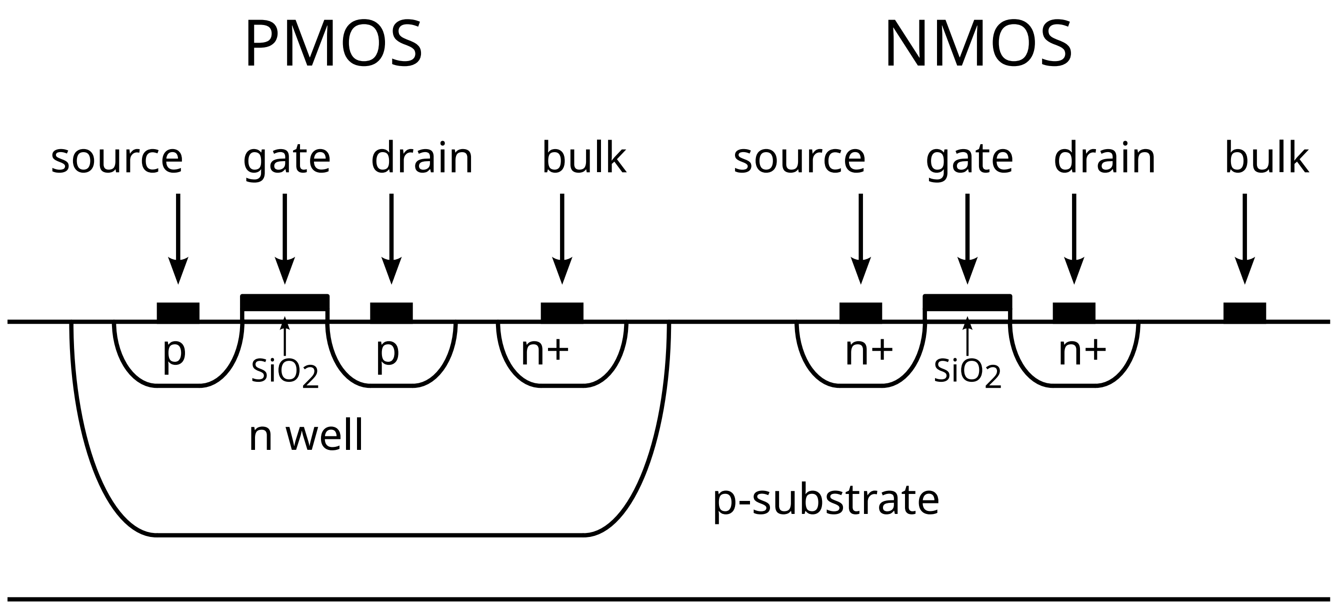
Drain current increases with drain-source voltage

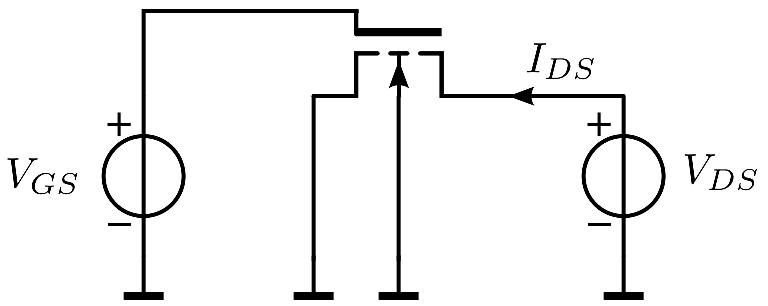
Breakdown

Short channel effects

Vertical field mobility reduction (VFMR)

MOS operation





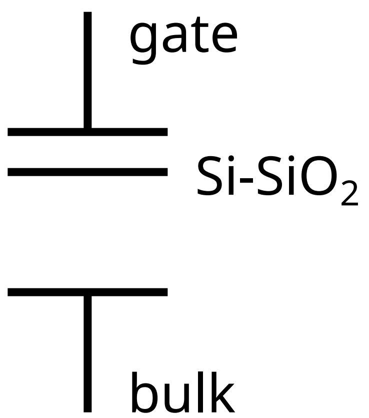
$V_{GS} = 0,\ V_{DS} > 0$ No current flow

$V_{GS} > 0,\ V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

Drain current increases exponentially with the gate-source voltage

capacitive coupling



$V_{GS} > V_{th},\ V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

Drain current increases quadratically with the gate-source voltage

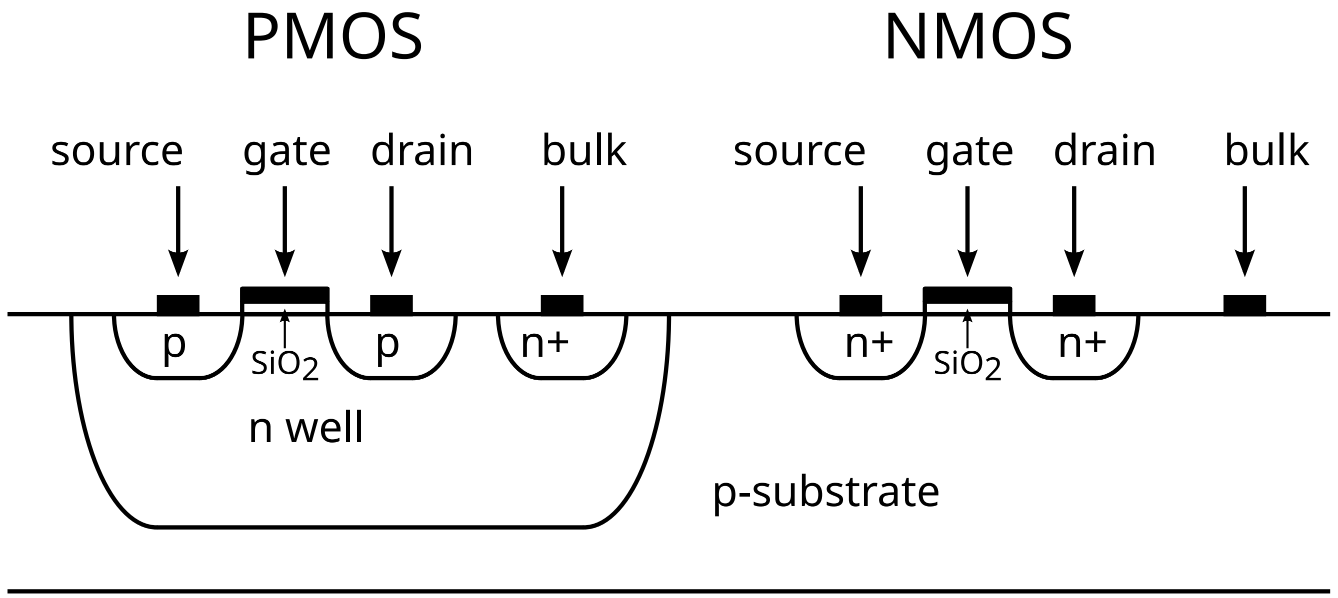
Drain-source voltage dependency

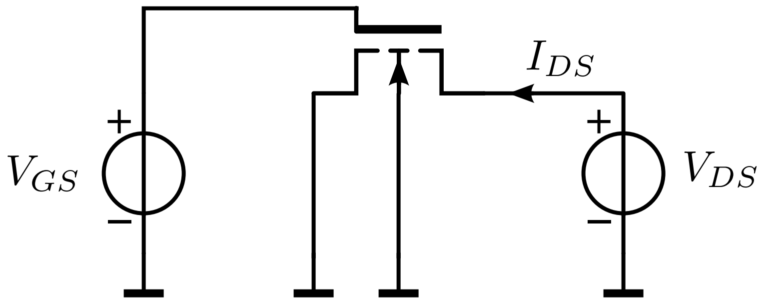
- Channel length modulation (CLM)
  - Drain current increases with drain-source voltage
- Breakdown

Short channel effects

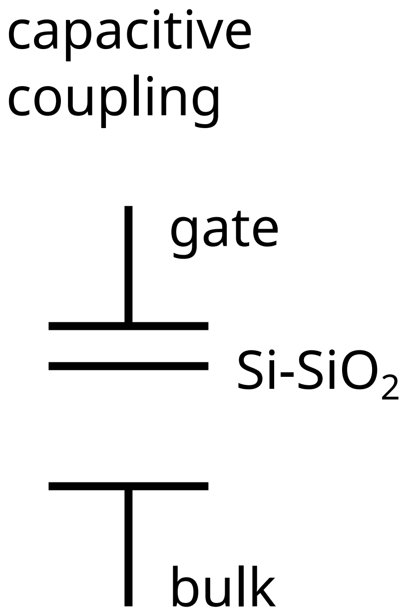
- Vertical field mobility reduction (VFMR)
- Velocity saturation (VS)

MOS operation





$V_{GS} = 0,\ V_{DS} > 0$ No current flow



$V_{GS} > 0,\ V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

Drain current increases exponentially with the gate-source voltage

$V_{GS} > V_{th},\ V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

Drain current increases quadratically with the gate-source voltage

Drain-source voltage dependency

Channel length modulation (CLM)

Drain current increases with drain-source voltage

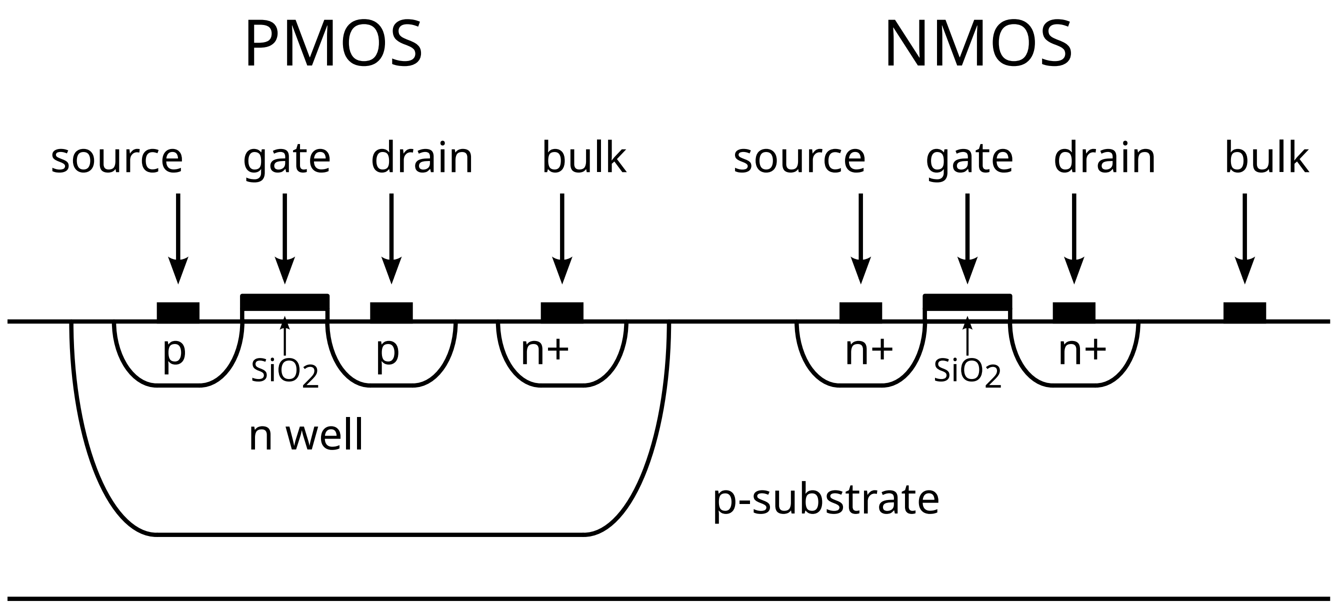
Breakdown

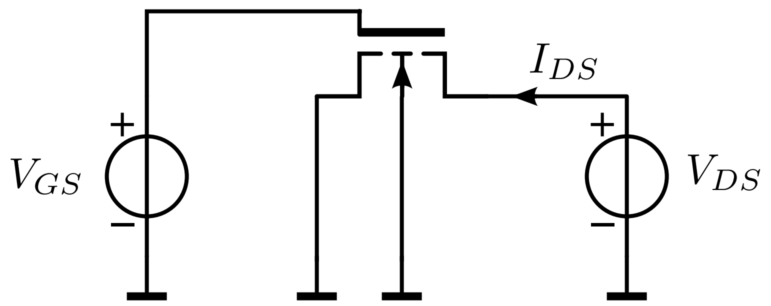
Short channel effects

Vertical field mobility reduction (VFMR)
Velocity saturation (VS)

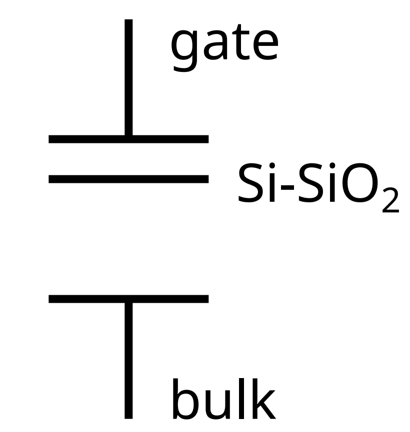
Drain current increases not longer quadratically with the gate-source voltage

MOS operation





$V_{GS} = 0,\ V_{DS} > 0$ No current flow



$V_{GS} > 0,\ V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

Drain current increases exponentially with the gate-source voltage

$V_{GS} > V_{th},\ V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

Drain current increases quadratically with the gate-source voltage

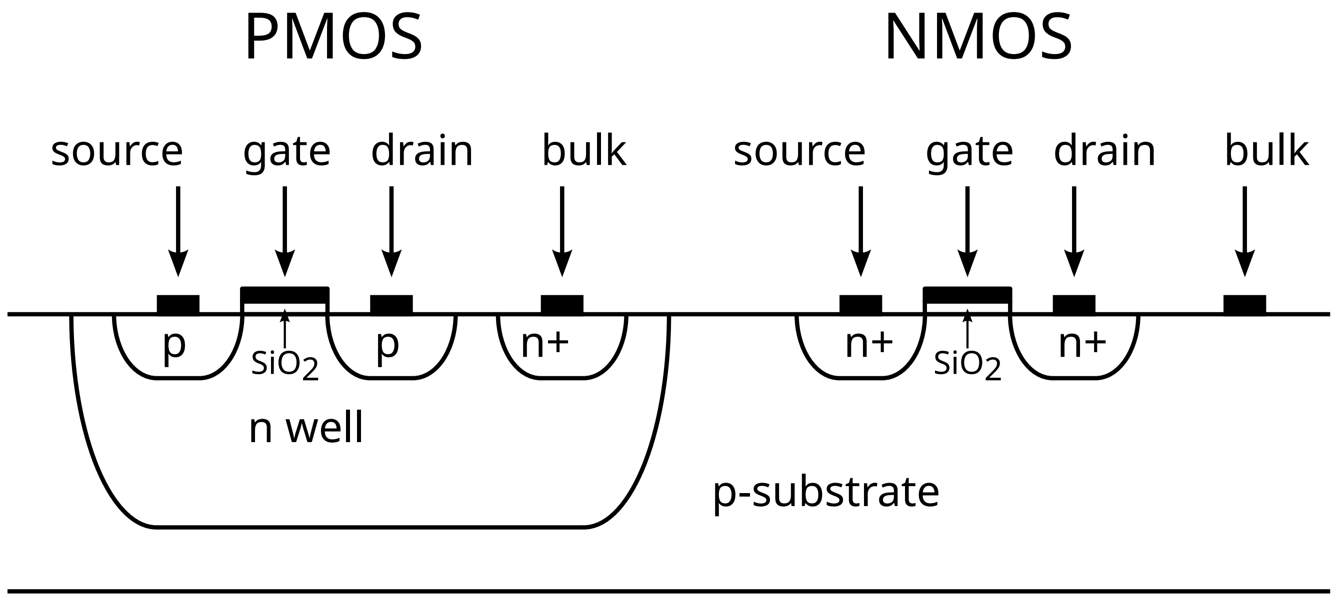
Drain-source voltage dependency

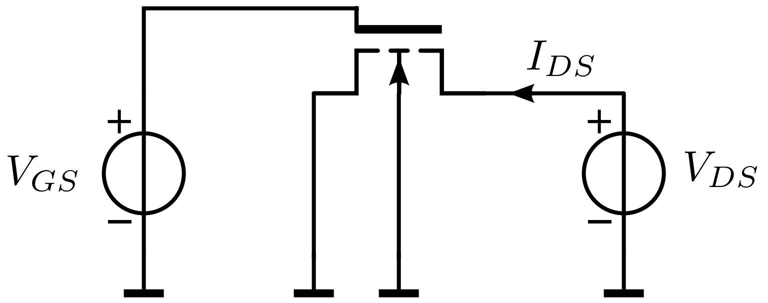
- Channel length modulation (CLM)
  - Drain current increases with drain-source voltage
- Breakdown

Short channel effects

- Vertical field mobility reduction (VFMR)
- Velocity saturation (VS)
  - Drain current increases not longer quadratically with the gate-source voltage
- Drain-induced barrier lowering (DIBL)

MOS operation





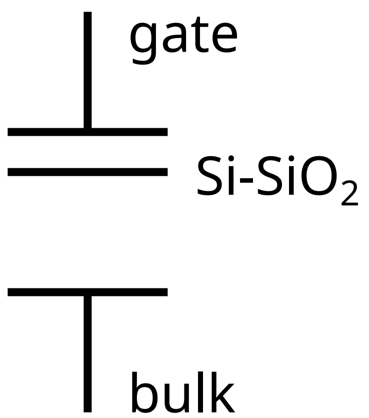
$V_{GS} = 0,\ V_{DS} > 0$ No current flow

$V_{GS} > 0,\ V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

Drain current increases exponentially with the gate-source voltage

capacitive coupling



$V_{GS} > V_{th},\ V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

Drain current increases quadratically with the gate-source voltage

Drain-source voltage dependency

Channel length modulation (CLM)

Drain current increases with drain-source voltage

Breakdown

Short channel effects

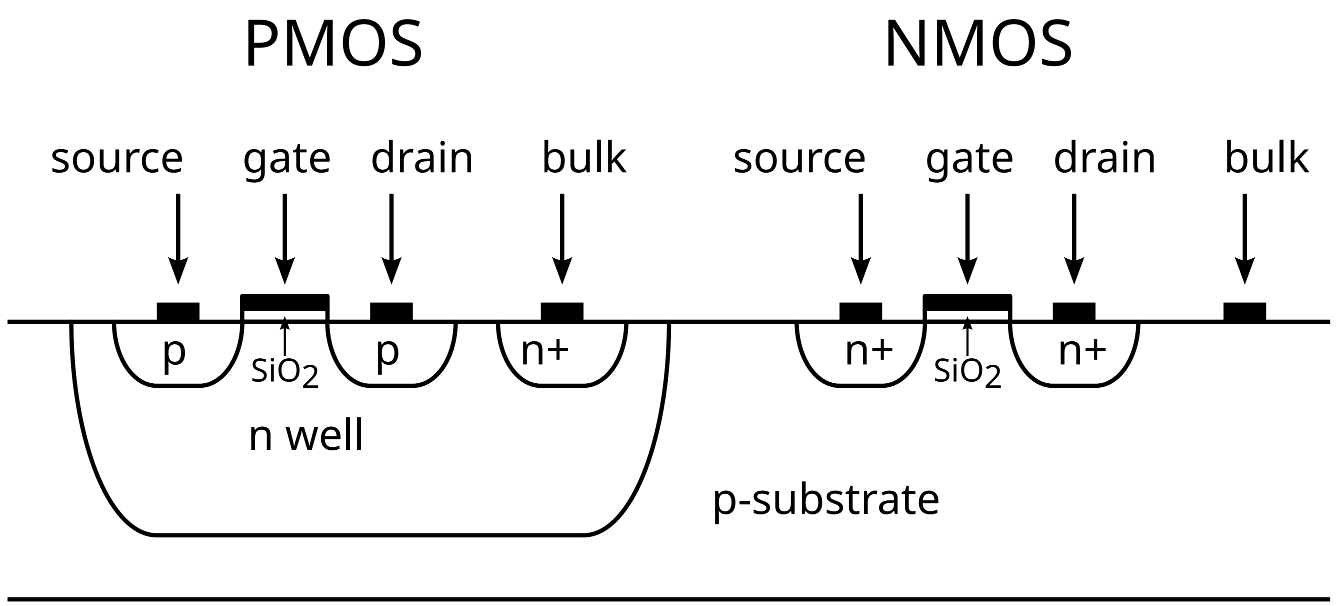
Vertical field mobility reduction (VFMR)
Velocity saturation (VS)

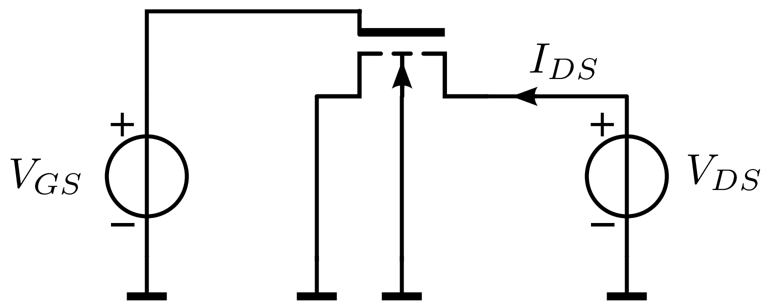
Drain current increases not longer quadratically with the gate-source voltage

Drain-induced barrier lowering (DIBL)

Capacitive coupling increases:

MOS operation





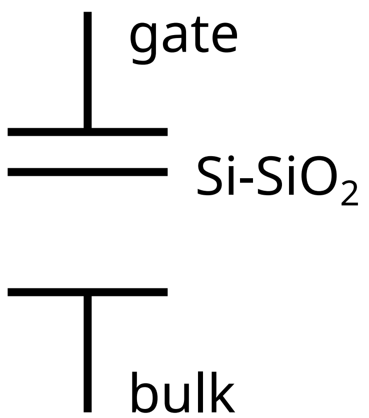
$V_{GS} = 0,\ V_{DS} > 0$ No current flow

$V_{GS} > 0,\ V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

Drain current increases exponentially with the gate-source voltage

capacitive coupling



$V_{GS} > V_{th},\ V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

Drain current increases quadratically with the gate-source voltage

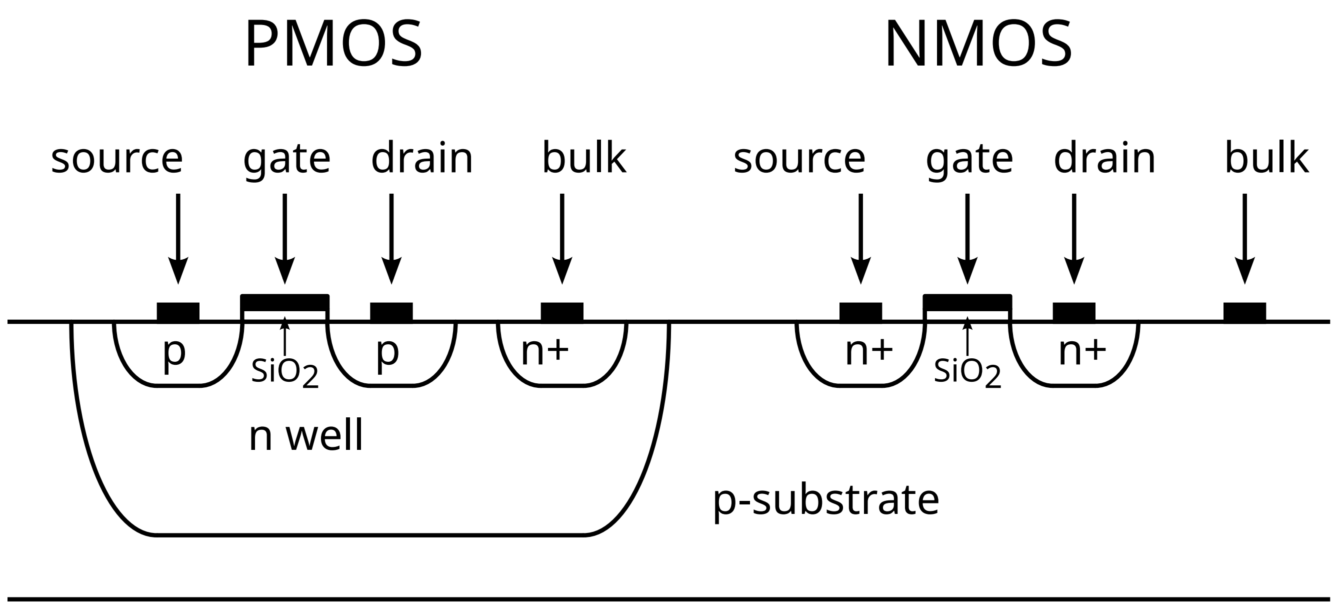
Drain-source voltage dependency

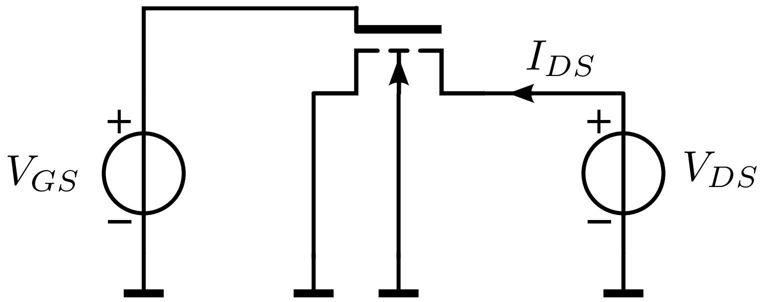
- Channel length modulation (CLM)
  - Drain current increases with drain-source voltage
- Breakdown

Short channel effects

- Vertical field mobility reduction (VFMR)
- Velocity saturation (VS)
  - Drain current increases not longer quadratically with the gate-source voltage
- Drain-induced barrier lowering (DIBL)
  - Capacitive coupling increases:
    Drain current increases

MOS operation





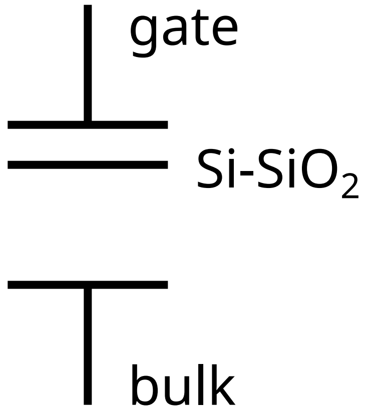
$V_{GS} = 0,\, V_{DS} > 0$ No current flow

$V_{GS} > 0,\, V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

Drain current increases exponentially with the gate-source voltage

capacitive coupling



$V_{GS} > V_{th},\, V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

Drain current increases quadratically with the gate-source voltage

Drain-source voltage dependency

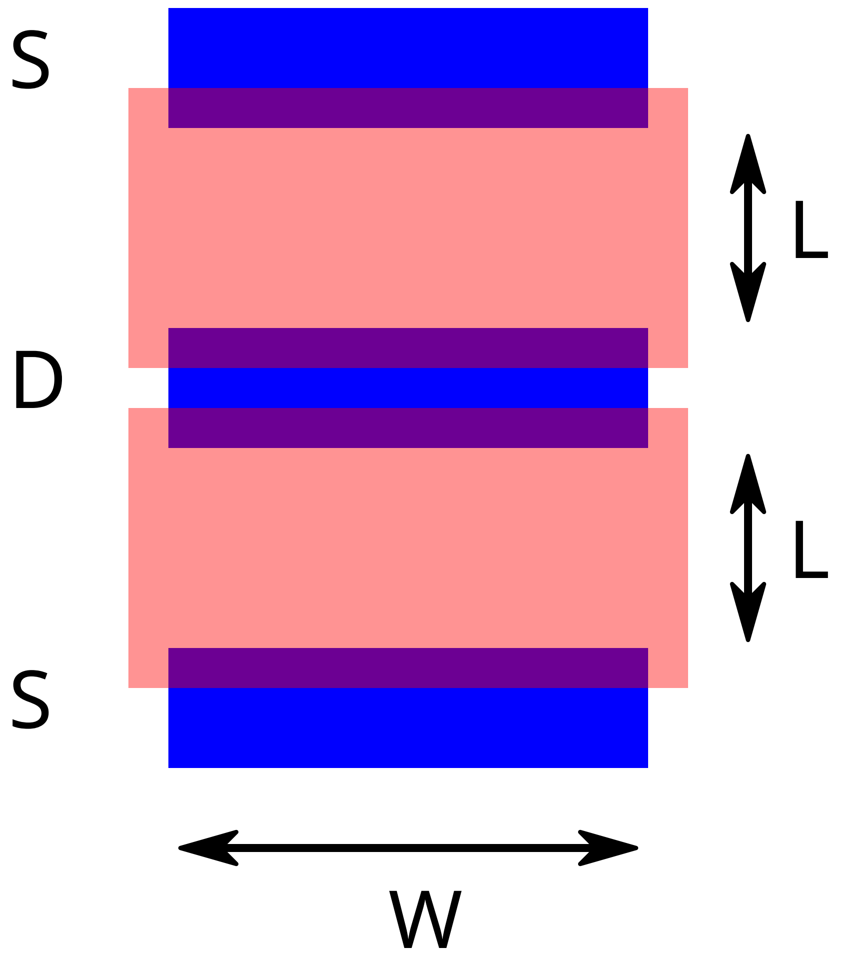
- Channel length modulation (CLM)
  - Drain current increases with drain-source voltage
- Breakdown

Short channel effects

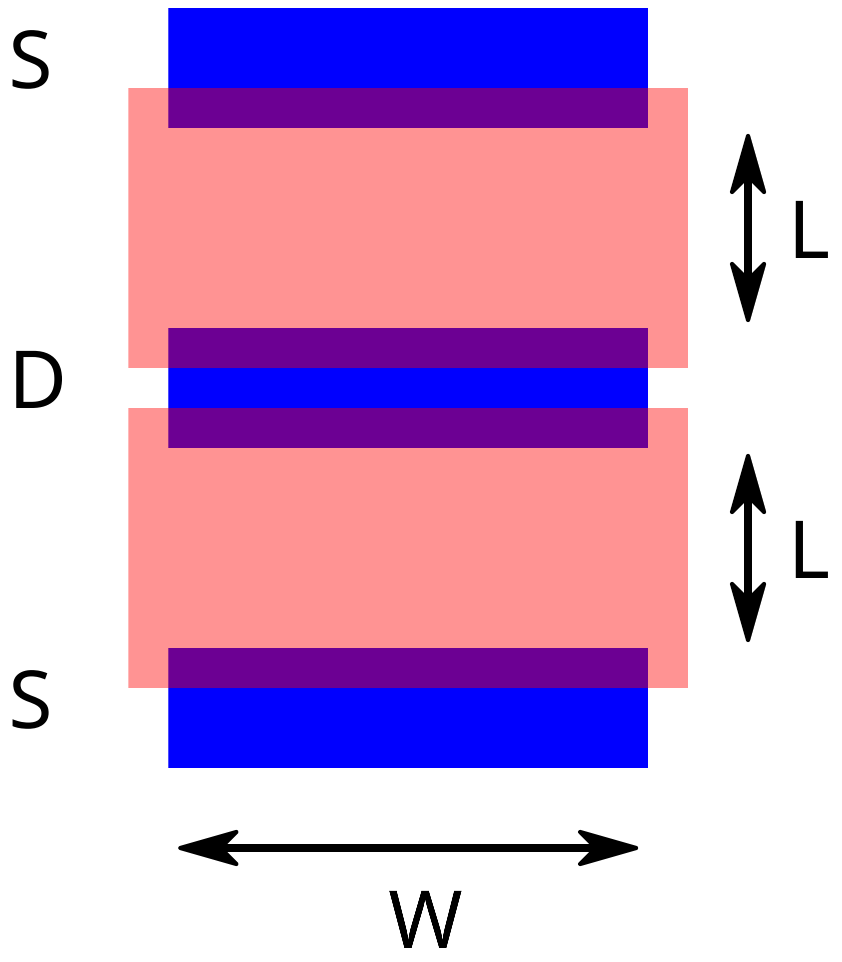
- Vertical field mobility reduction (VFMR)
- Velocity saturation (VS)
  - Drain current increases not longer quadratically with the gate-source voltage
- Drain-induced barrier lowering (DIBL)
  - Capacitive coupling increases:
    Drain current increases

MOS design

MOS design

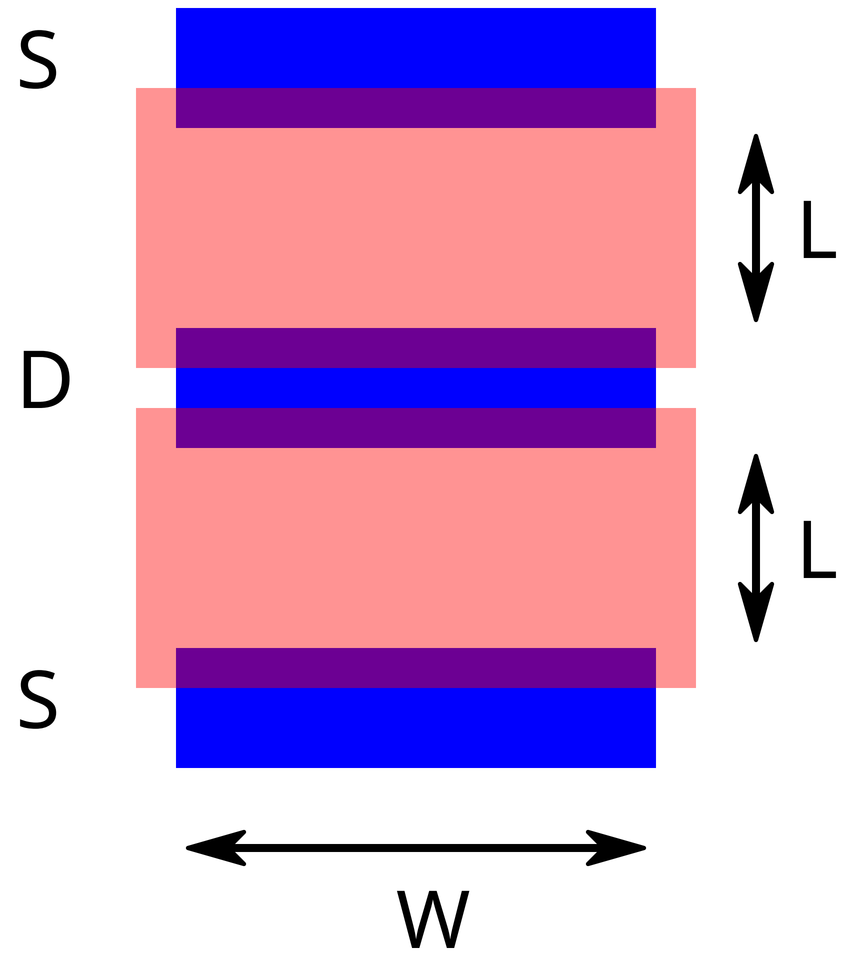


MOS design



Design question

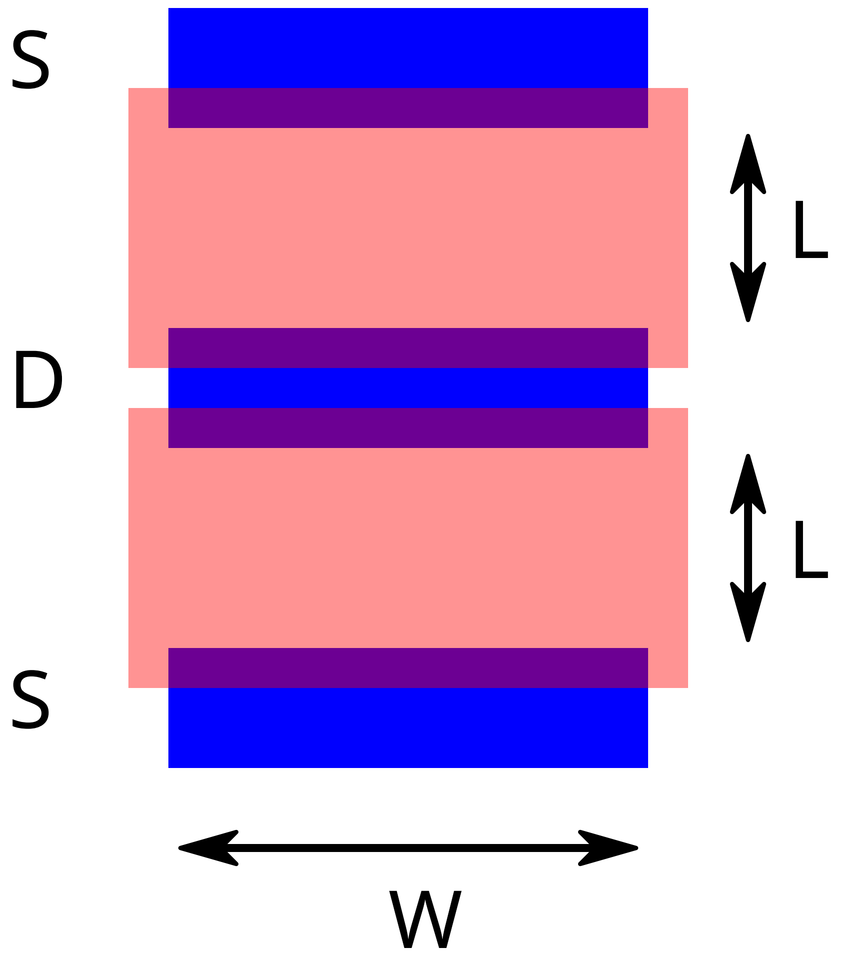
MOS design



Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

MOS design

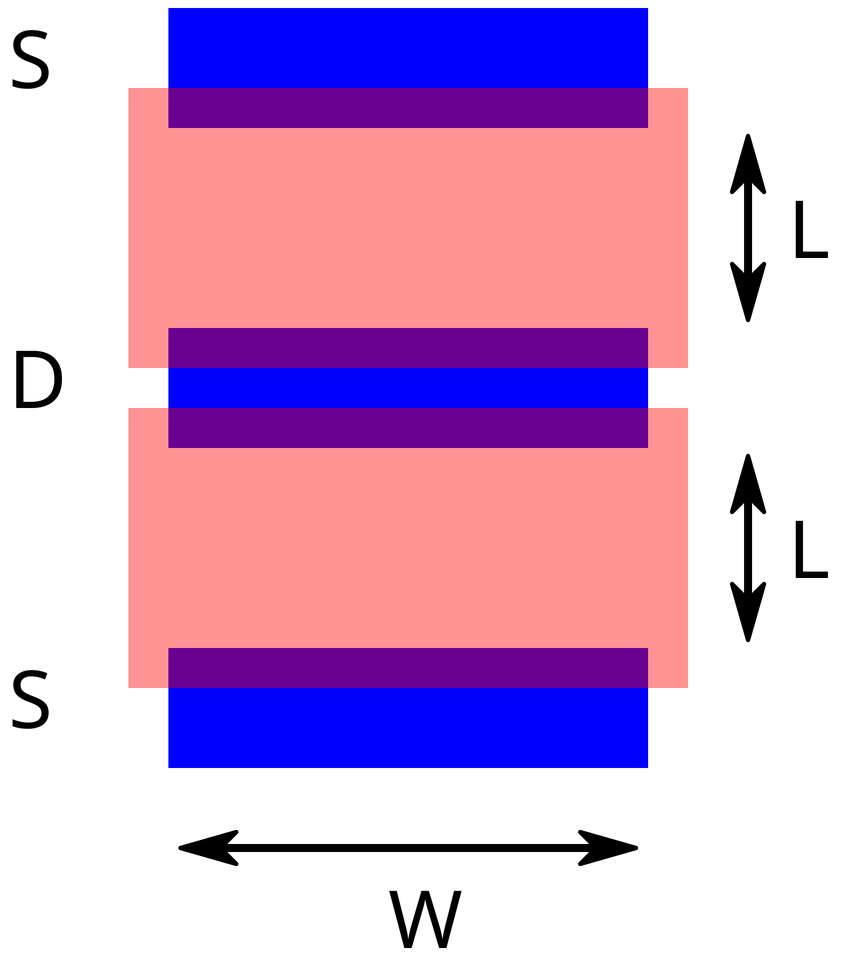


Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

MOS design



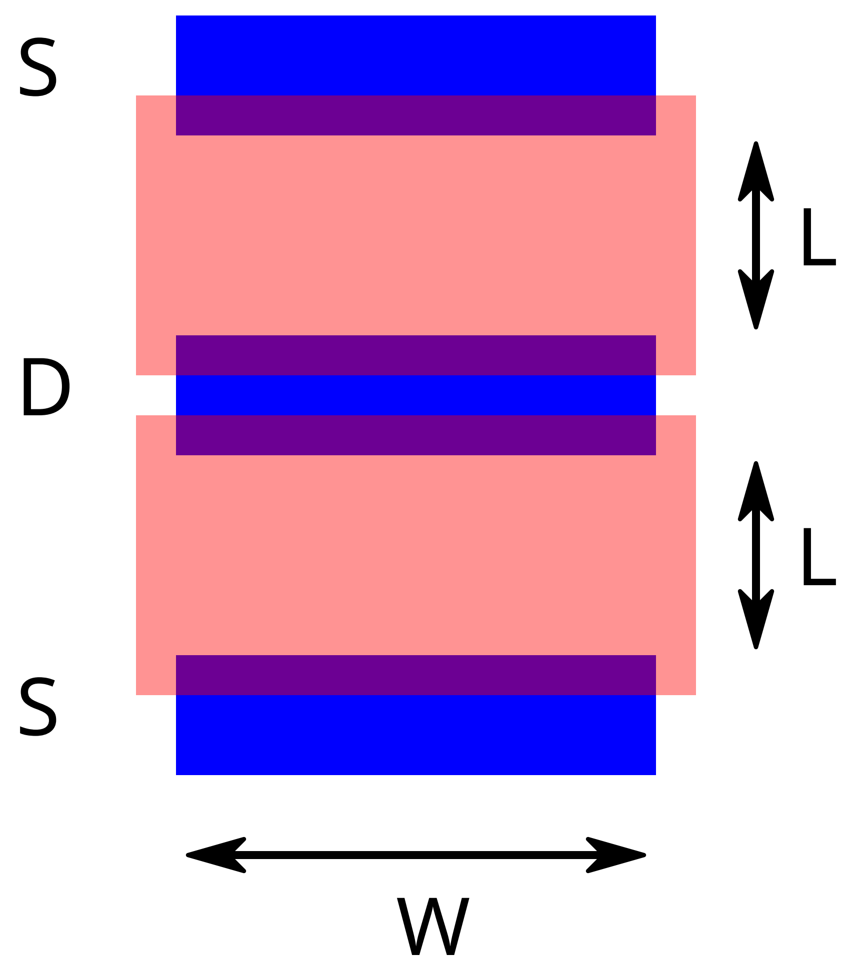
Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

Channel width

MOS design



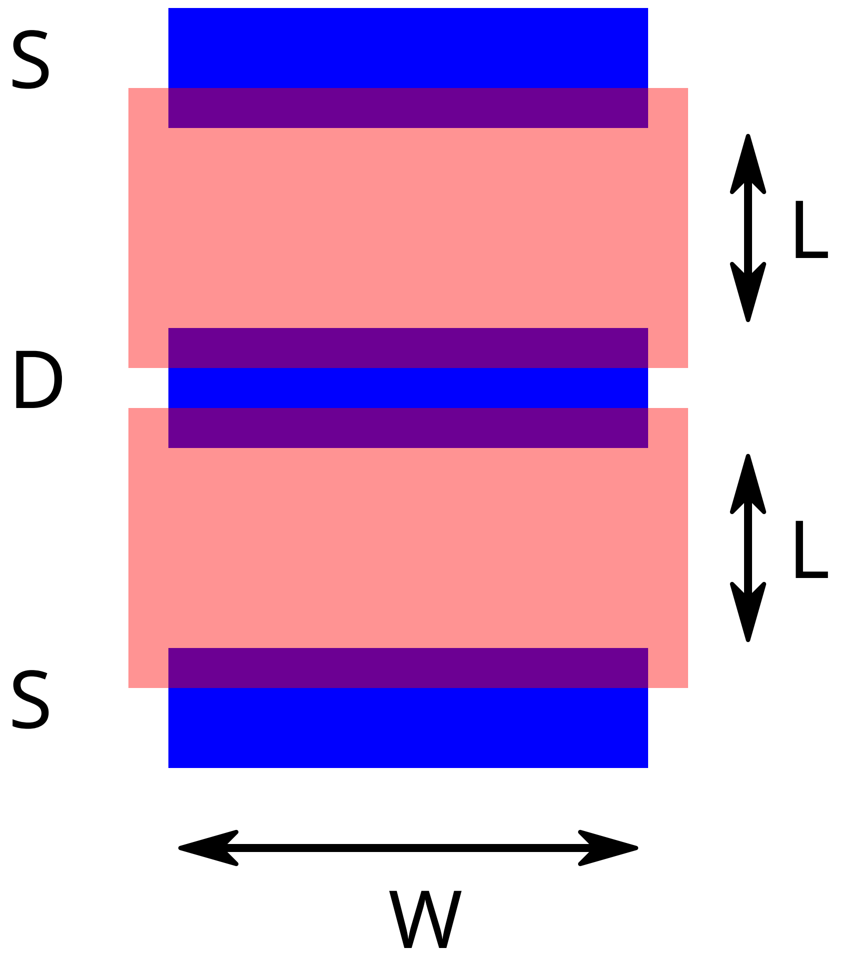
Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

Channel width
Channel length

MOS design



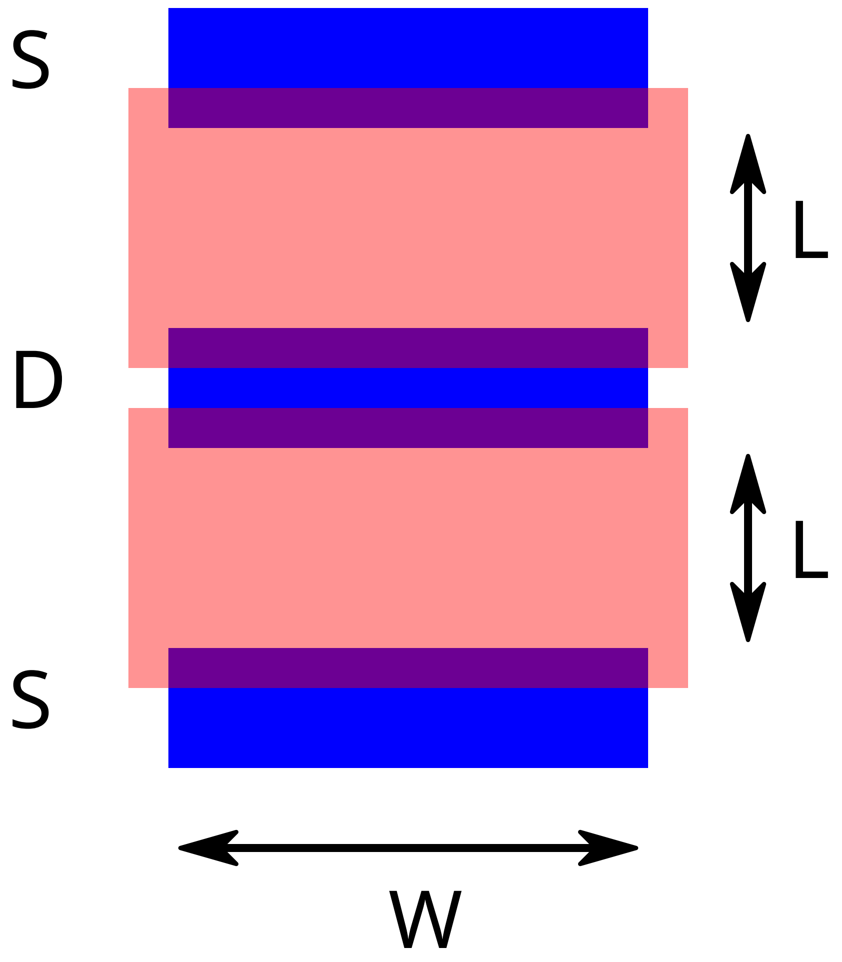
Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

Channel width
Channel length
Number of sections

MOS design



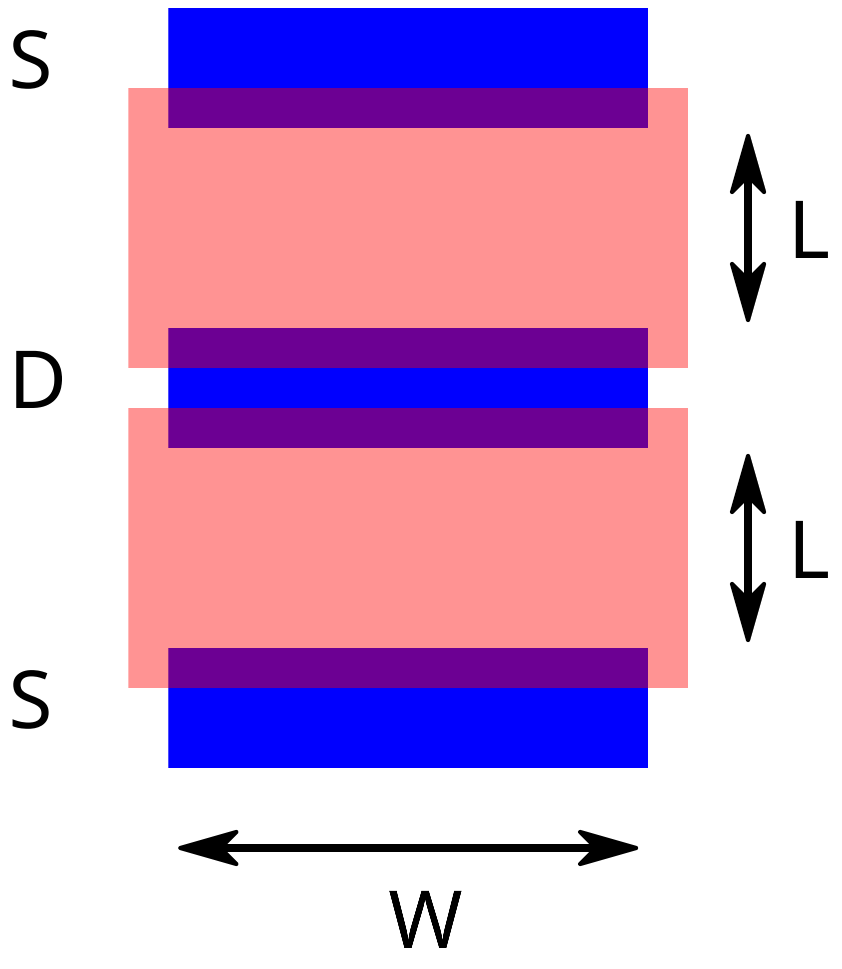
Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

Channel width
Channel length
Number of sections
Drain current

MOS design



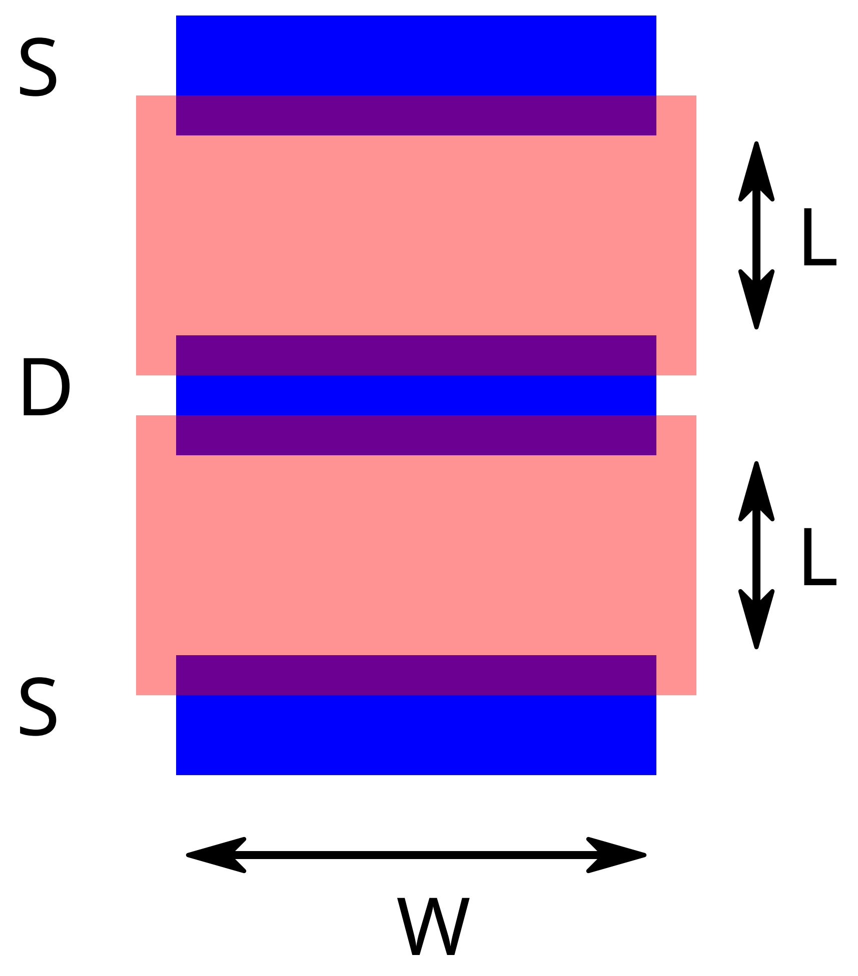
Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

Channel width
Channel length
Number of sections
Drain current
Drain-source voltage

MOS design



Design question

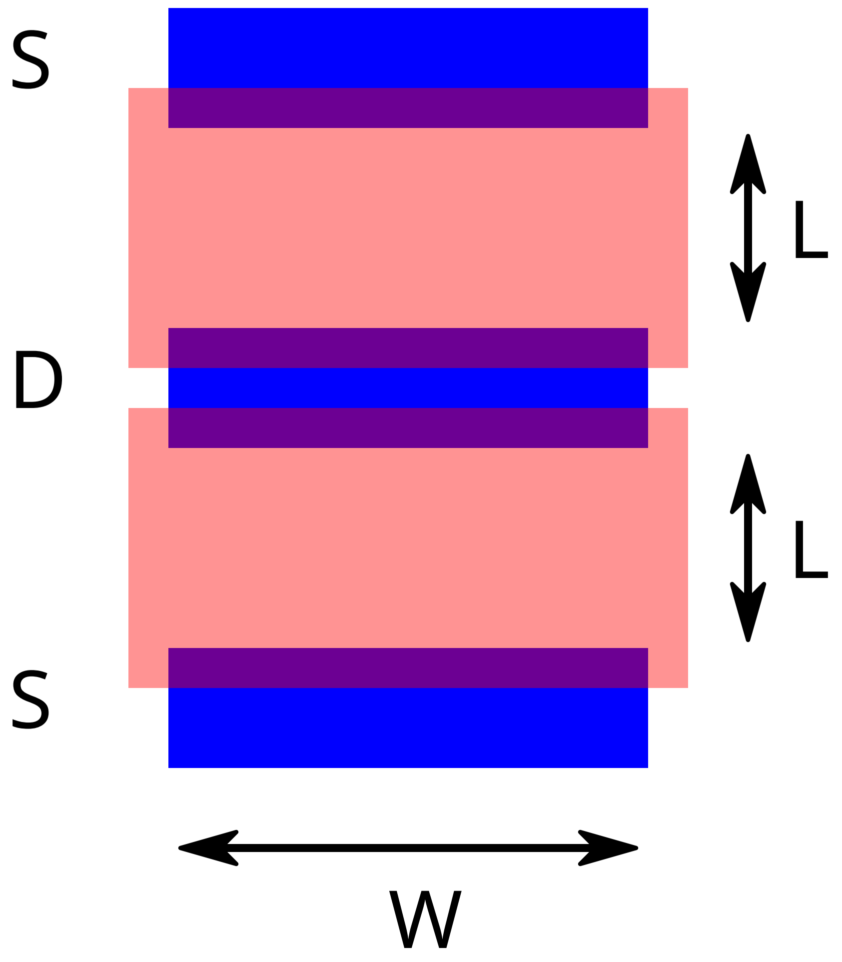
In which way do the performance parameters of a MOS transistor depend on its design parameters

Methods

Design parameters available to the designer

Channel width
Channel length
Number of sections
Drain current
Drain-source voltage

MOS design



Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

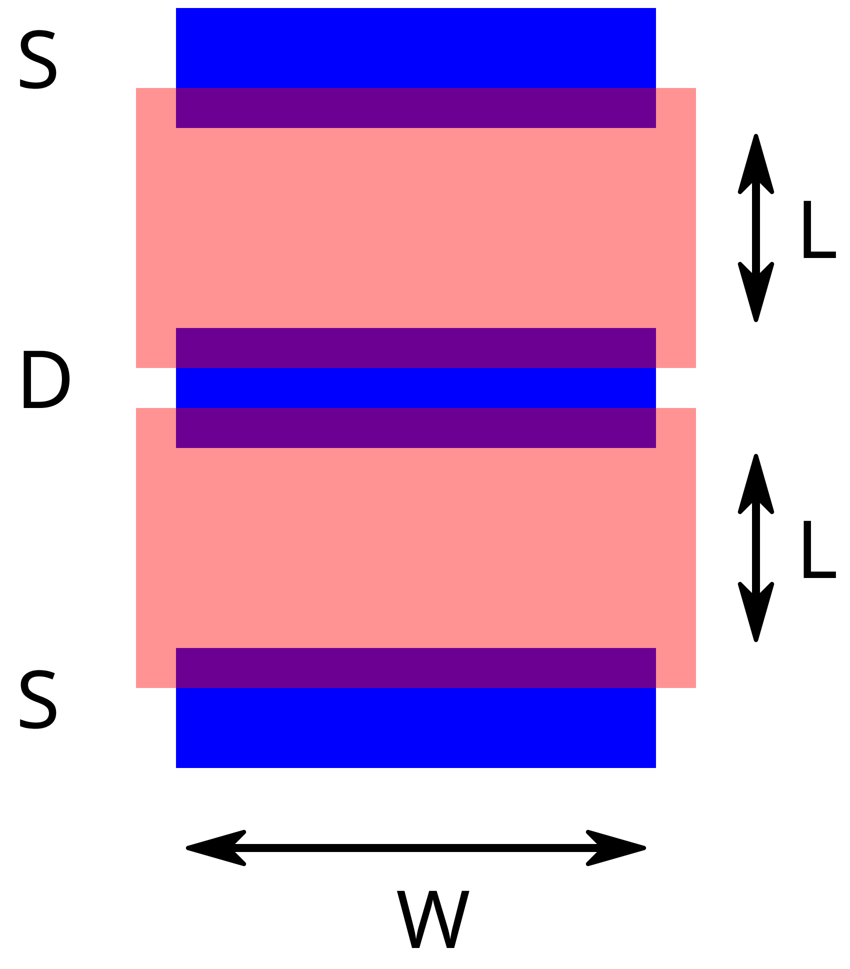
Design parameters available to the designer

Channel width
Channel length
Number of sections
Drain current
Drain-source voltage

Methods

Use a design manual with graphs and tables and scale devices

MOS design



Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

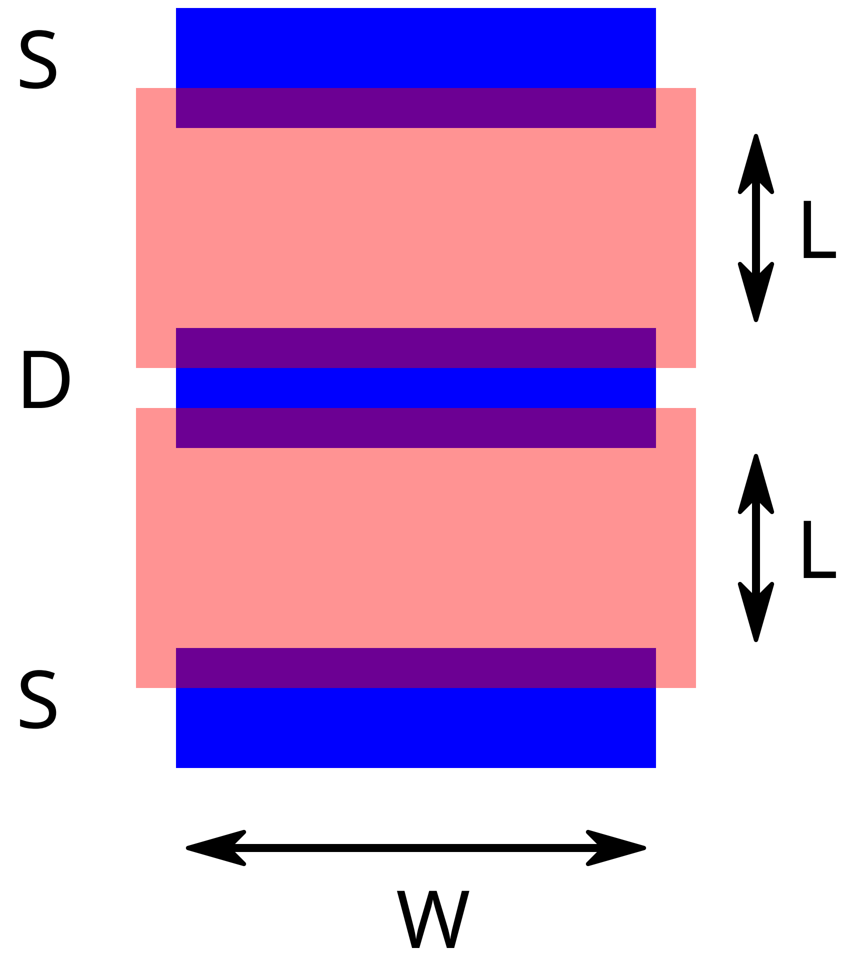
Channel width
Channel length
Number of sections
Drain current
Drain-source voltage

Methods

Use a design manual with graphs and tables and scale devices

Useful, but generally not all situations will be covered

MOS design



Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

Channel width
Channel length
Number of sections
Drain current
Drain-source voltage

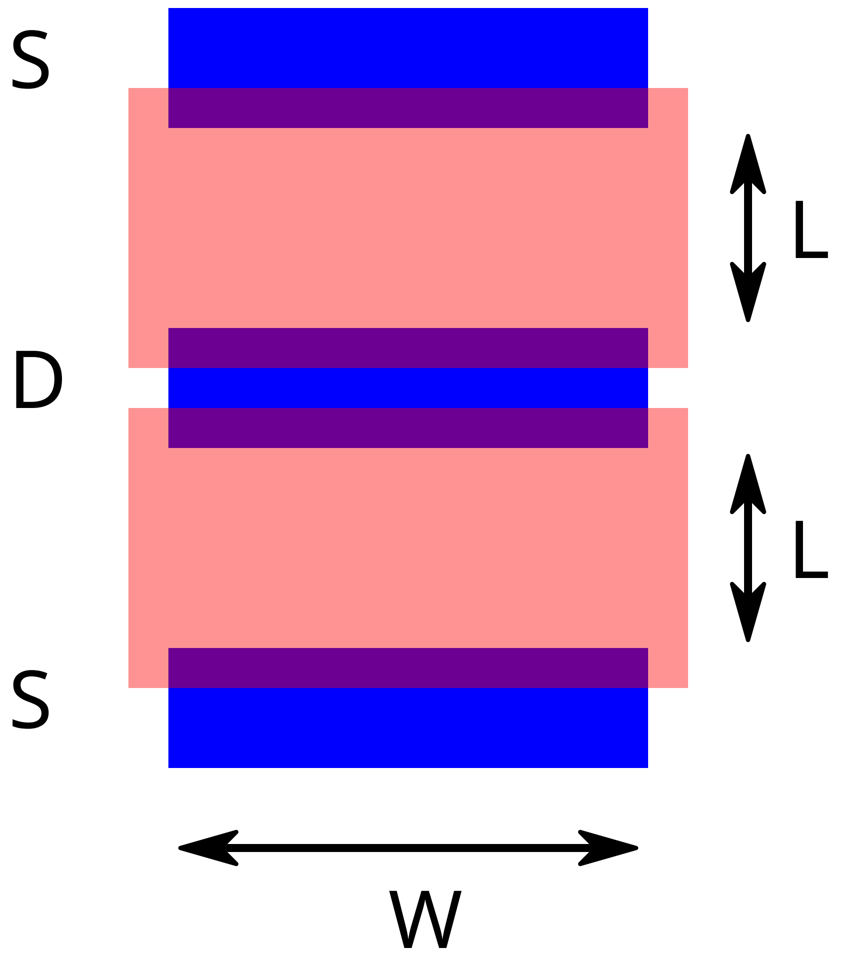
Methods

Use a design manual with graphs and tables and scale devices

Useful, but generally not all situations will be covered

Design a device and study its performance through simulation

MOS design



Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

Channel width
Channel length
Number of sections
Drain current
Drain-source voltage

Methods

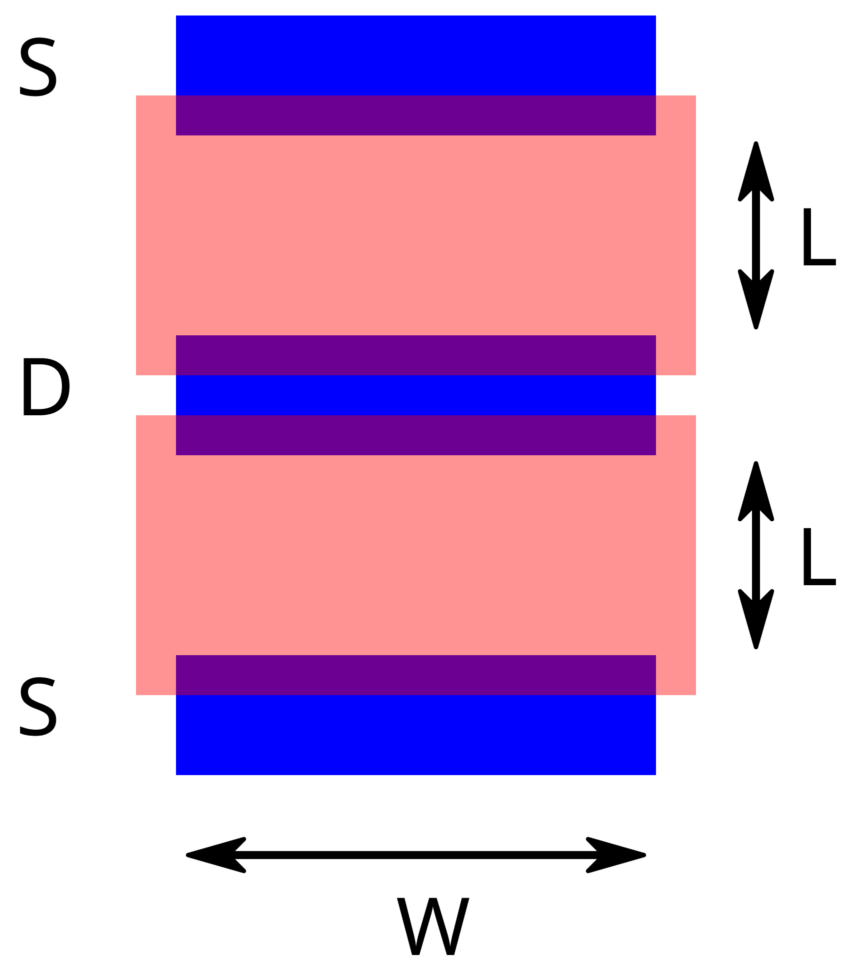
Use a design manual with graphs and tables and scale devices

- Useful, but generally not all situations will be covered

Design a device and study its performance through simulation

- Useful for finding DC operating conditions and small-signal model parameters

MOS design



Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

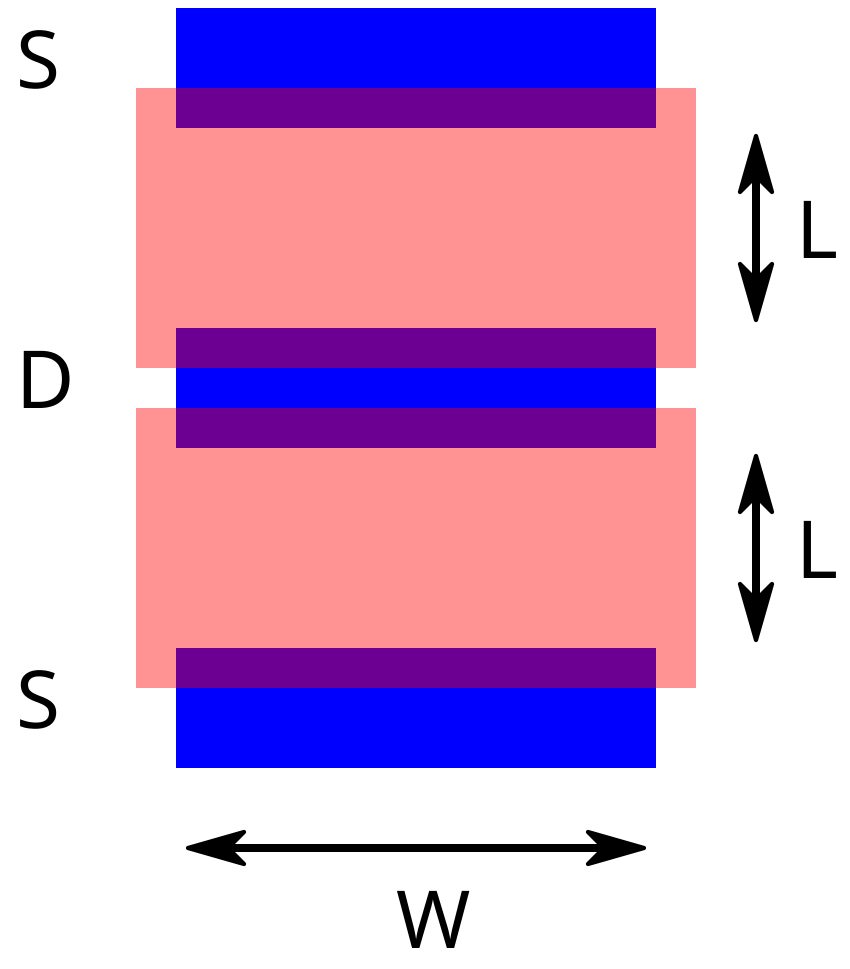
Design parameters available to the designer

Channel width
Channel length
Number of sections
Drain current
Drain-source voltage

Methods

- Use a design manual with graphs and tables and scale devices
  - Useful, but generally not all situations will be covered
- Design a device and study its performance through simulation
  - Useful for finding DC operating conditions and small-signal model parameters
  - Jupyter notebook tool

MOS design



Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

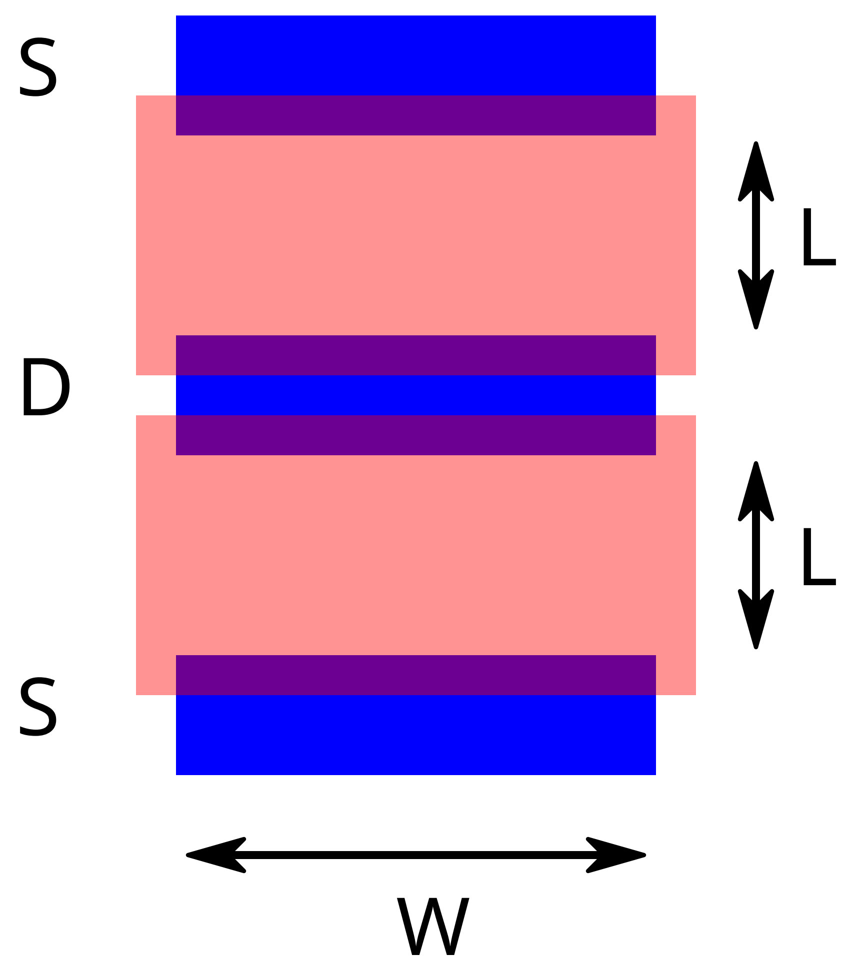
Design parameters available to the designer

- Channel width
- Channel length
- Number of sections
- Drain current
- Drain-source voltage

Methods

- Use a design manual with graphs and tables and scale devices
  - Useful, but generally not all situations will be covered
- Design a device and study its performance through simulation
  - Useful for finding DC operating conditions and small-signal model parameters
  - Jupyter notebook tool
- Use simplified design models

MOS design



Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

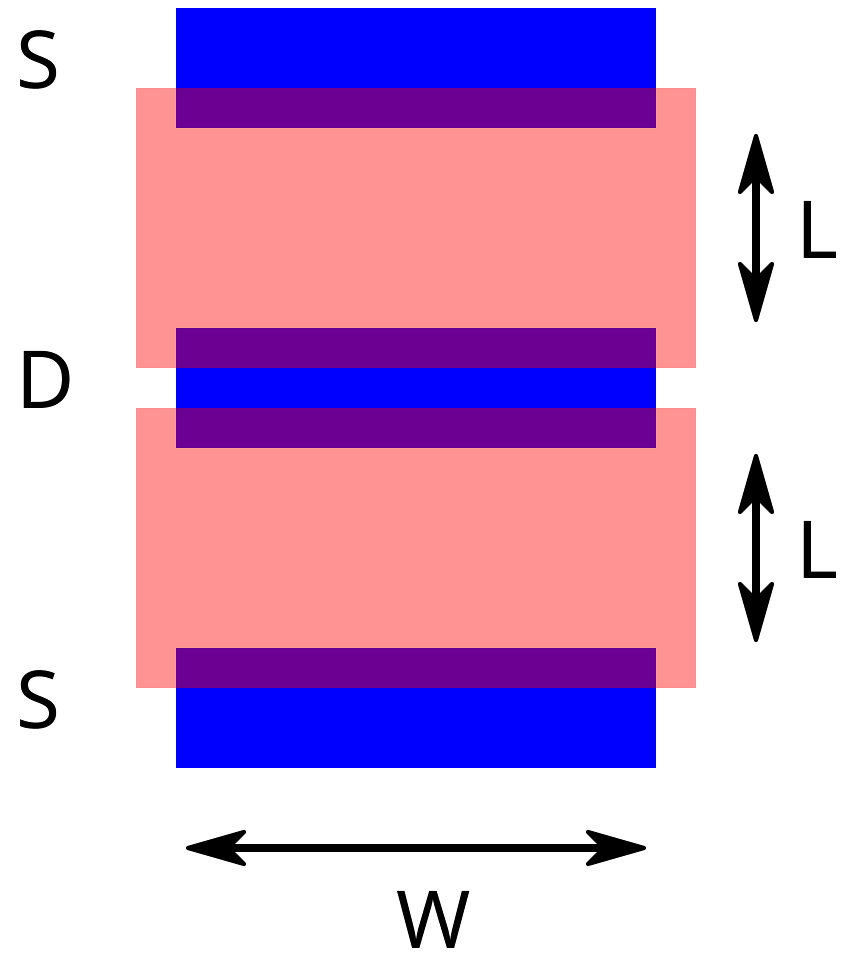
Design parameters available to the designer

Channel width
Channel length
Number of sections
Drain current
Drain-source voltage

Methods

- Use a design manual with graphs and tables and scale devices
  - Useful, but generally not all situations will be covered
- Design a device and study its performance through simulation
  - Useful for finding DC operating conditions and small-signal model parameters
  - Jupyter notebook tool
- Use simplified design models
  - Useful for design of small signal behavior: bandwidth frequency response and noise

MOS design



Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

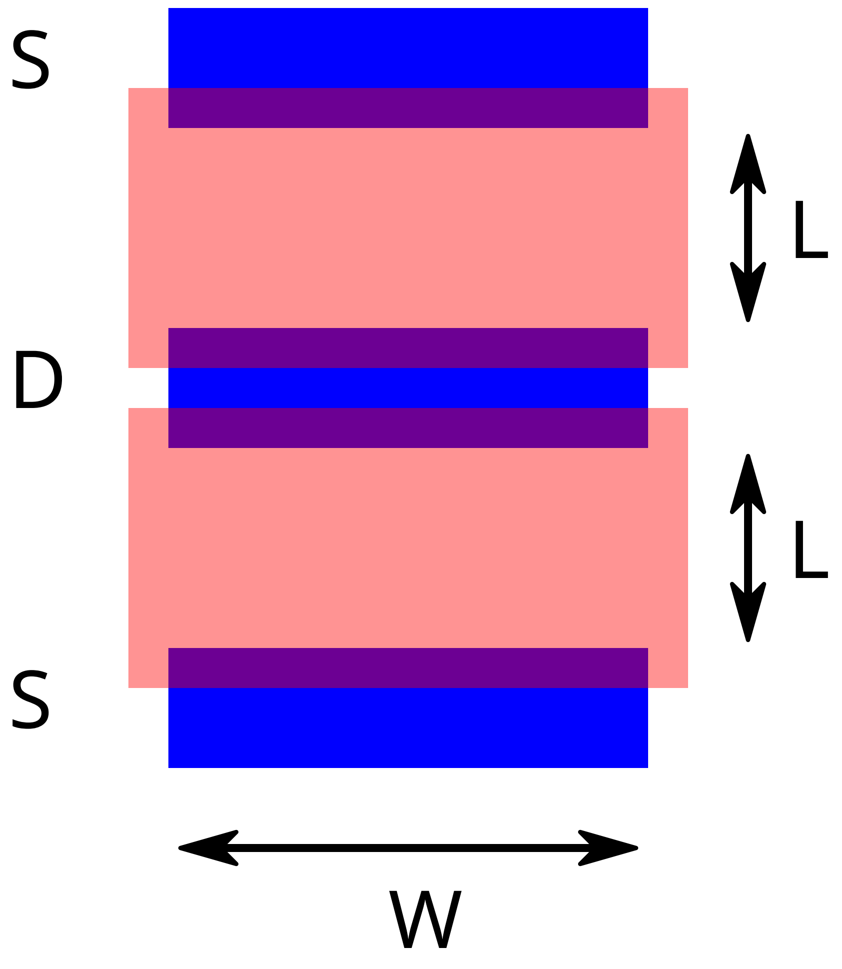
Design parameters available to the designer

Channel width
Channel length
Number of sections
Drain current
Drain-source voltage

Methods

- Use a design manual with graphs and tables and scale devices
  - Useful, but generally not all situations will be covered
- Design a device and study its performance through simulation
  - Useful for finding DC operating conditions and small-signal model parameters
  - Jupyter notebook tool
- Use simplified design models
  - Useful for design of small signal behavior: bandwidth frequency response and noise
  - SLiCAP small-signal models

MOS design



Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

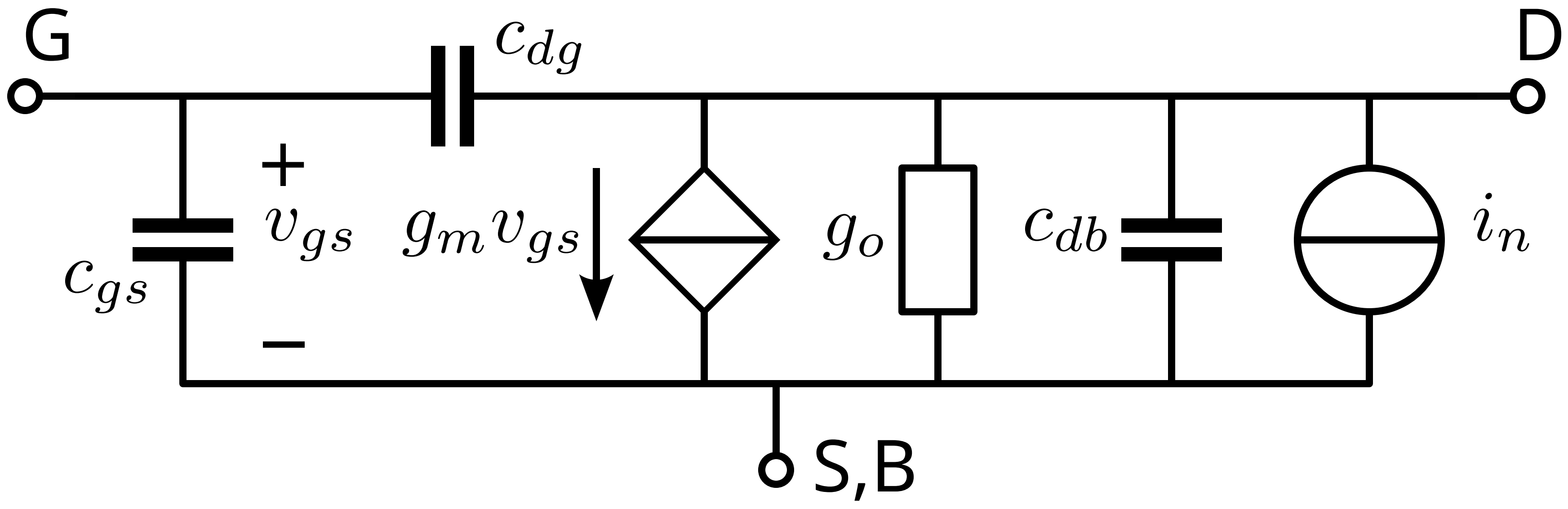
Channel width
Channel length
Number of sections
Drain current
Drain-source voltage

Methods

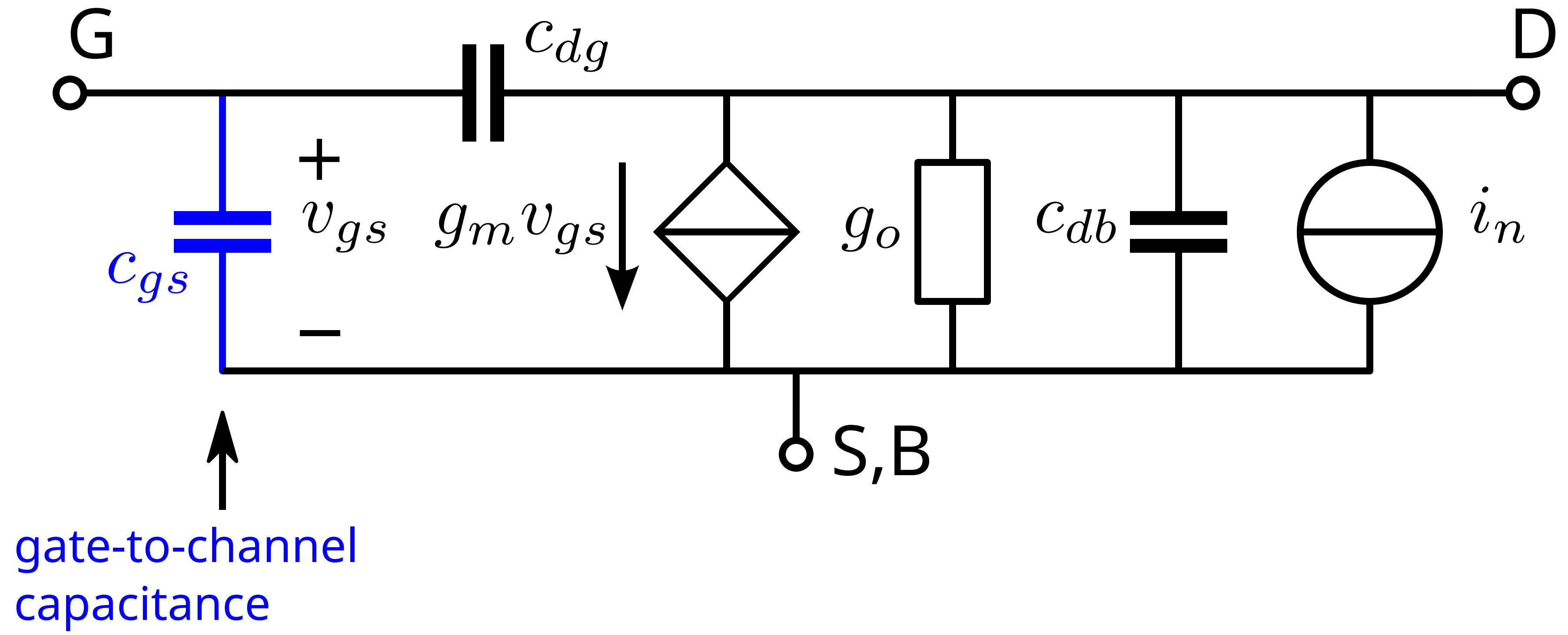
- Use a design manual with graphs and tables and scale devices
  - Useful, but generally not all situations will be covered
- Design a device and study its performance through simulation
  - Useful for finding DC operating conditions and small-signal model parameters
  - Jupyter notebook tool
- Use simplified design models
  - Useful for design of small signal behavior: bandwidth frequency response and noise
  - SLiCAP small-signal models

MOS small-signal model

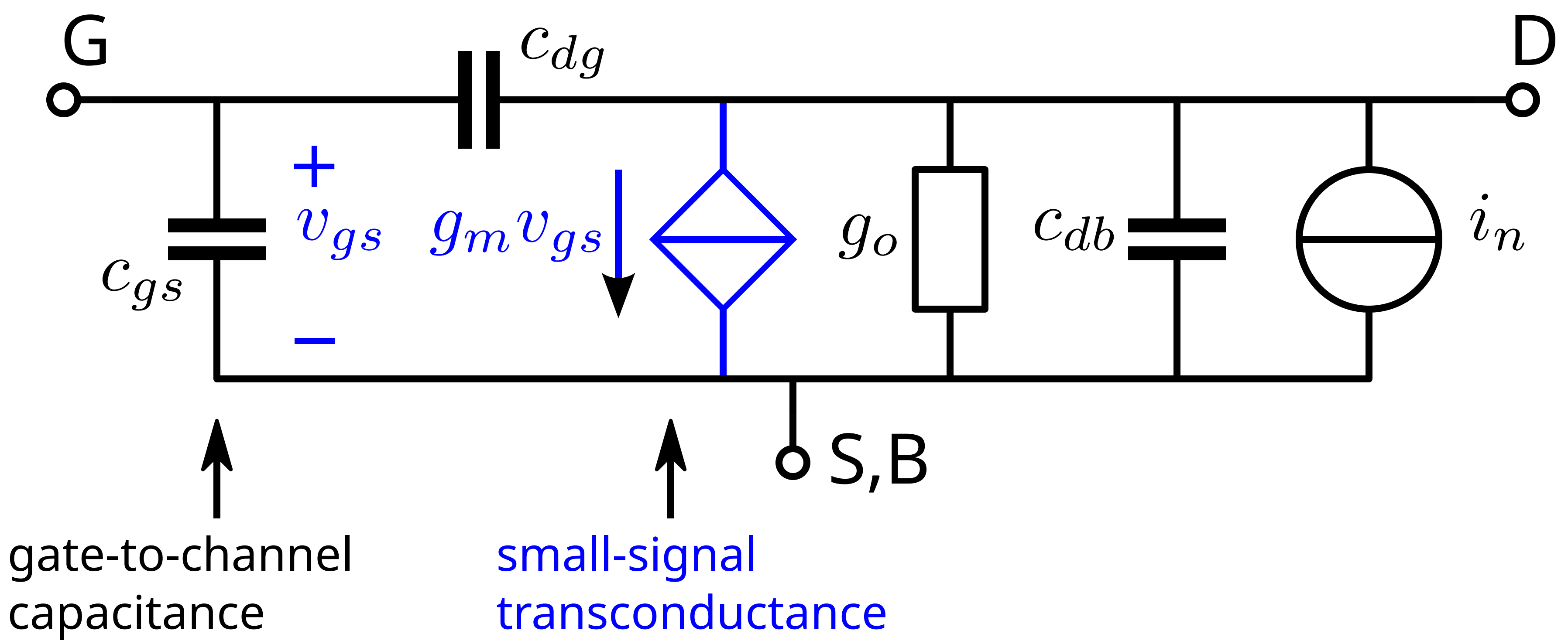
MOS small-signal model



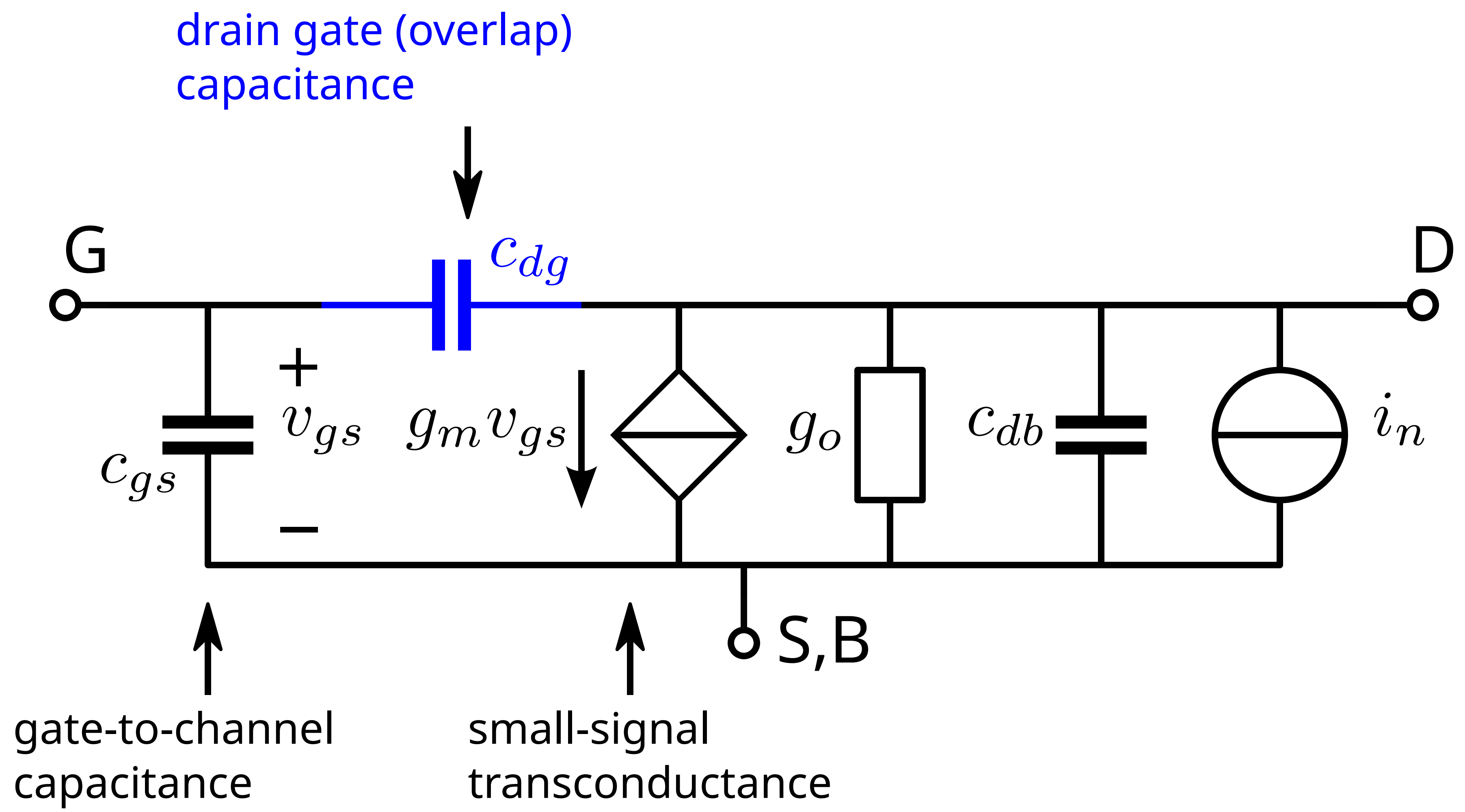
MOS small-signal model



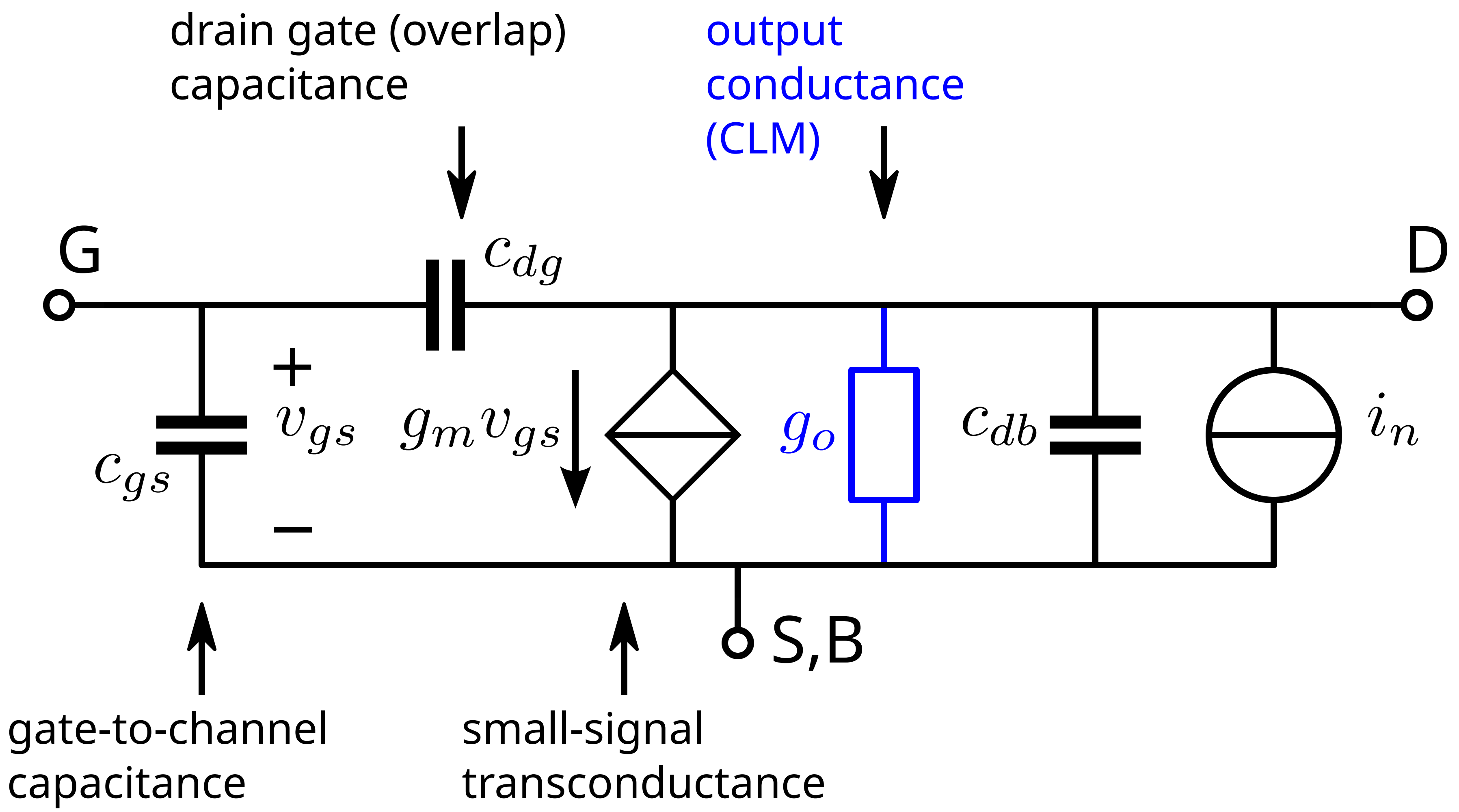
MOS small-signal model



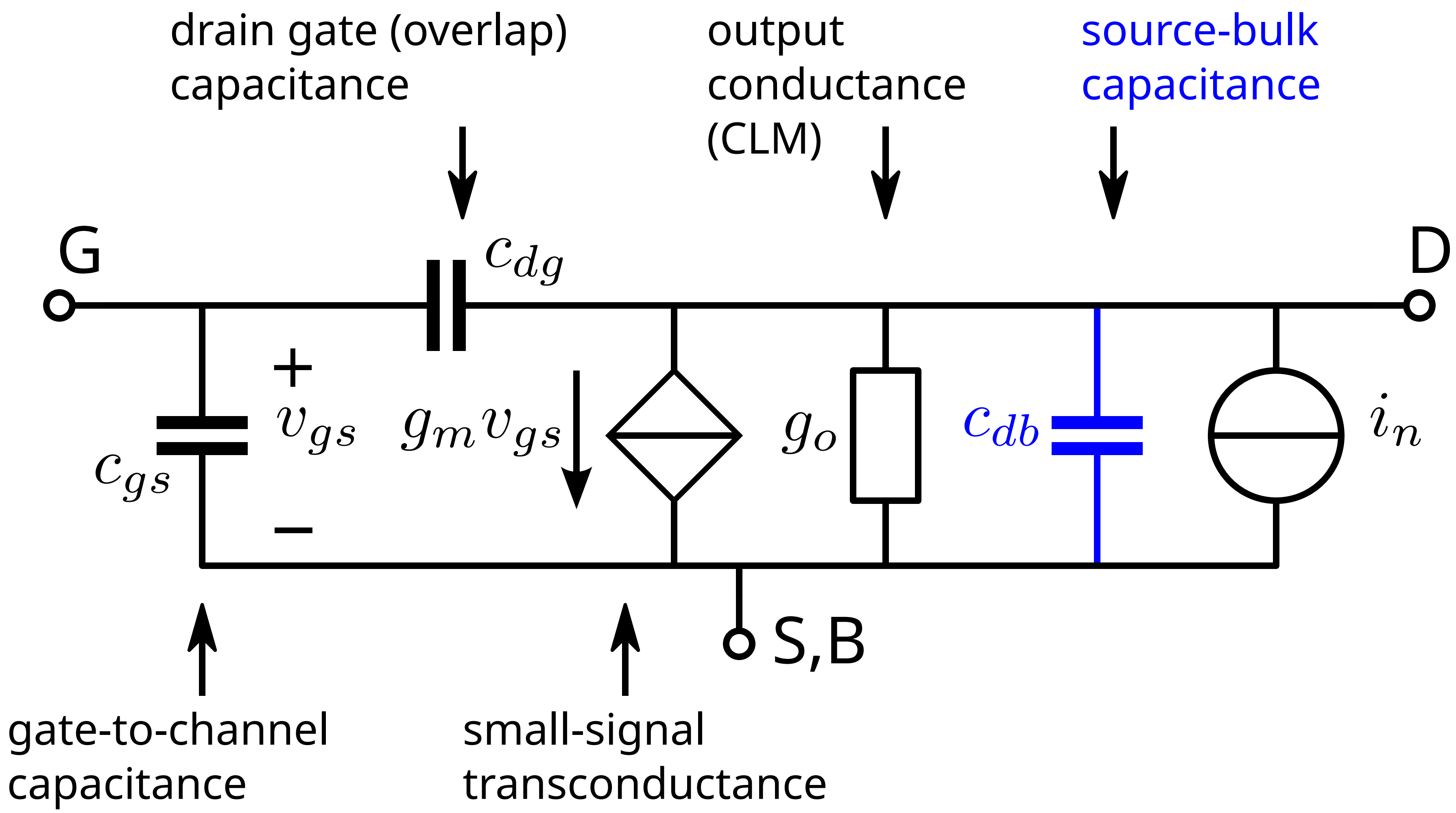
MOS small-signal model



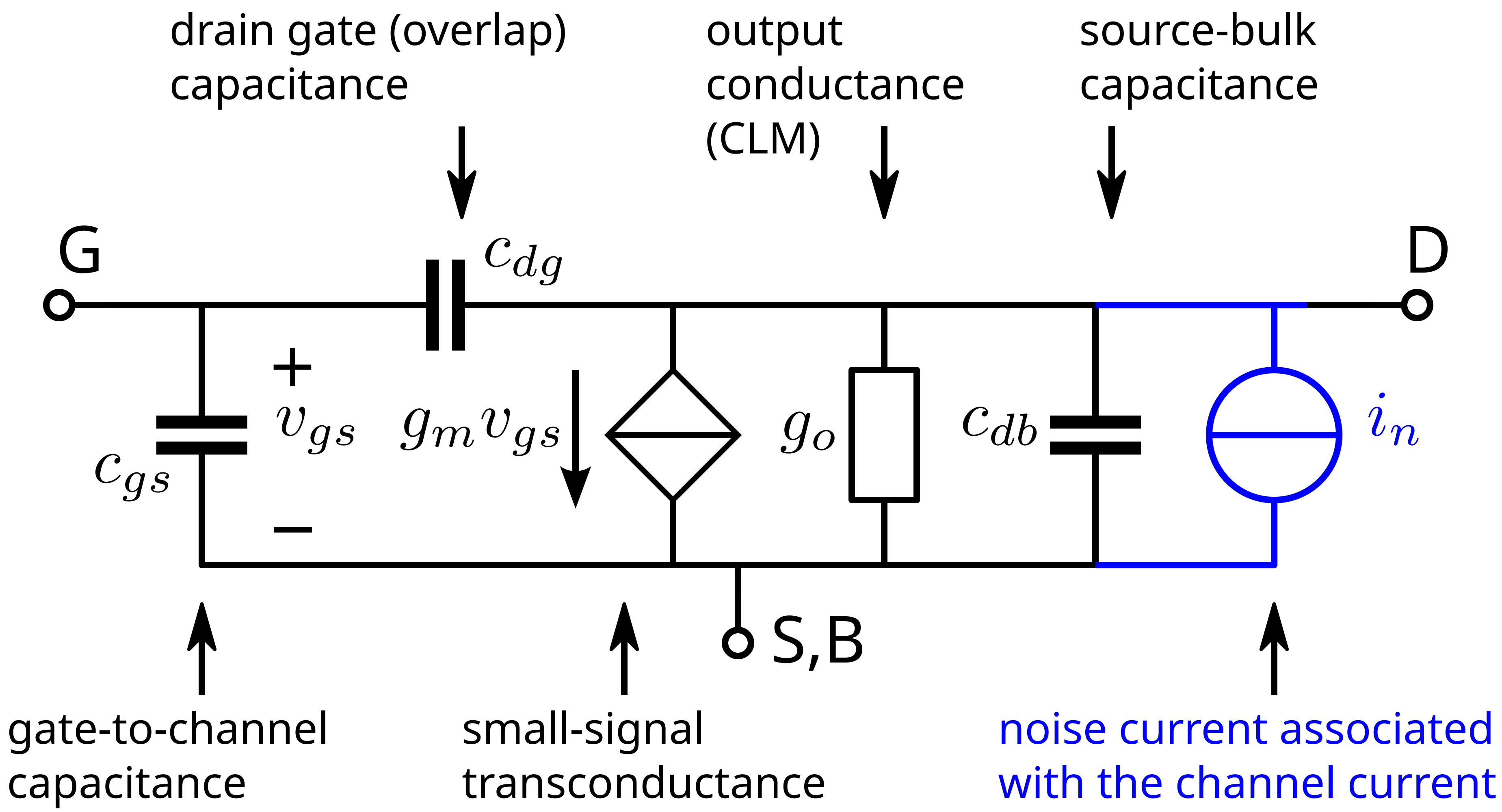
MOS small-signal model



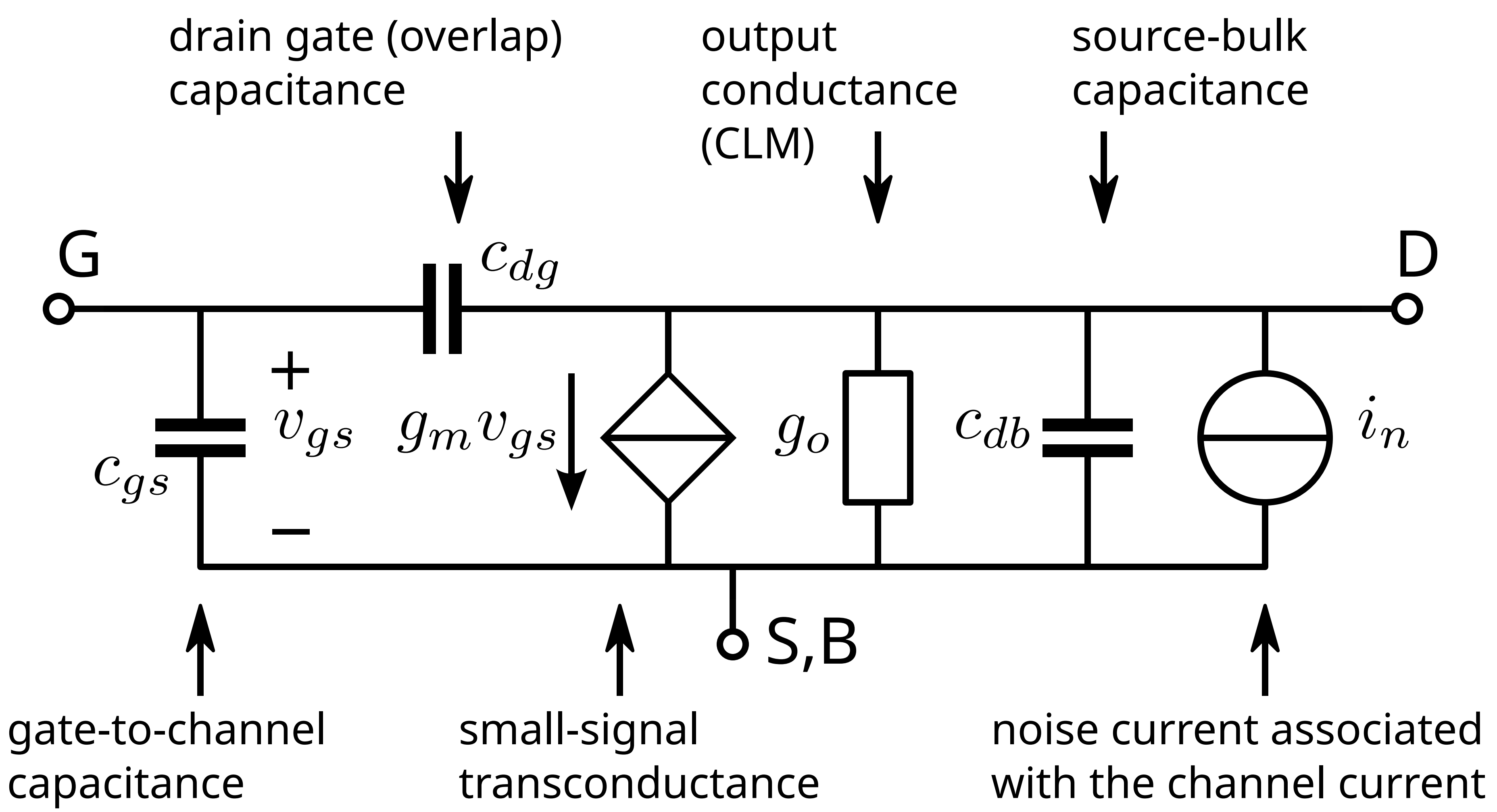
MOS small-signal model



MOS small-signal model

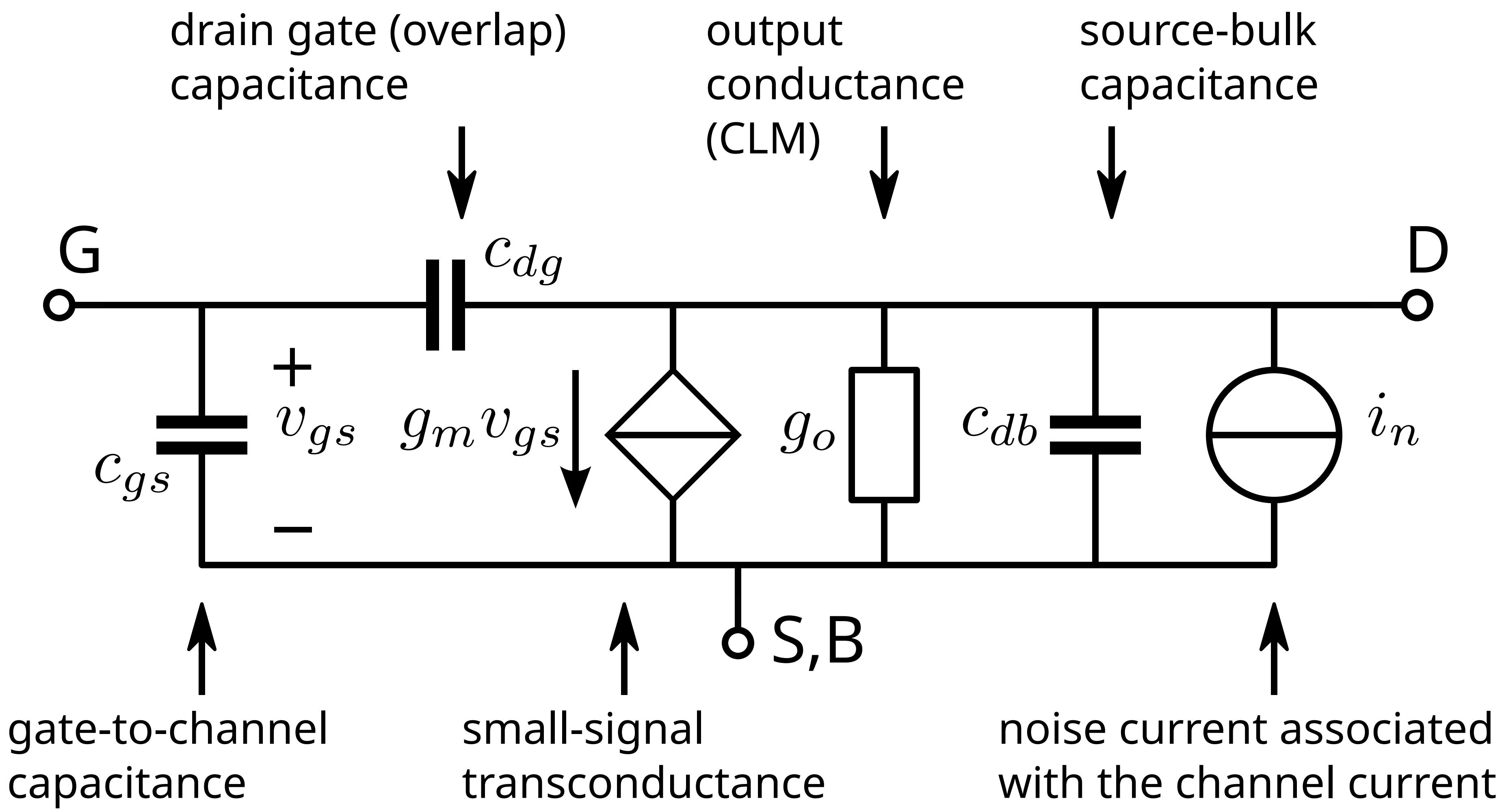


MOS small-signal model



How do these model parameters depend on the device geometry and the operating conditions?

MOS small-signal model



How do these model parameters depend on the device geometry and the operating conditions?

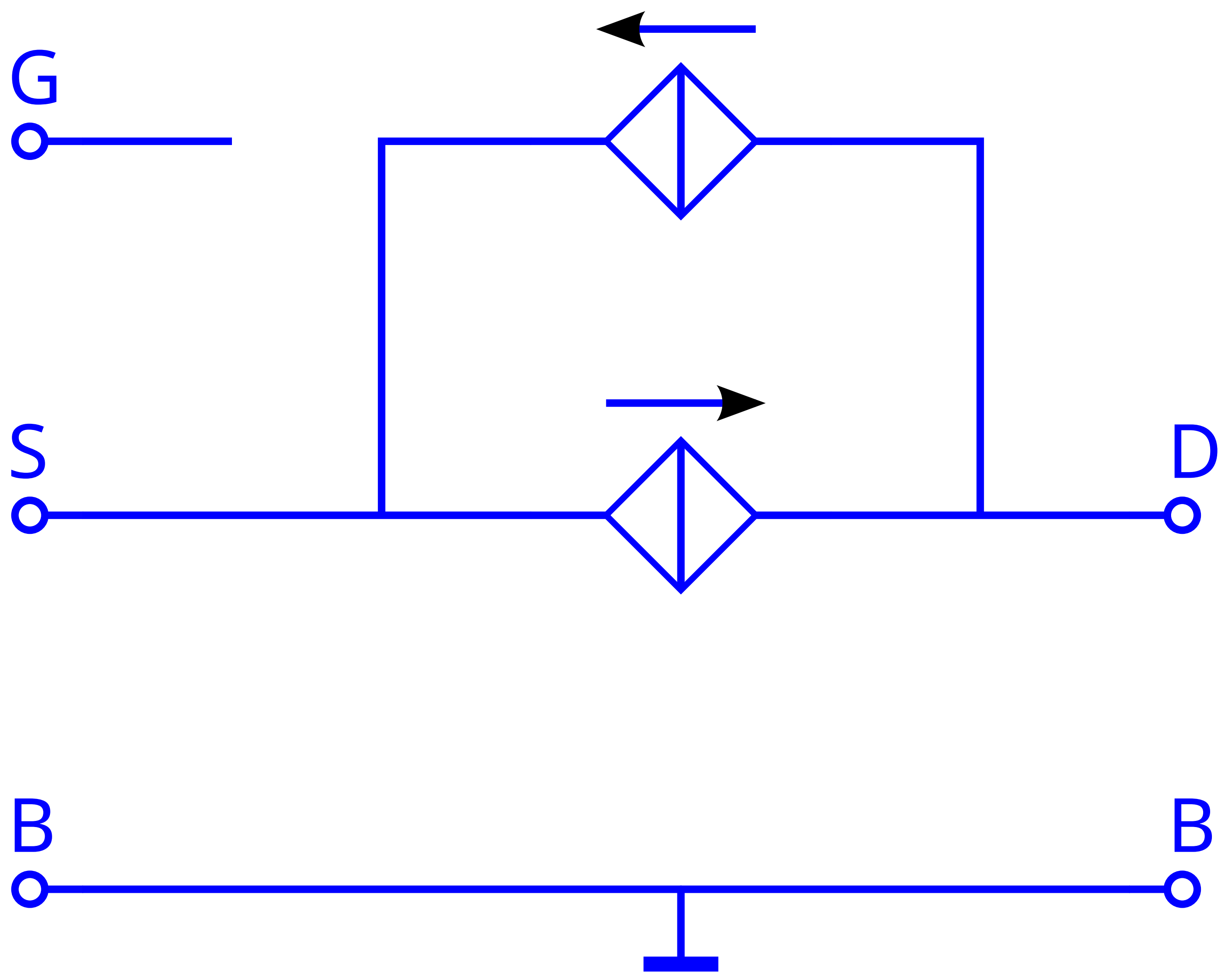
MOS EKV model

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz

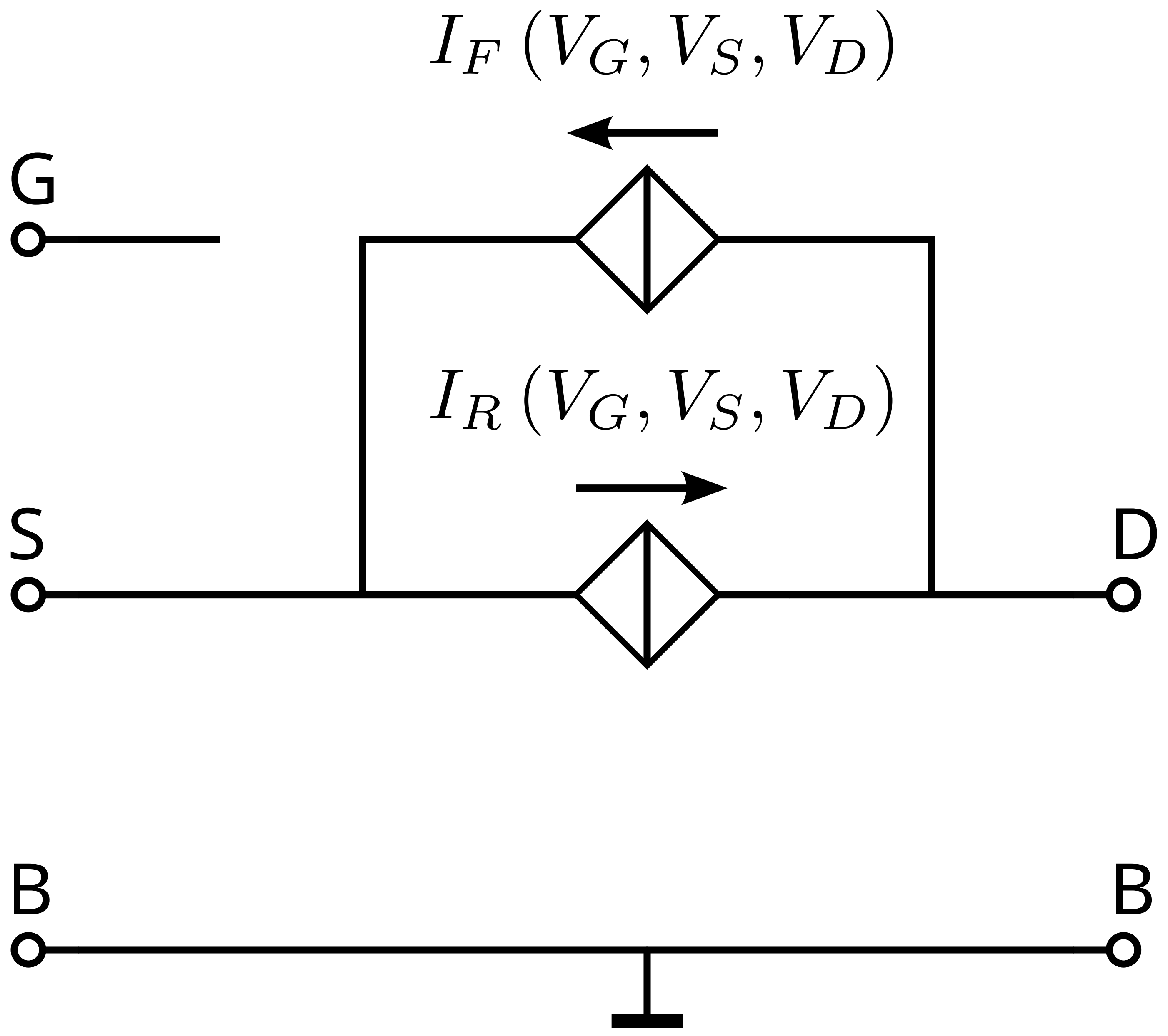
MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



MOS EKV model

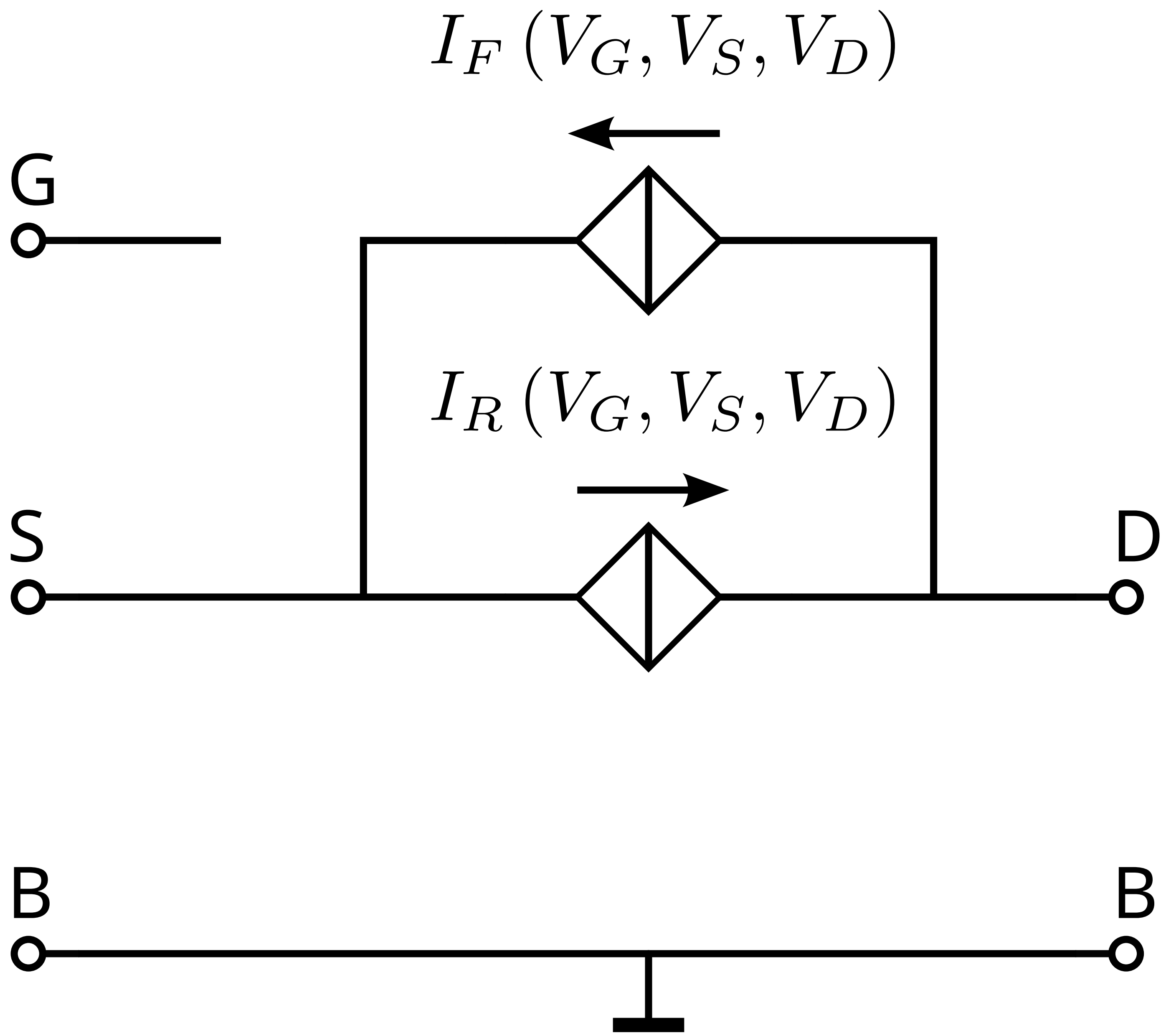
1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



Models all operating regions
from weak inversion to strong inversion

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz

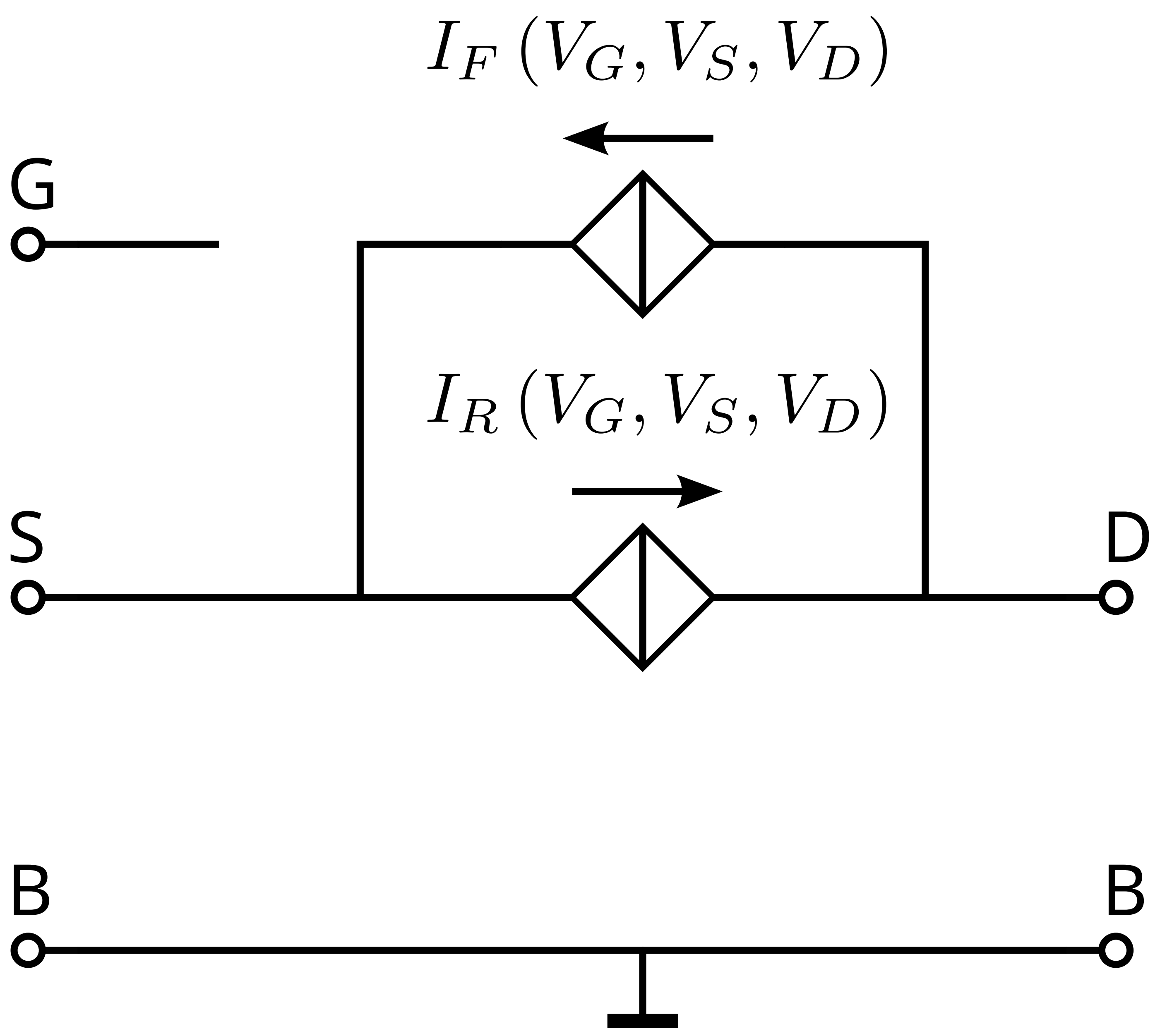


Models all operating regions
from weak inversion to strong inversion

Gate, source and drain voltages
with respect to the bulk

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



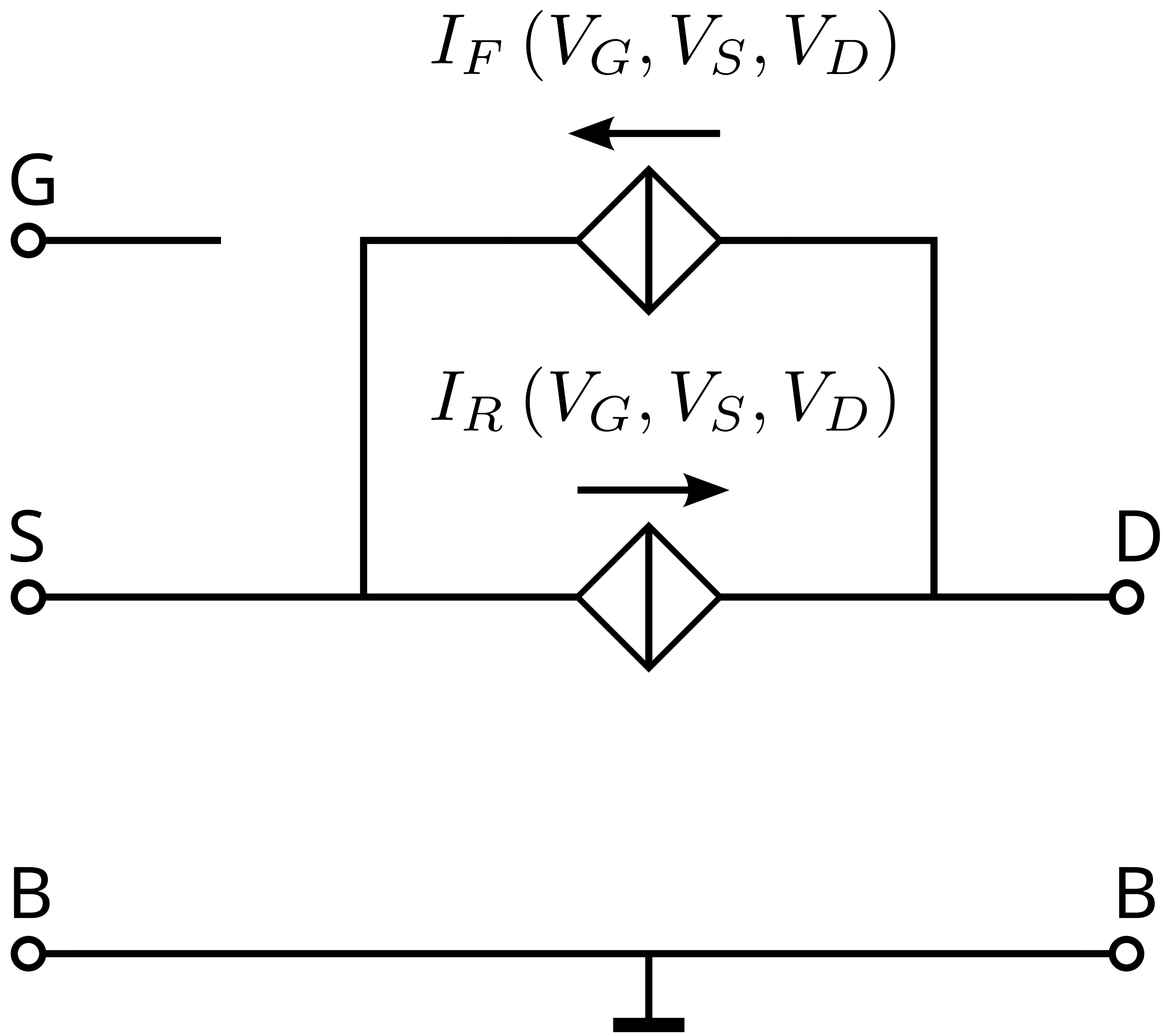
Models all operating regions
from weak inversion to strong inversion

Gate, source and drain voltages
with respect to the bulk

Symmetrical charge-controlled model

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



Models all operating regions
from weak inversion to strong inversion

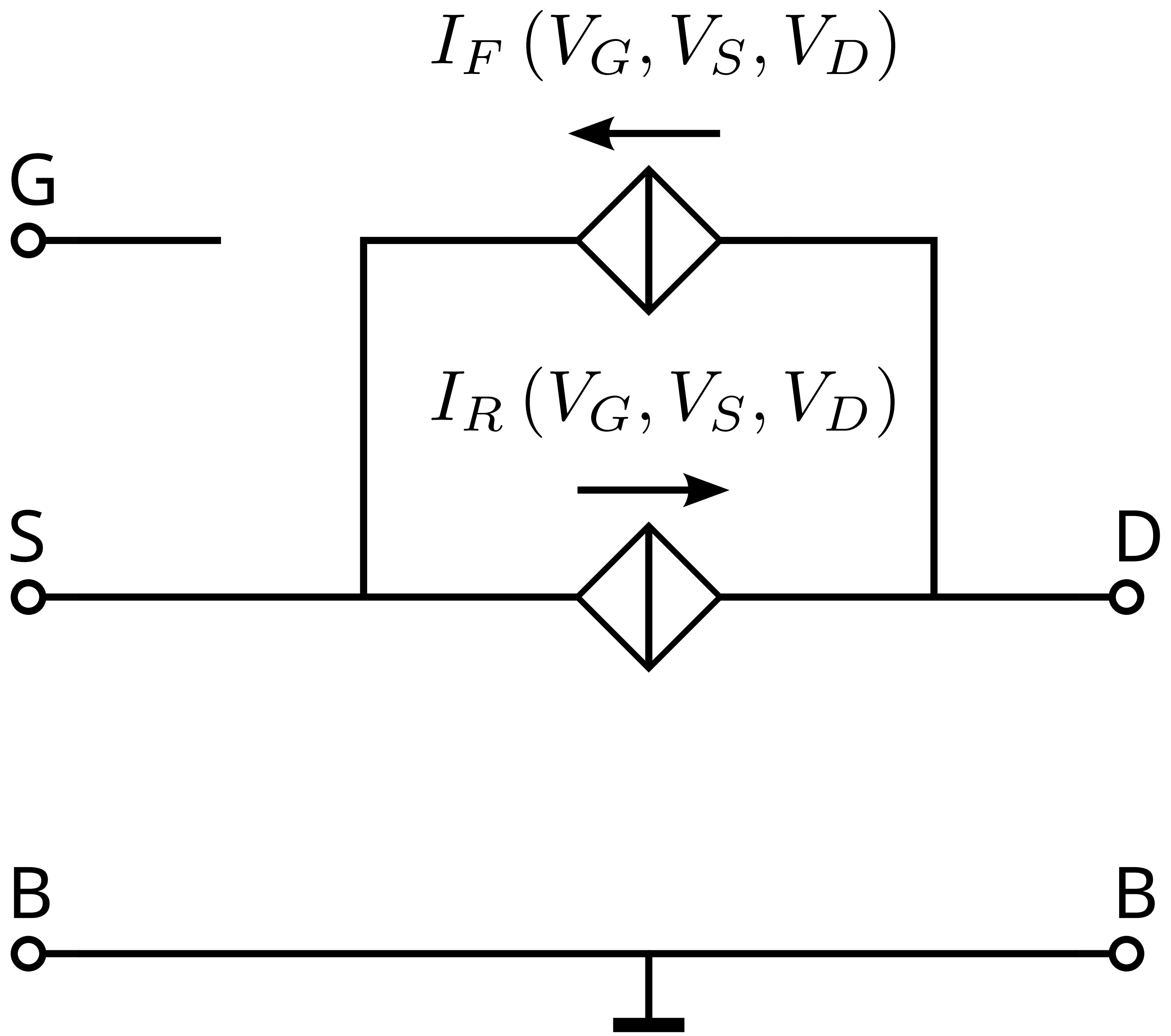
Gate, source and drain voltages
with respect to the bulk

Symmetrical charge-controlled model

Technology current: $I_0 \triangleq 2n\mu_0 C'_{OX} U_T^2 \;[\mathrm{A}]$

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



Models all operating regions
from weak inversion to strong inversion

Gate, source and drain voltages
with respect to the bulk

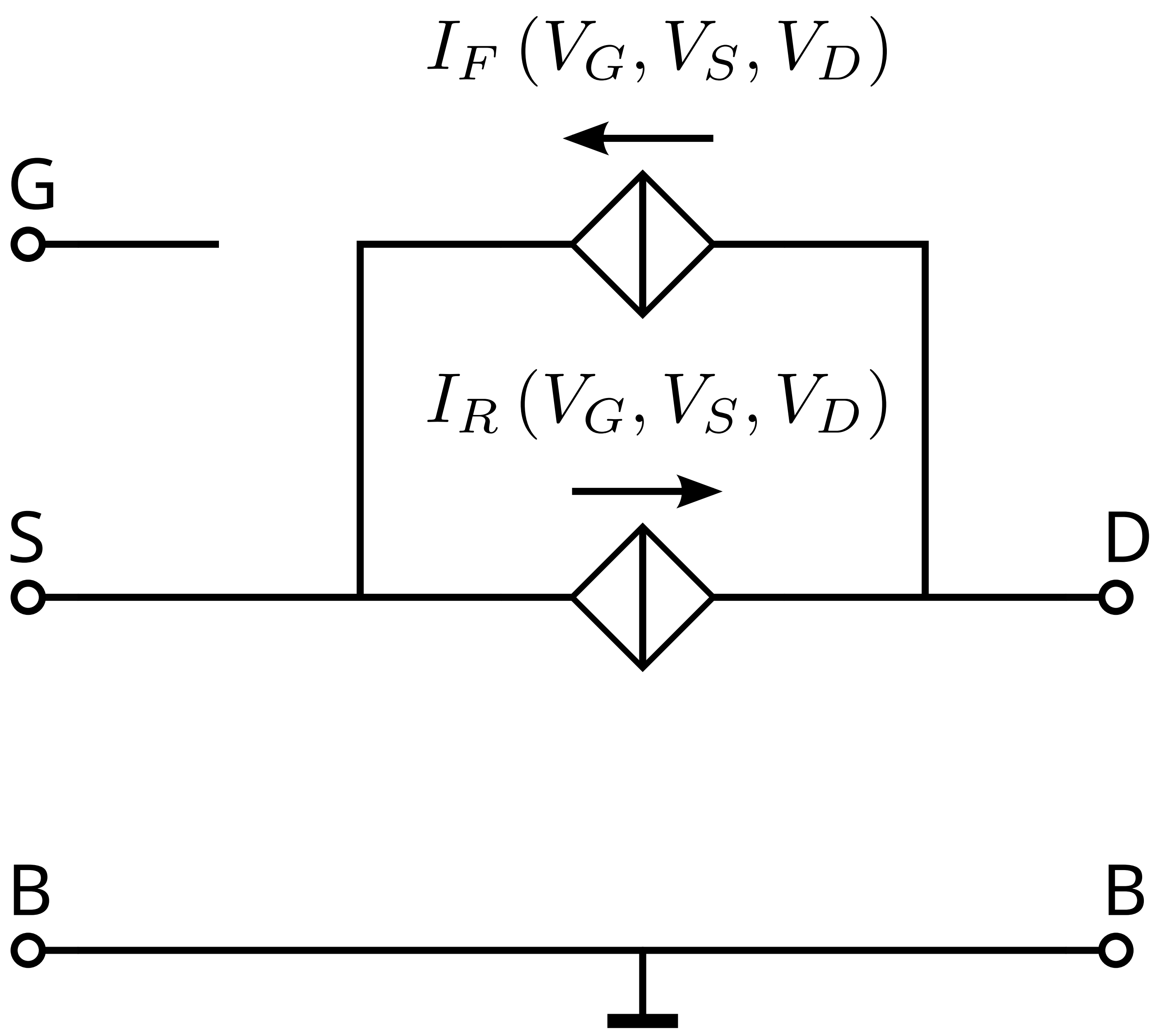
Symmetrical charge-controlled model

Technology current: $I_0 \triangleq 2n\mu_0 C'_{OX} U_T^2$ [A]

$C'_{OX} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}}$ [Fm^{-2}]

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



Models all operating regions
from weak inversion to strong inversion

Gate, source and drain voltages
with respect to the bulk

Symmetrical charge-controlled model

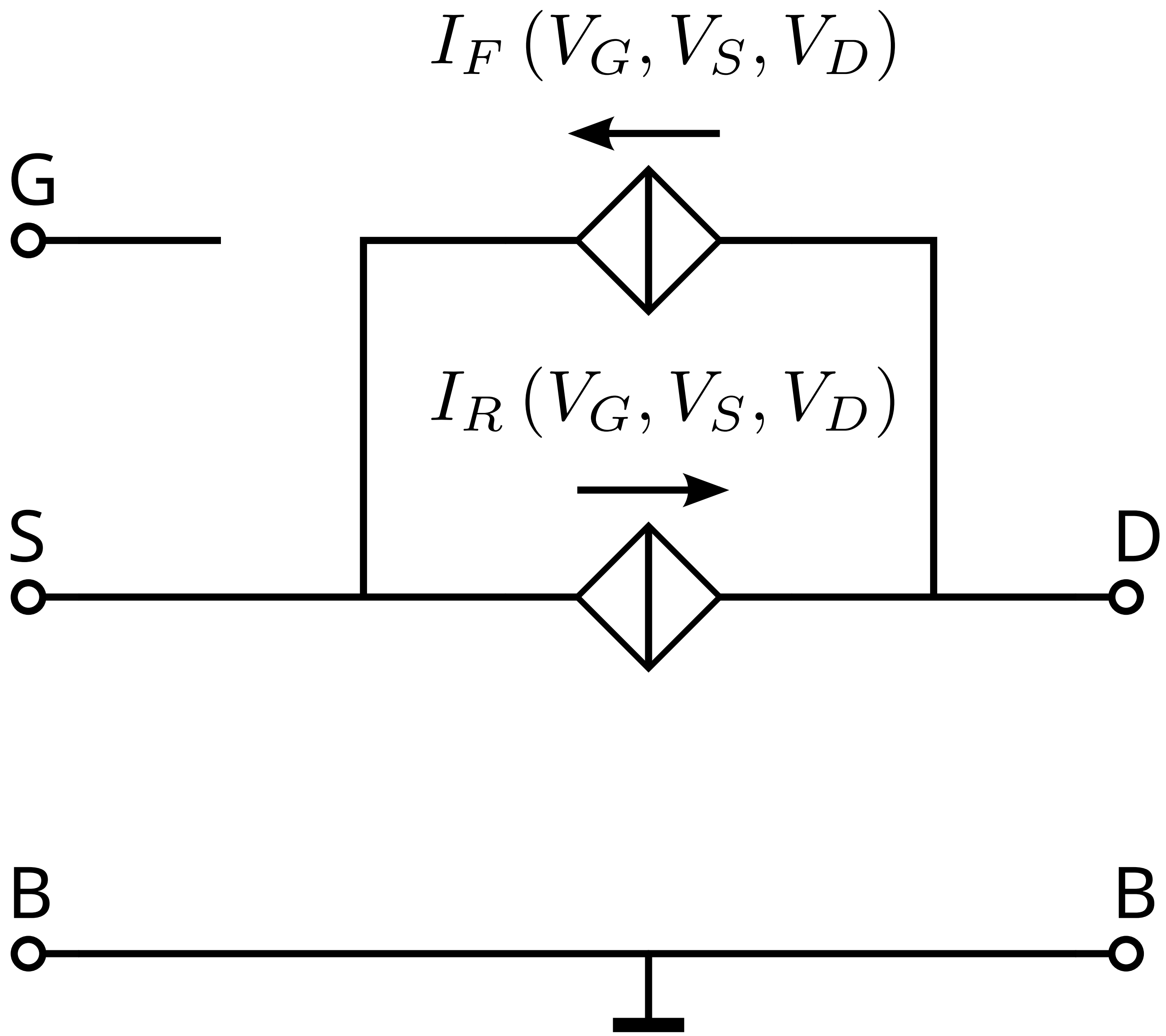
Technology current: $I_0 \triangleq 2n\mu_0 C'_{OX} U_T^2\ [\mathrm{A}]$

$$C'_{OX} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}}\ [\mathrm{Fm}^{-2}]$$

$$U_T = \frac{kT}{q}\ [\mathrm{V}]$$

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



Models all operating regions
from weak inversion to strong inversion

Gate, source and drain voltages
with respect to the bulk

Symmetrical charge-controlled model

Technology current: $I_0 \triangleq 2n\mu_0 C'_{OX} U_T^2 \text{ [A]}$

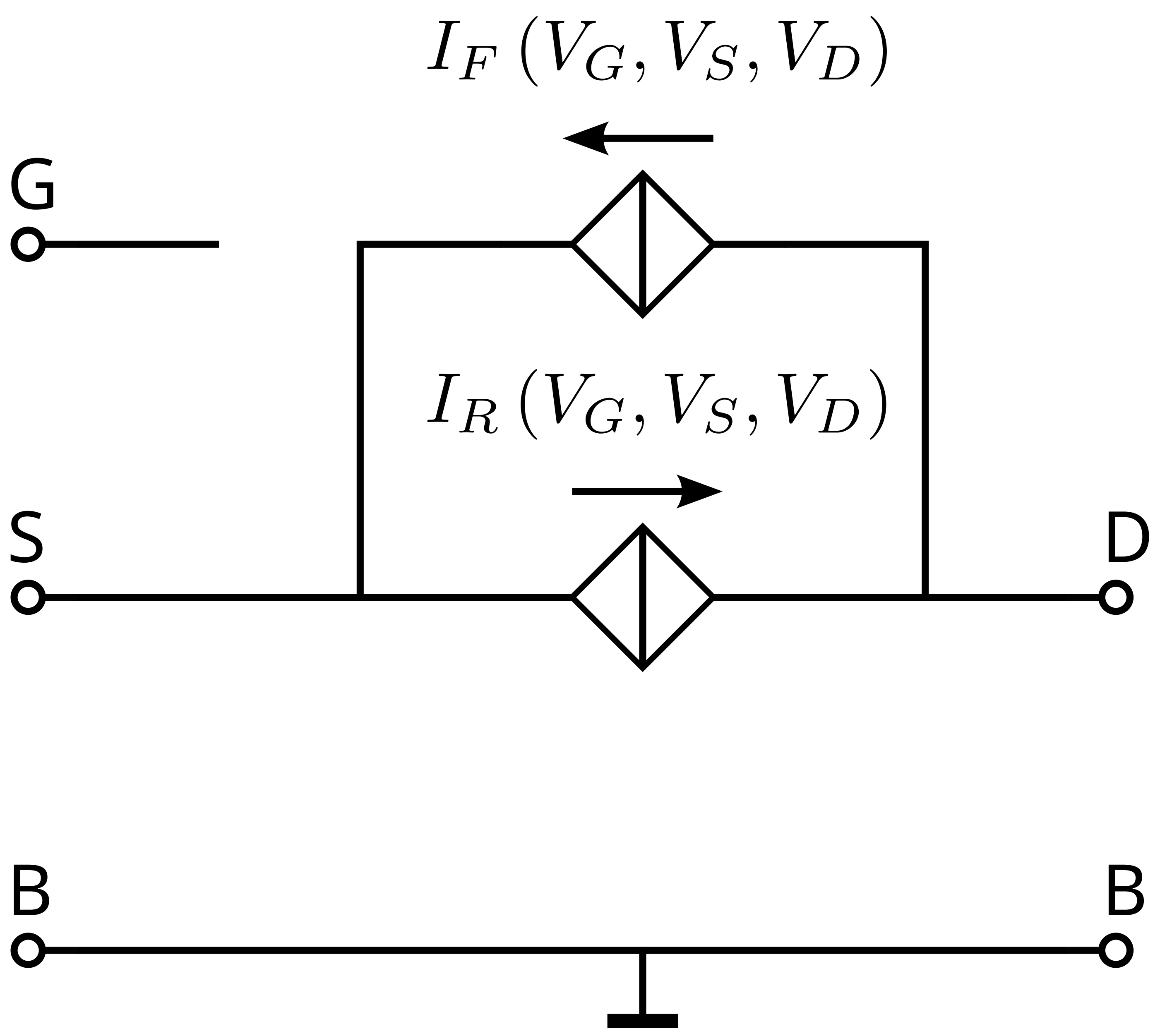
$$C'_{OX} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}} \text{ [Fm}^{-2}\text{]}$$

$$U_T = \frac{kT}{q} \text{ [V]}$$

Ratio of
surface potential
and gate voltage $\longrightarrow$ $n = 1 + \frac{C'_{DEP}}{C'_{OX}}$ [-]

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



Models all operating regions
from weak inversion to strong inversion

Gate, source and drain voltages
with respect to the bulk

Symmetrical charge-controlled model

Technology current: $I_0 \triangleq 2n\mu_0 C'_{OX} U_T^2 \ [\mathrm{A}]$

$$C'_{OX} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}} \ [\mathrm{Fm}^{-2}]$$

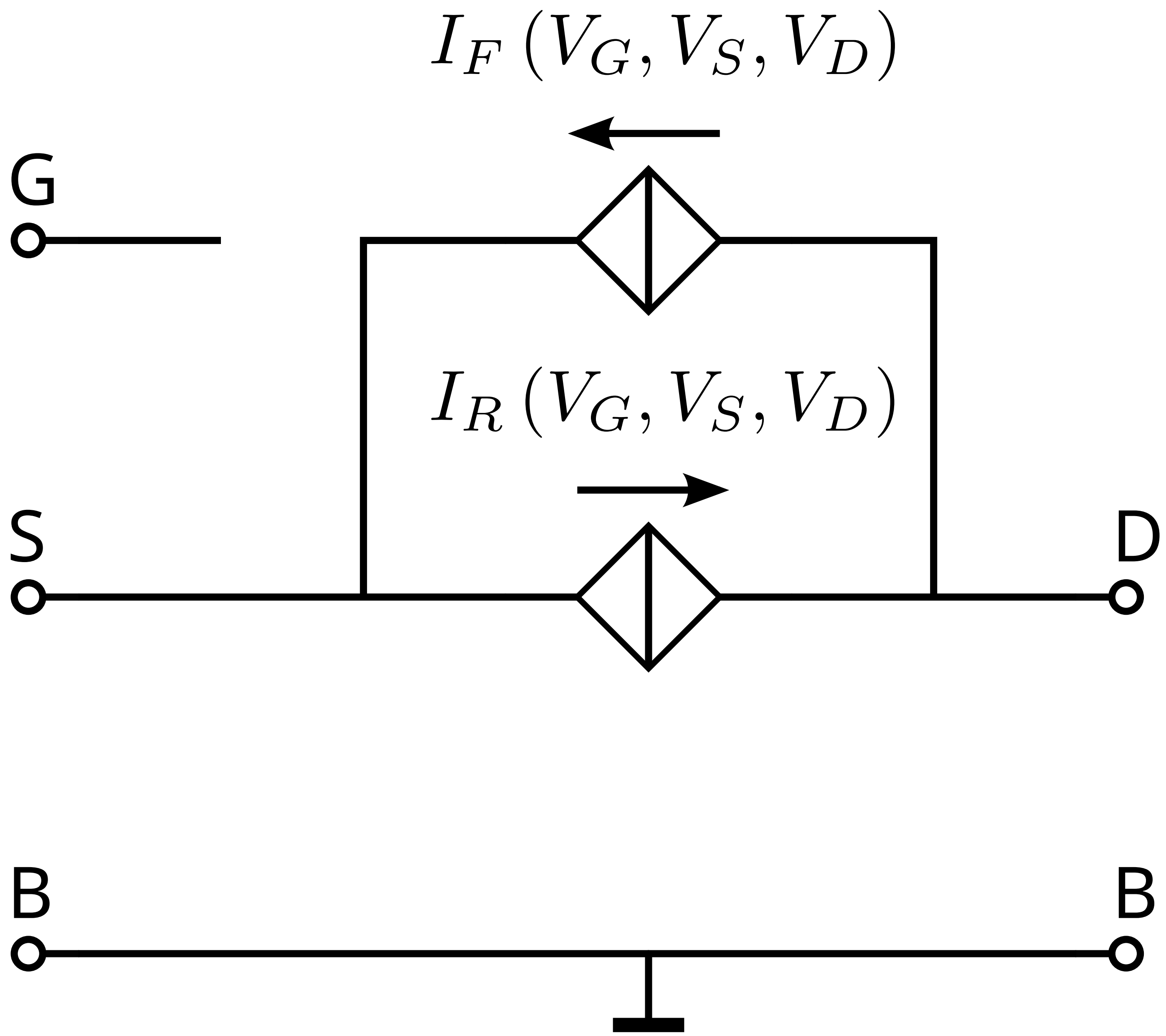
$$U_T = \frac{kT}{q} \ [\mathrm{V}]$$

Ratio of surface potential and gate voltage → $n = 1 + \frac{C'_{DEP}}{C'_{OX}}$ [-]

zero-field carrier mobility → $\mu_0 \ [\mathrm{m}^2\mathrm{V}^{-1}\mathrm{s}^{-1}]$

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



Models all operating regions
from weak inversion to strong inversion

Gate, source and drain voltages
with respect to the bulk

Symmetrical charge-controlled model

Technology current: $I_0 \triangleq 2n\mu_0 C'_{OX} U_T^2\ [\mathrm{A}]$

$$C'_{OX} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}}\ [\mathrm{Fm}^{-2}]$$

$$U_T = \frac{kT}{q}\ [\mathrm{V}]$$

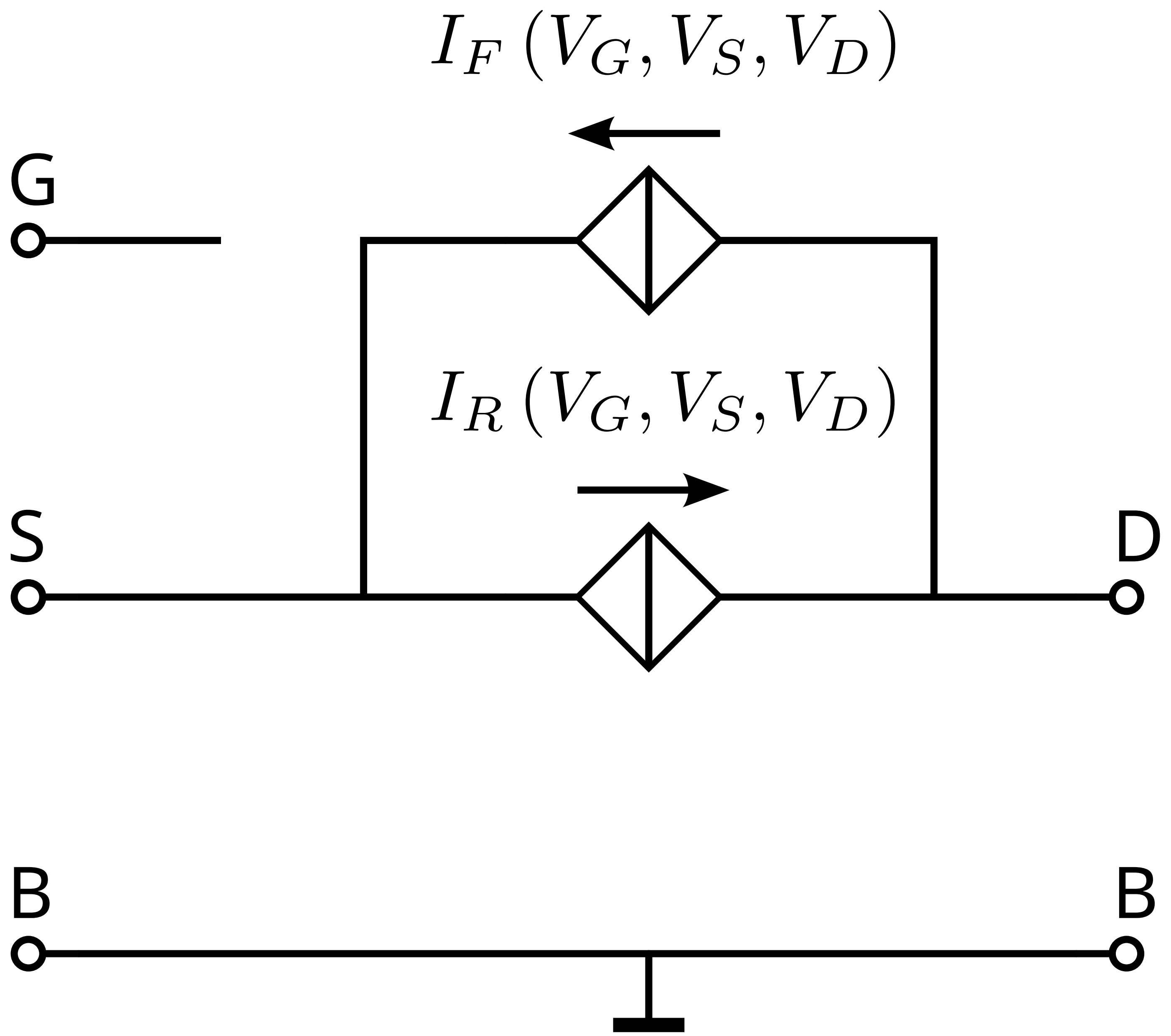
Ratio of surface potential and gate voltage → $n = 1 + \frac{C'_{DEP}}{C'_{OX}}$ [-]

zero-field carrier mobility → $\mu_0\ [\mathrm{m}^2\mathrm{V}^{-1}\mathrm{s}^{-1}]$

oxide thickness → $t_{ox}\ [\mathrm{m}]$

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



Models all operating regions
from weak inversion to strong inversion

Gate, source and drain voltages
with respect to the bulk

Symmetrical charge-controlled model

Technology current: $I_0 \triangleq 2n\mu_0 C'_{OX} U_T^2 \ [\mathrm{A}]$

$$C'_{OX} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}} \ [\mathrm{Fm^{-2}}]$$

$$U_T = \frac{kT}{q} \ [\mathrm{V}]$$

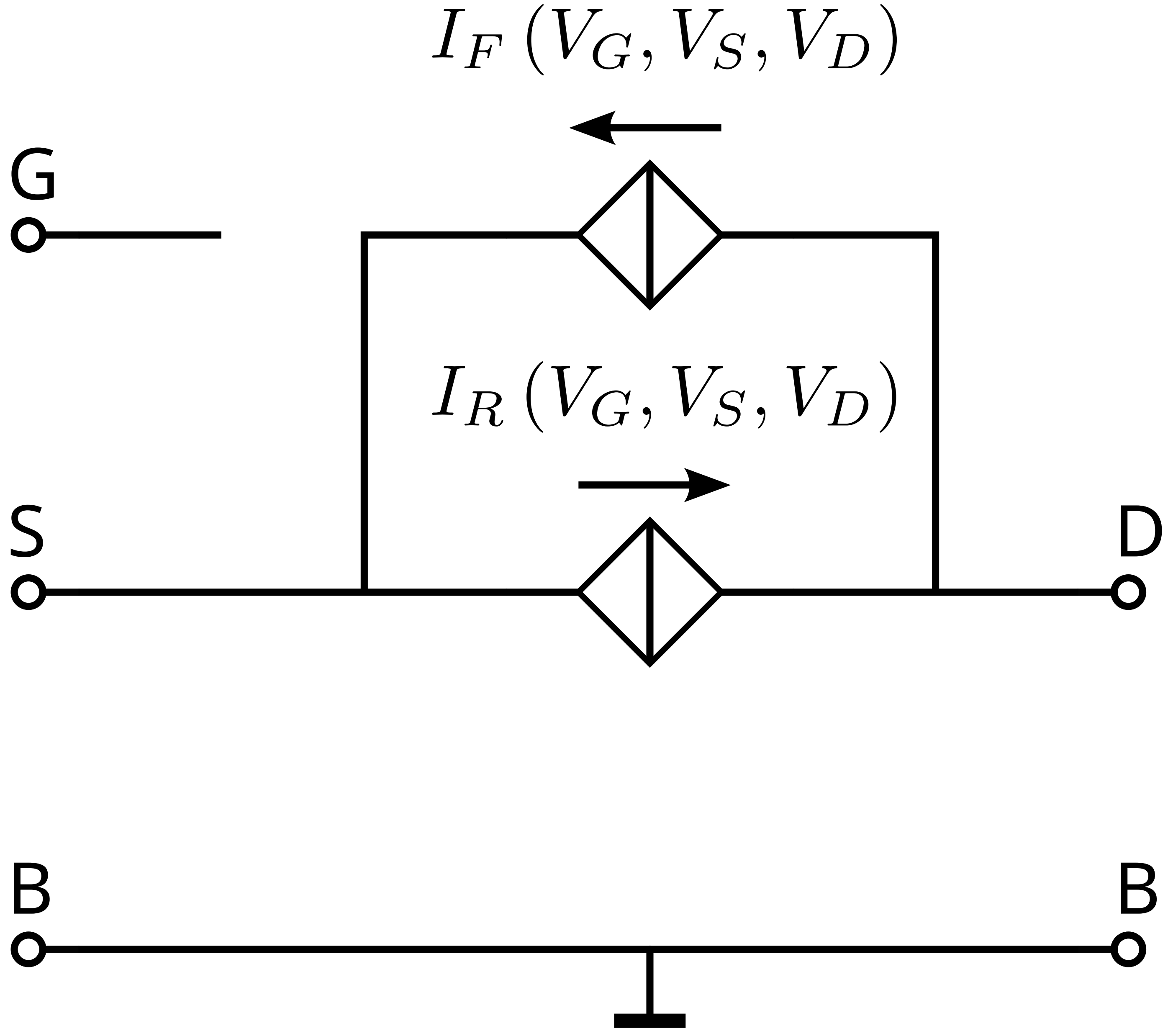
Ratio of surface potential and gate voltage $\longrightarrow$ $n = 1 + \frac{C'_{DEP}}{C'_{OX}} \ [\text{-}]$

zero-field carrier mobility $\longrightarrow$ $\mu_0 \left[\mathrm{m^2 V^{-1} s^{-1}}\right]$

oxide thickness $\longrightarrow$ $t_{ox} \, [\mathrm{m}]$

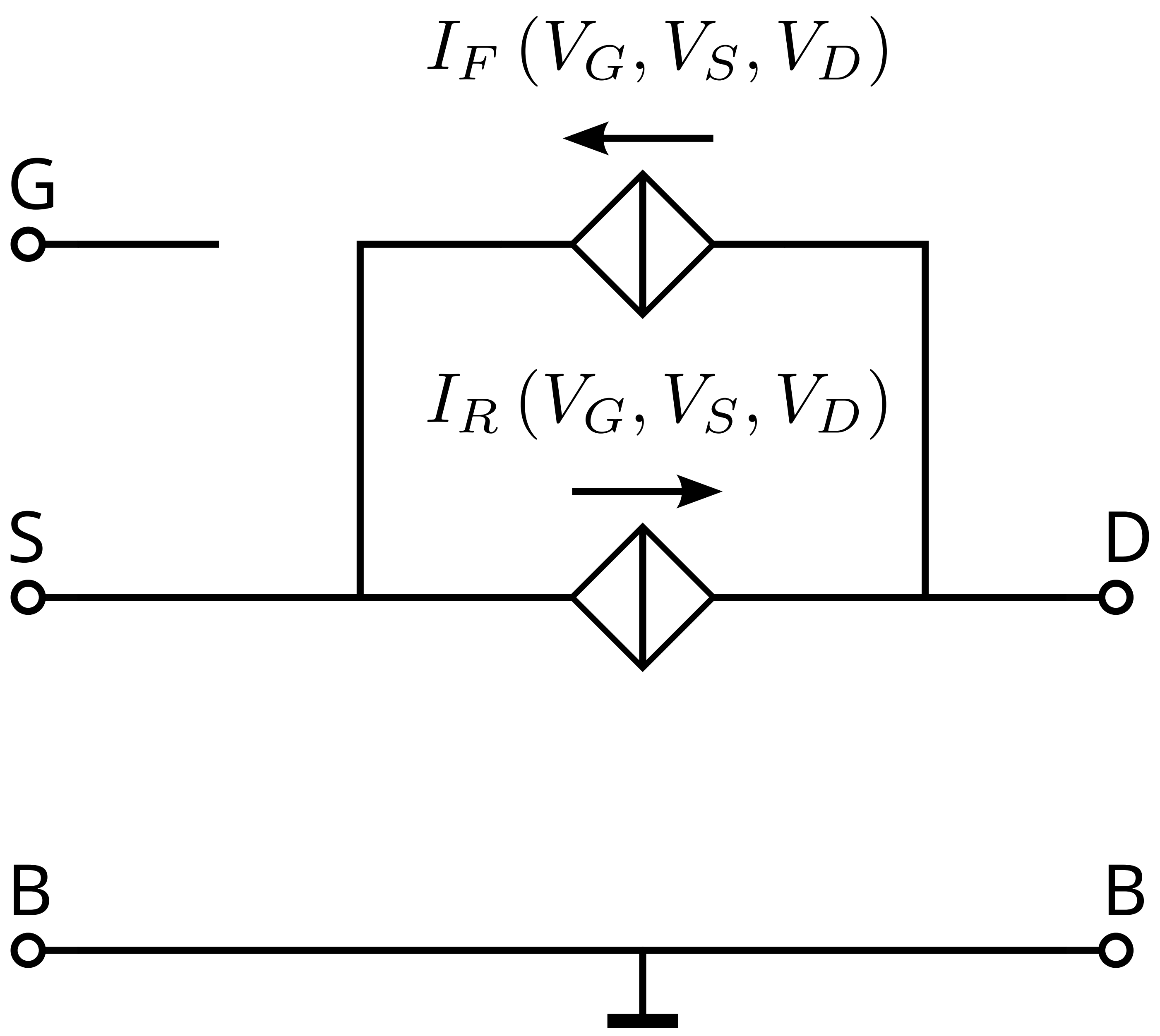
MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



MOS EKV model

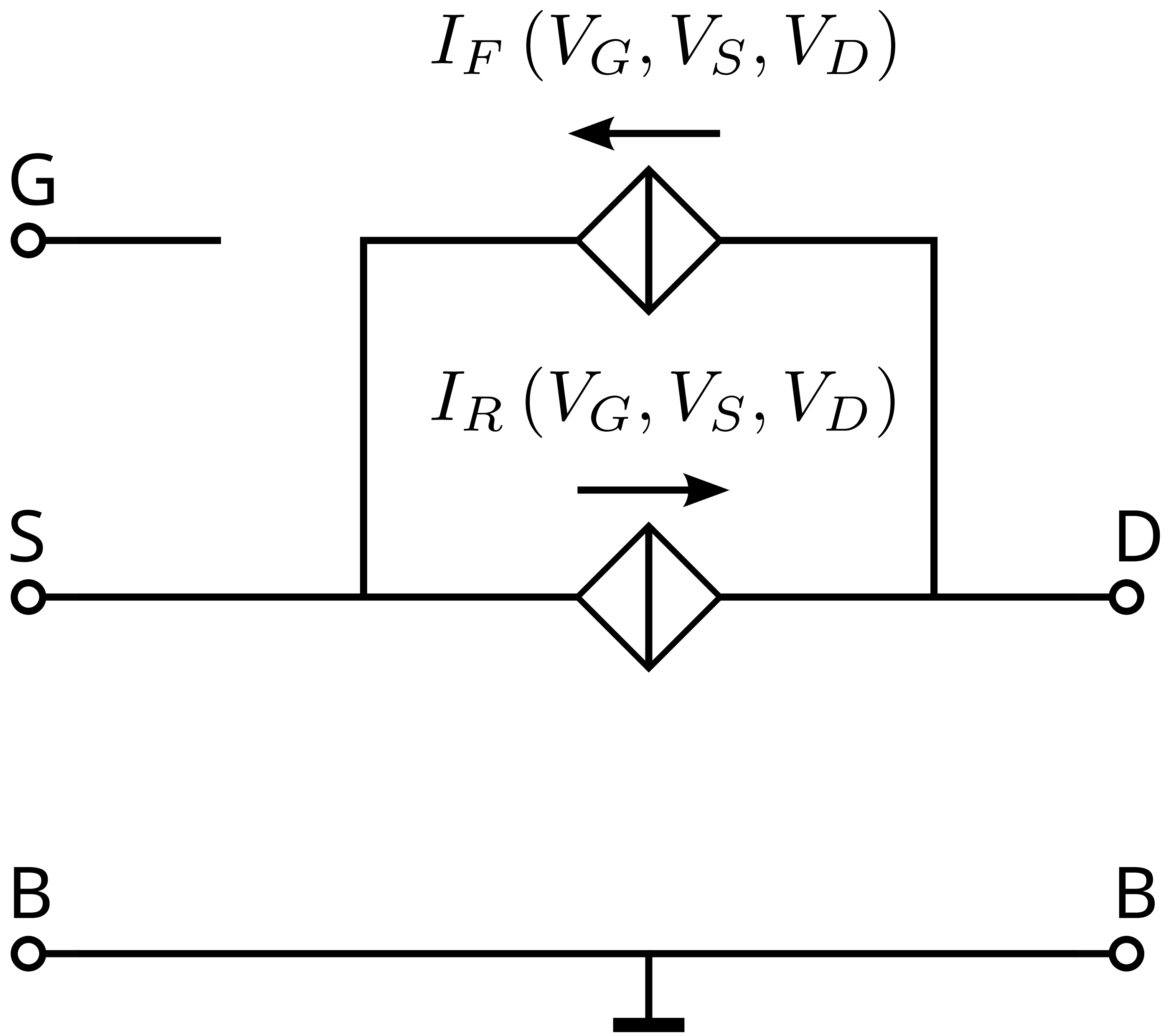
1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



$$F\left(x\right) = \left(\ln\left(1 + \exp\left(\frac{x}{2}\right)\right)\right)^2 \text{ [-]}$$

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz

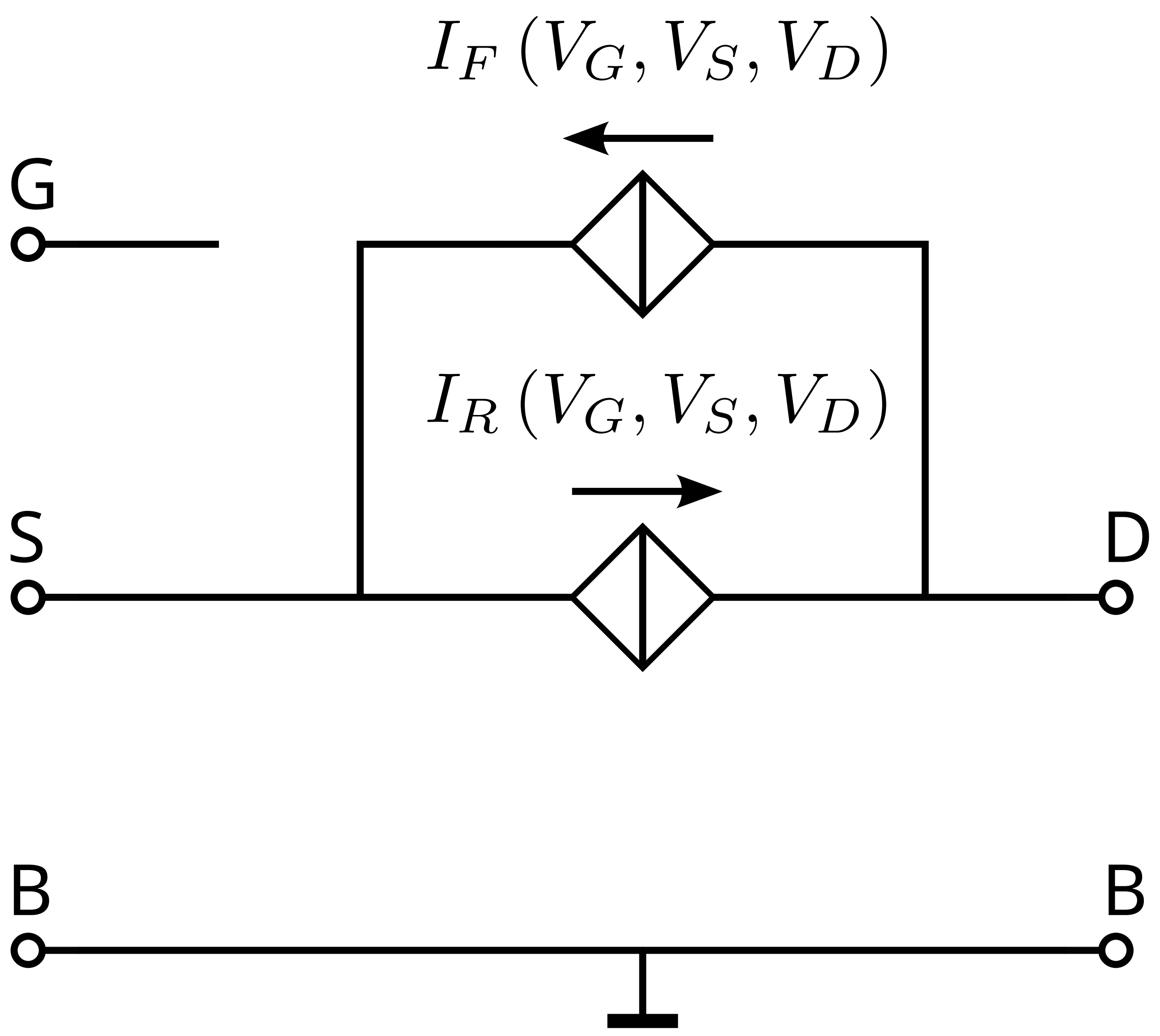


$$F\left(x\right) = \left(\ln\left(1 + \exp\left(\tfrac{x}{2}\right)\right)\right)^2 \quad [-]$$

this yields: $\begin{cases} \exp(x) & \text{if } x \ll 0, \\ \left(\frac{x}{2}\right)^2 & \text{if } x \gg 0. \end{cases}$

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



$$F\left(x\right) = \left(\ln\left(1+\exp\left(\frac{x}{2}\right)\right)\right)^2 \quad \text{[-]}$$

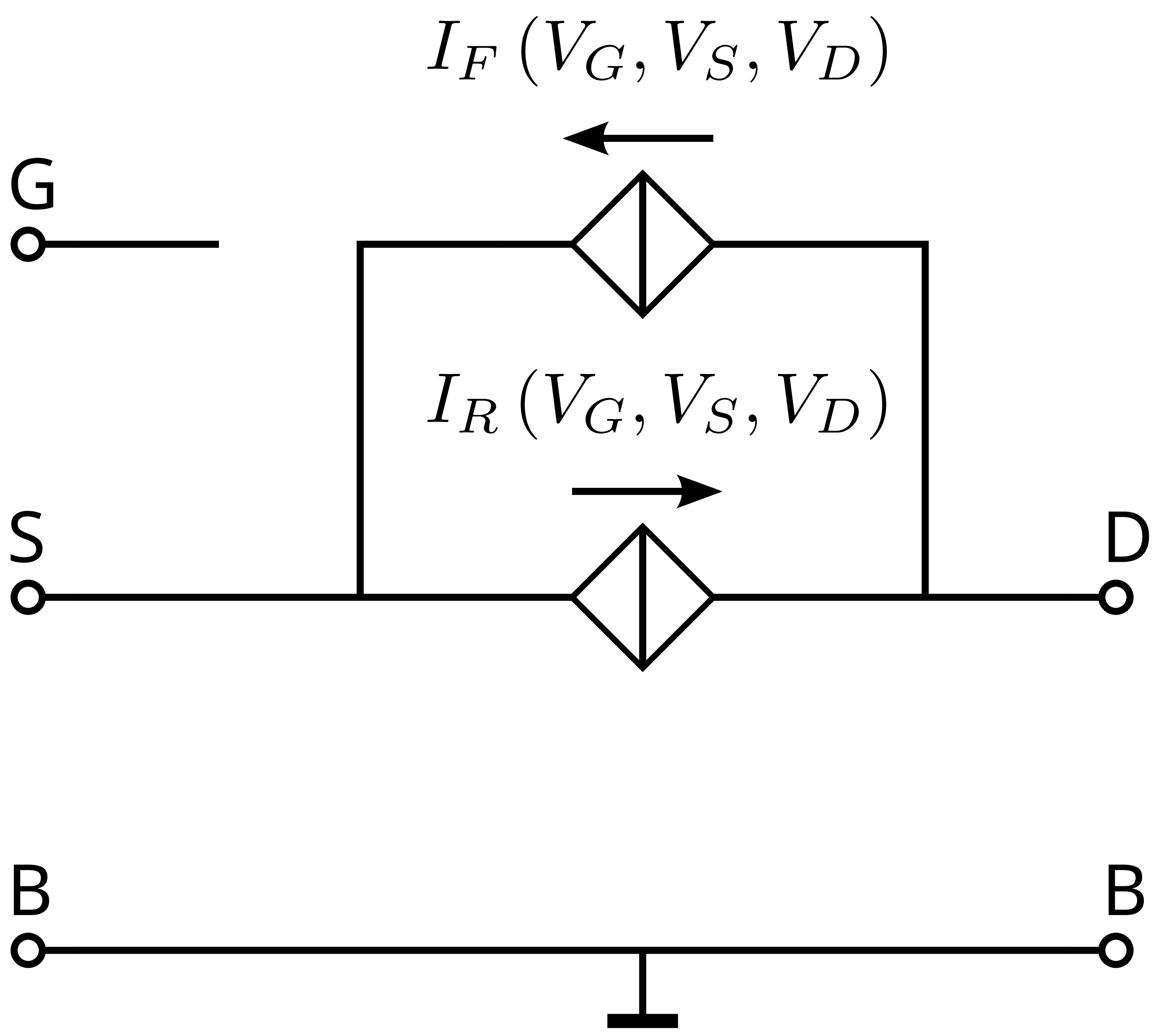
this yields: $\begin{cases} \exp(x) & \text{if } x \ll 0, \\ \left(\frac{x}{2}\right)^2 & \text{if } x \gg 0. \end{cases}$

Forward and reverse inversion coefficient:

$$IC_{F,R} = F\left(\frac{V_G - V_{T0} - nV_{S,D}}{nU_T}\right) \quad \text{[-]}$$

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



$$F(x) = \left(\ln\left(1+\exp\left(\tfrac{x}{2}\right)\right)\right)^2 \ \text{[-]}$$

this yields: $\begin{cases} \exp(x) & \text{if } x \ll 0, \\ \left(\frac{x}{2}\right)^2 & \text{if } x \gg 0. \end{cases}$

Forward and reverse inversion coefficient:

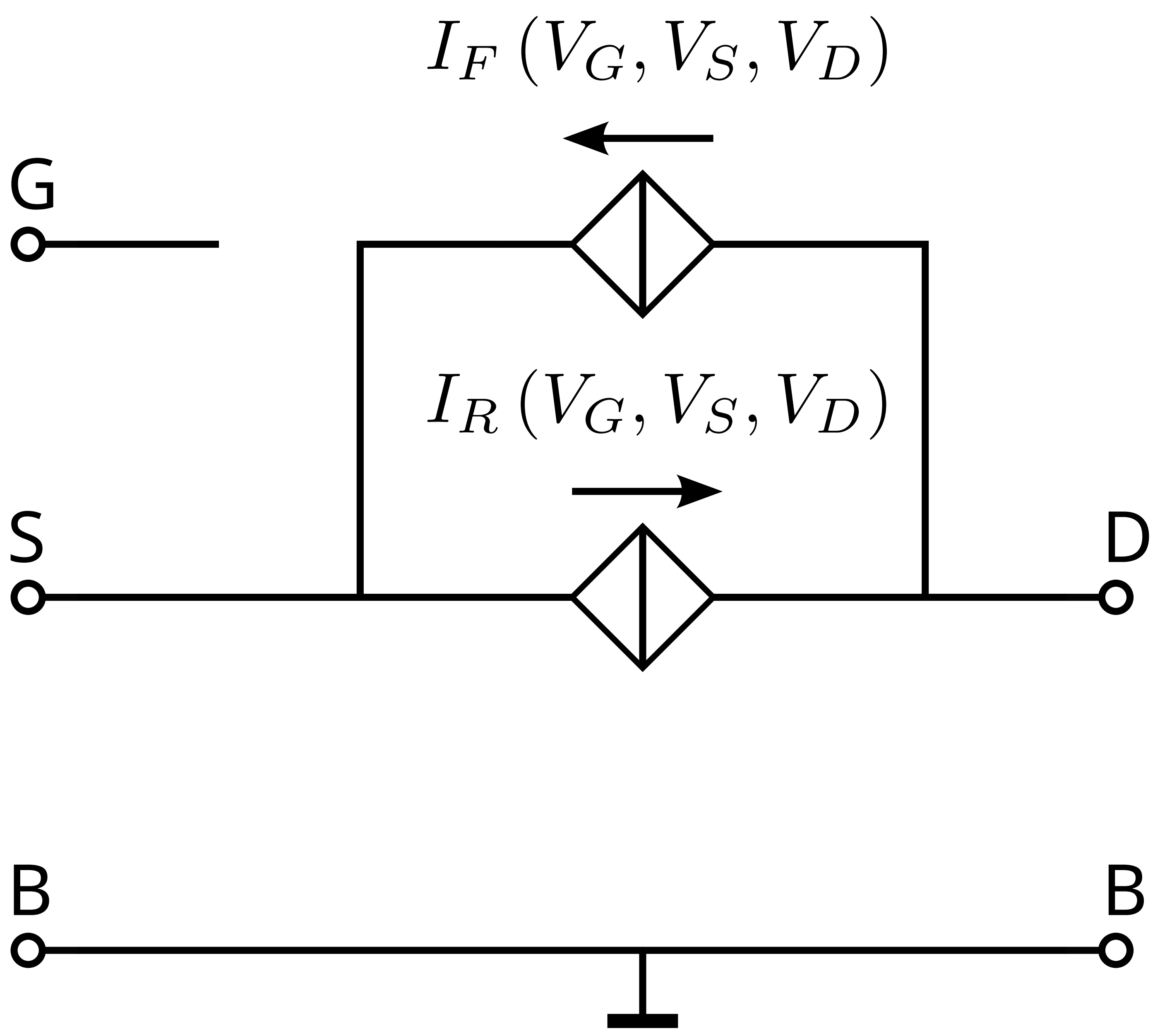
$$IC_{F,R} = F\left(\frac{V_G - V_{T0} - nV_{S,D}}{nU_T}\right) \ \text{[-]}$$

Forward and reverse current:

$$I_{F,R} = 2n\beta_{sq}U_T^2\frac{W}{L}IC_{F,R} \ \text{[A]}$$

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



$$F(x) = \left(\ln\left(1+\exp\left(\tfrac{x}{2}\right)\right)\right)^2 \;[\text{-}]$$

this yields: $\begin{cases} \exp(x) & \text{if } x \ll 0, \\ \left(\frac{x}{2}\right)^2 & \text{if } x \gg 0. \end{cases}$

Forward and reverse inversion coefficient:

$$IC_{F,R} = F\left(\frac{V_G - V_{T0} - nV_{S,D}}{nU_T}\right) \;[\text{-}]$$

Forward and reverse current:

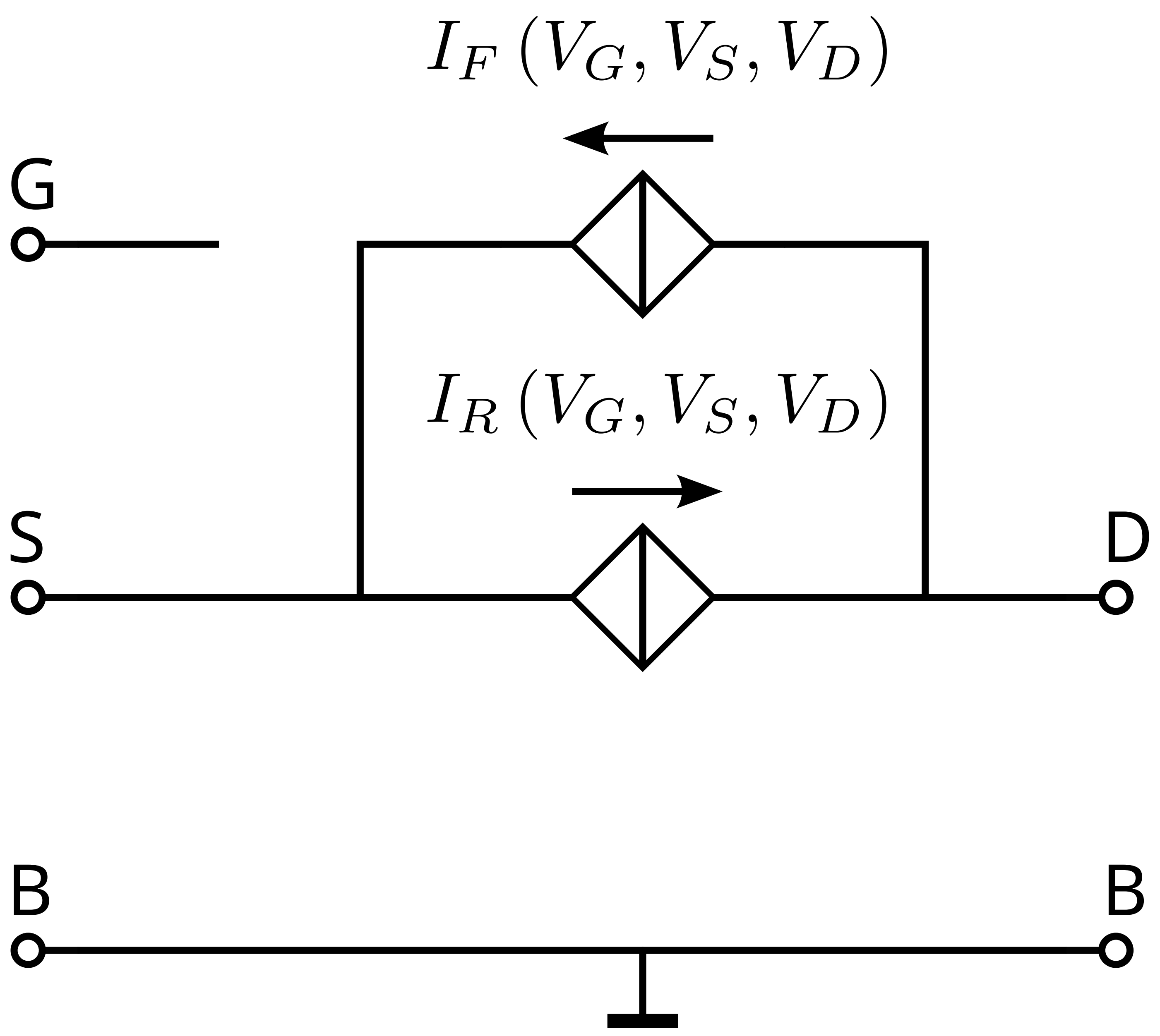
$$I_{F,R} = 2n\beta_{sq}U_T^2\frac{W}{L}IC_{F,R} \;[\mathrm{A}]$$

Transconductance factor:

$$\beta_{sq} = \mu_0 C'_{OX} \;[\mathrm{AV^{-2}m^{-2}}]$$

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



$$F(x) = \left(\ln\left(1+\exp\left(\frac{x}{2}\right)\right)\right)^2 \text{ [-]}$$

this yields: $\begin{cases} \exp(x) & \text{if } x \ll 0, \\ \left(\frac{x}{2}\right)^2 & \text{if } x \gg 0. \end{cases}$

Forward and reverse inversion coefficient:

$$IC_{F,R} = F\left(\frac{V_G - V_{T0} - nV_{S,D}}{nU_T}\right) \text{ [-]}$$

Forward and reverse current:

$$I_{F,R} = 2n\beta_{sq}U_T^2\frac{W}{L}IC_{F,R} \text{ [A]}$$

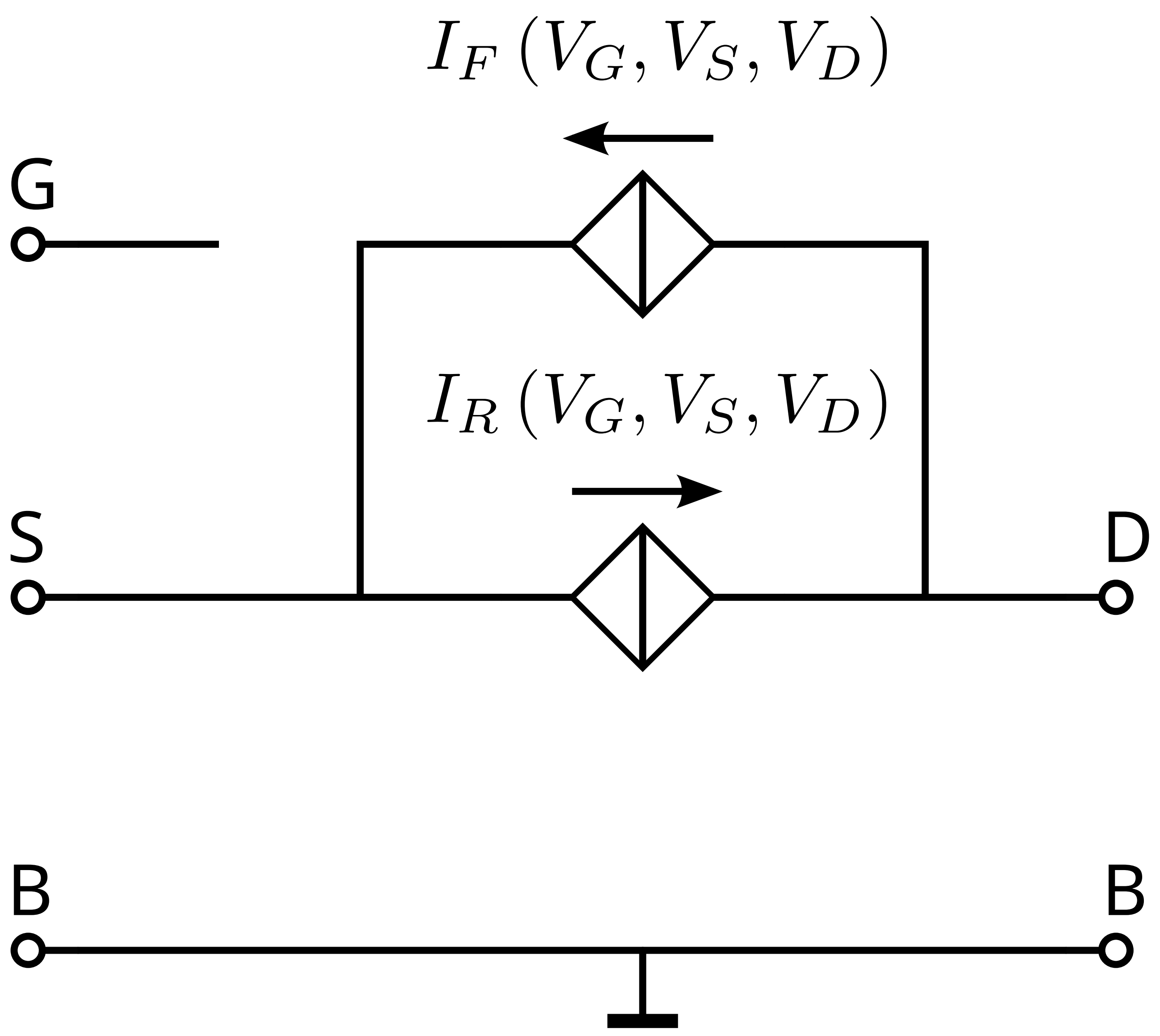
Transconductance factor:

$$\beta_{sq} = \mu_0 C'_{OX} \text{ [AV}^{-2}\text{m}^{-2}\text{]}$$

Total drain current: $I_{DS} = I_F - I_R$ [A]

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



$$F\left(x\right) = \left(\ln\left(1 + \exp\left(\frac{x}{2}\right)\right)\right)^2 \text{ [-]}$$

this yields: $\begin{cases} \exp(x) & \text{if } x \ll 0, \\ \left(\frac{x}{2}\right)^2 & \text{if } x \gg 0. \end{cases}$

Forward and reverse inversion coefficient:

$$IC_{F,R} = F\left(\frac{V_G - V_{T0} - nV_{S,D}}{nU_T}\right) \text{ [-]}$$

Forward and reverse current:

$$I_{F,R} = 2n\beta_{sq}U_T^2\frac{W}{L}IC_{F,R} \ [\mathrm{A}]$$

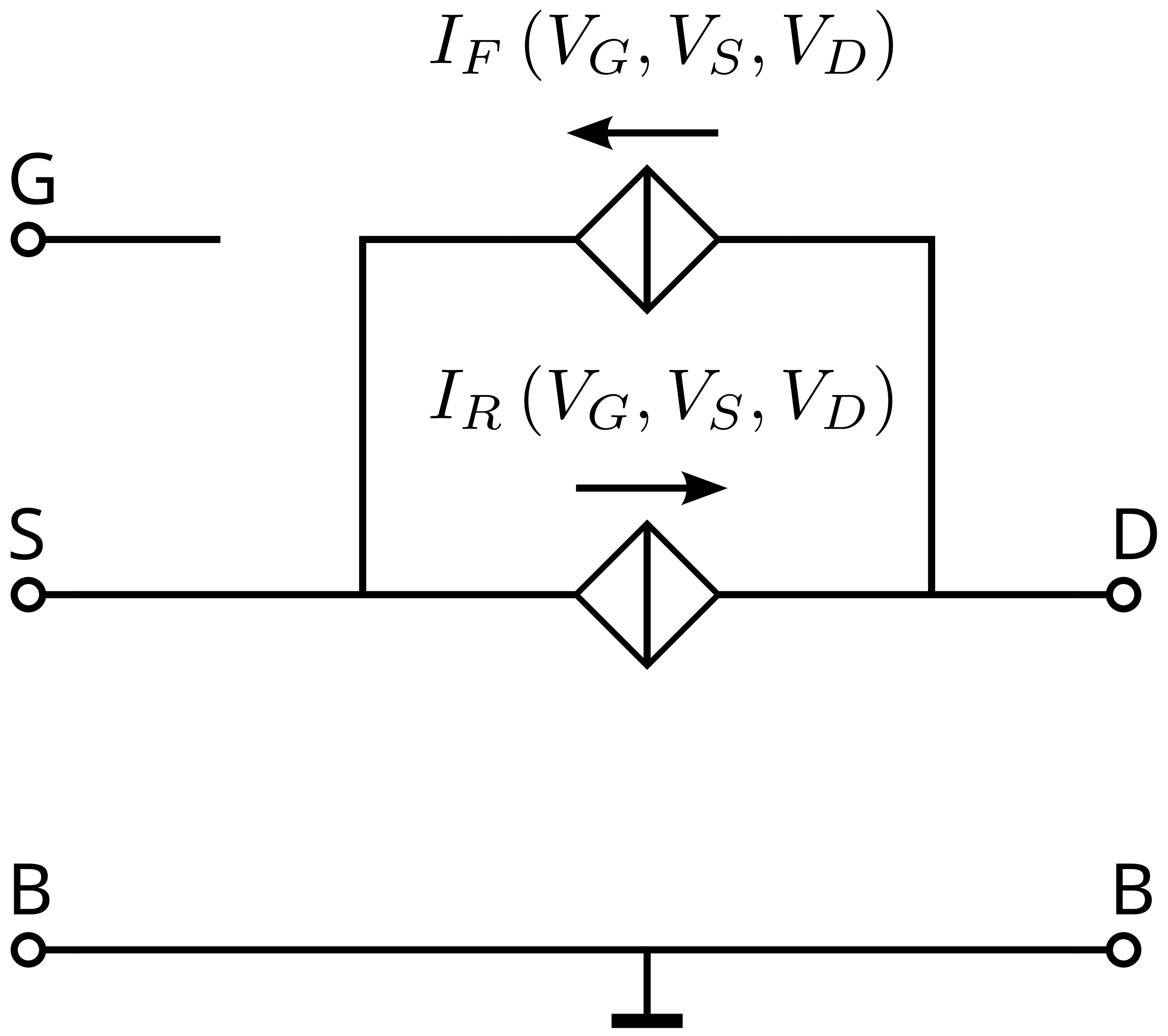
Transconductance factor:

$$\beta_{sq} = \mu_0 C'_{OX} \ [\mathrm{AV^{-2}m^{-2}}]$$

Total drain current: $I_{DS} = I_F - I_R \ [\mathrm{A}]$

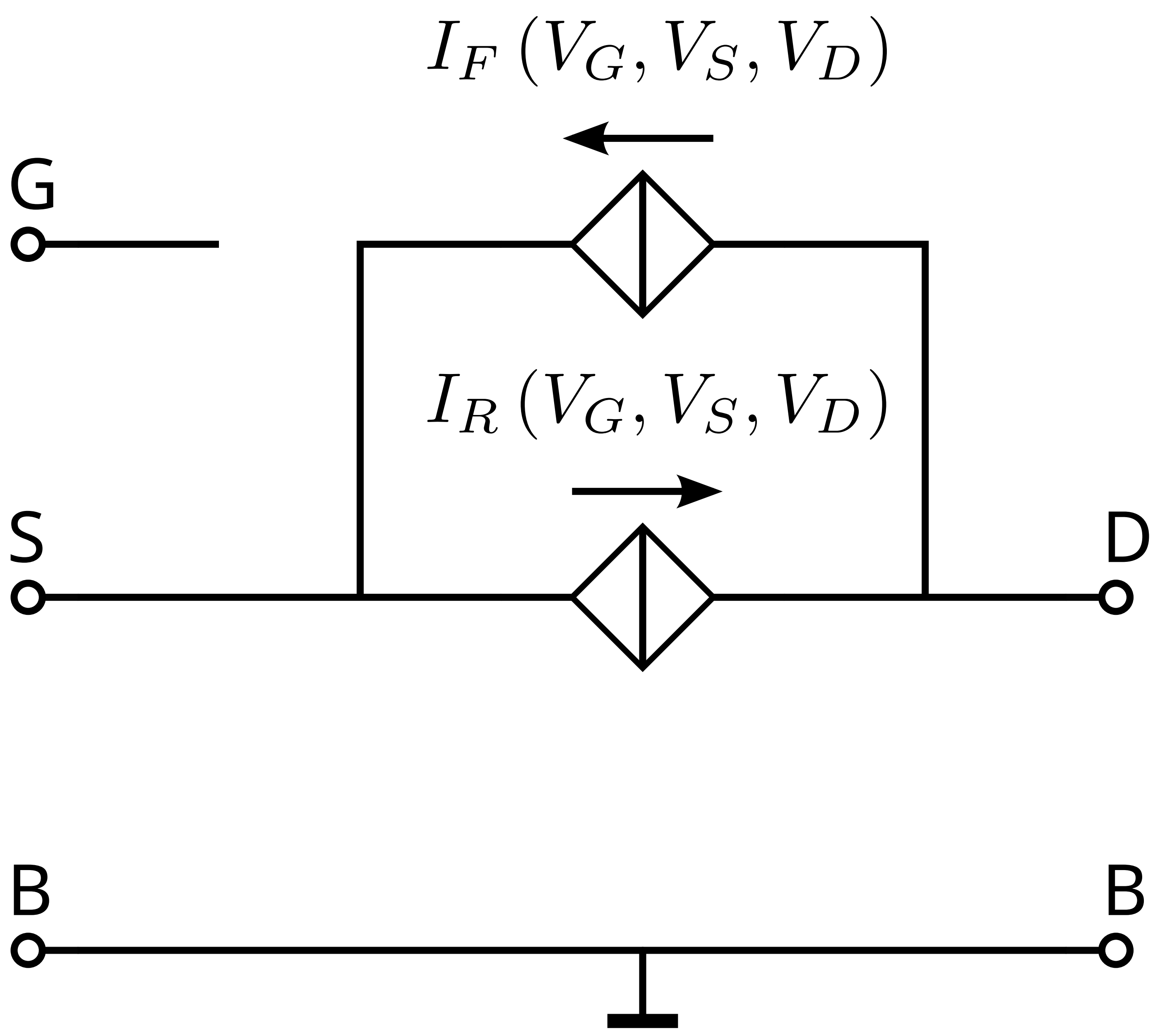
MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



MOS EKV model

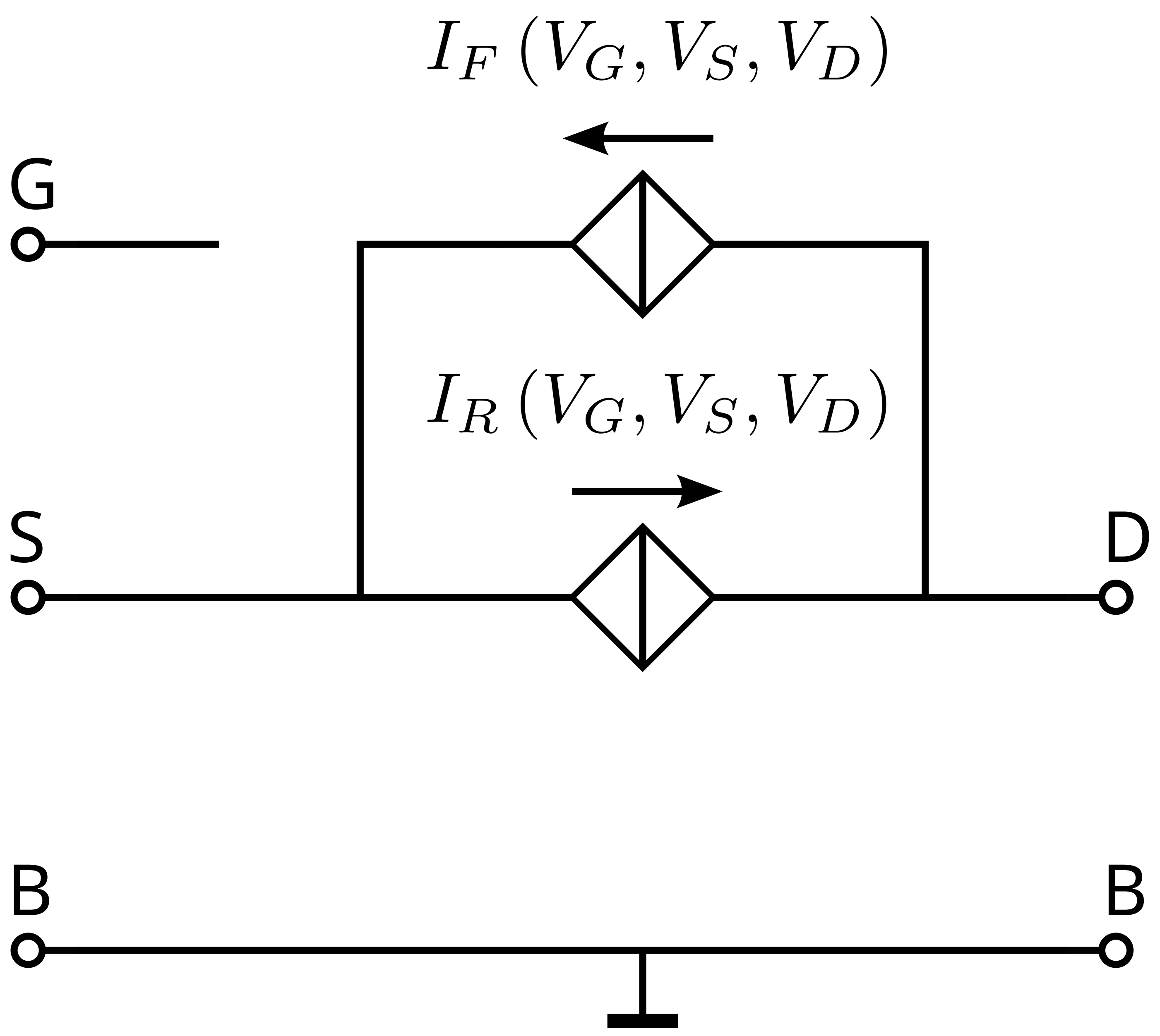
1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



CLM modeled as early voltage
in bipolar transistors

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz

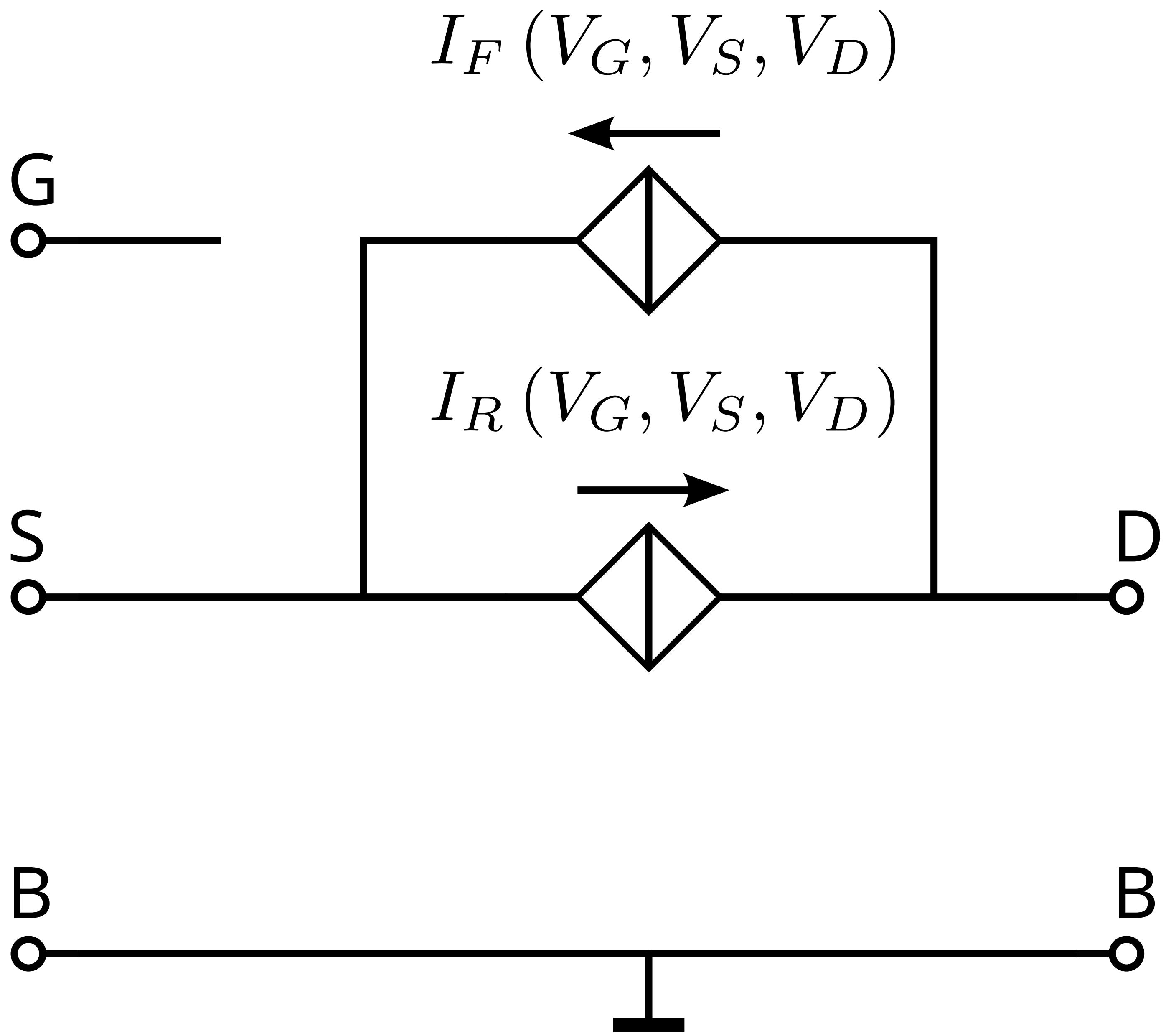


CLM modeled as early voltage
in bipolar transistors

Short-channel effects (VFMR, VS)
modeled as reduction of the
transconductance factor

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



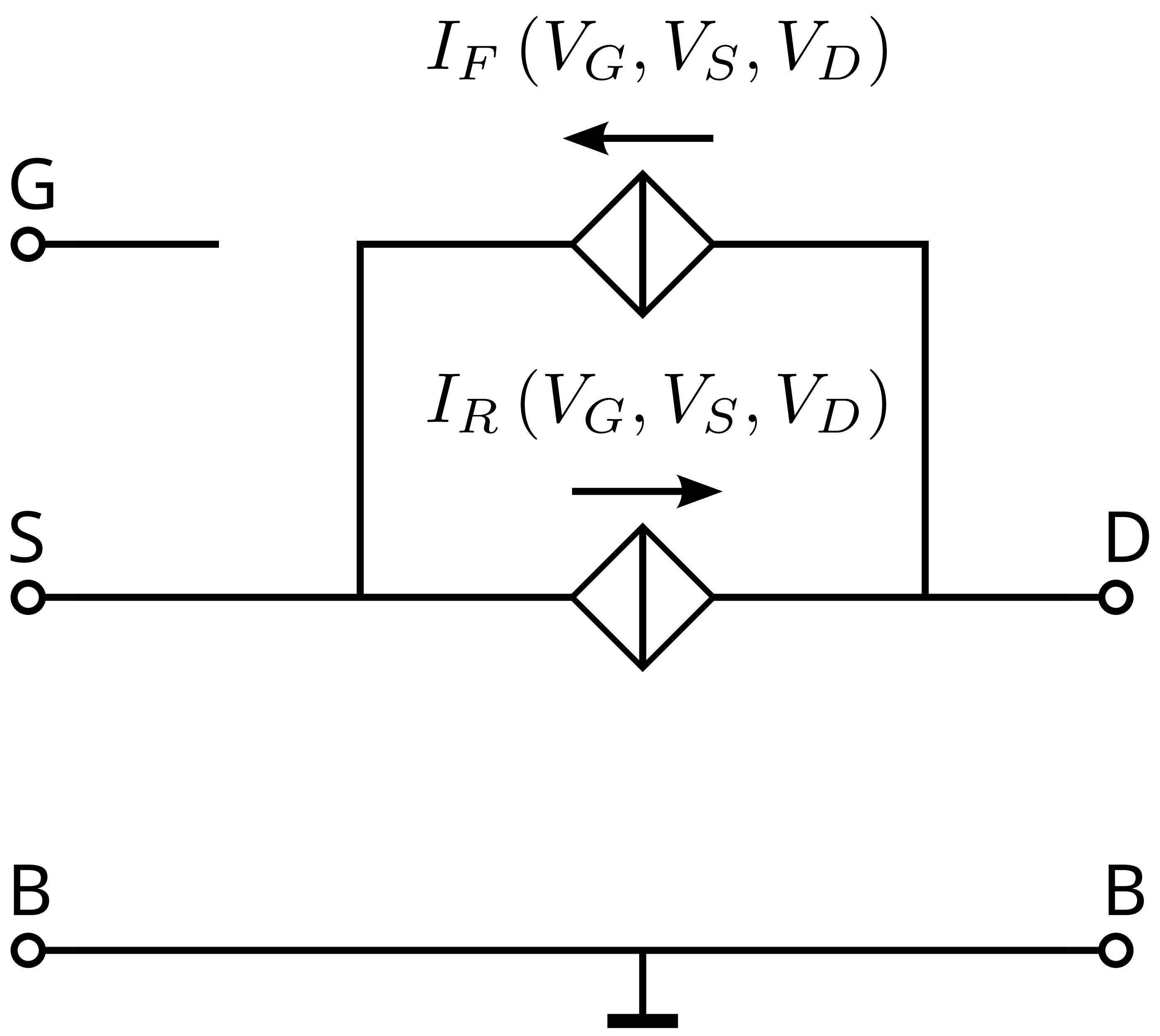
CLM modeled as early voltage
in bipolar transistors

Short-channel effects (VFMR, VS)
modeled as reduction of the
transconductance factor

The critical inversion coefficient
is the value of the inversion coefficient
at which the short-channel effects set in

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



CLM modeled as early voltage
in bipolar transistors

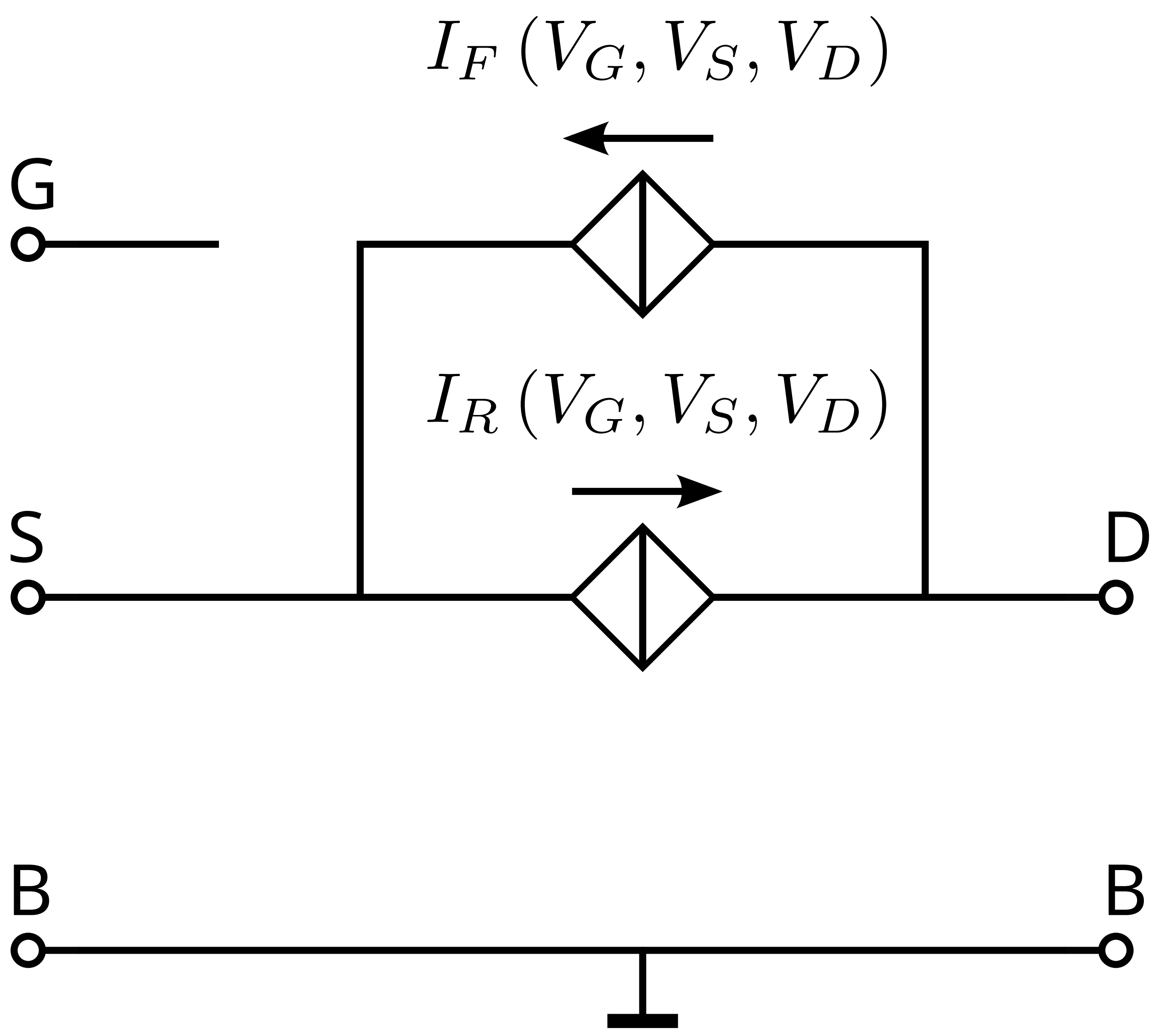
Short-channel effects (VFMR, VS)
modeled as reduction of the
transconductance factor

The critical inversion coefficient
is the value of the inversion coefficient
at which the short-channel effects set in

$$IC_{CRIT} \approx \frac{1}{\left(4nU_T\left(\theta + \frac{1}{L\,E_{CRIT}}\right)\right)^2} \text{ [-]}$$

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



CLM modeled as early voltage
in bipolar transistors

Short-channel effects (VFMR, VS)
modeled as reduction of the
transconductance factor

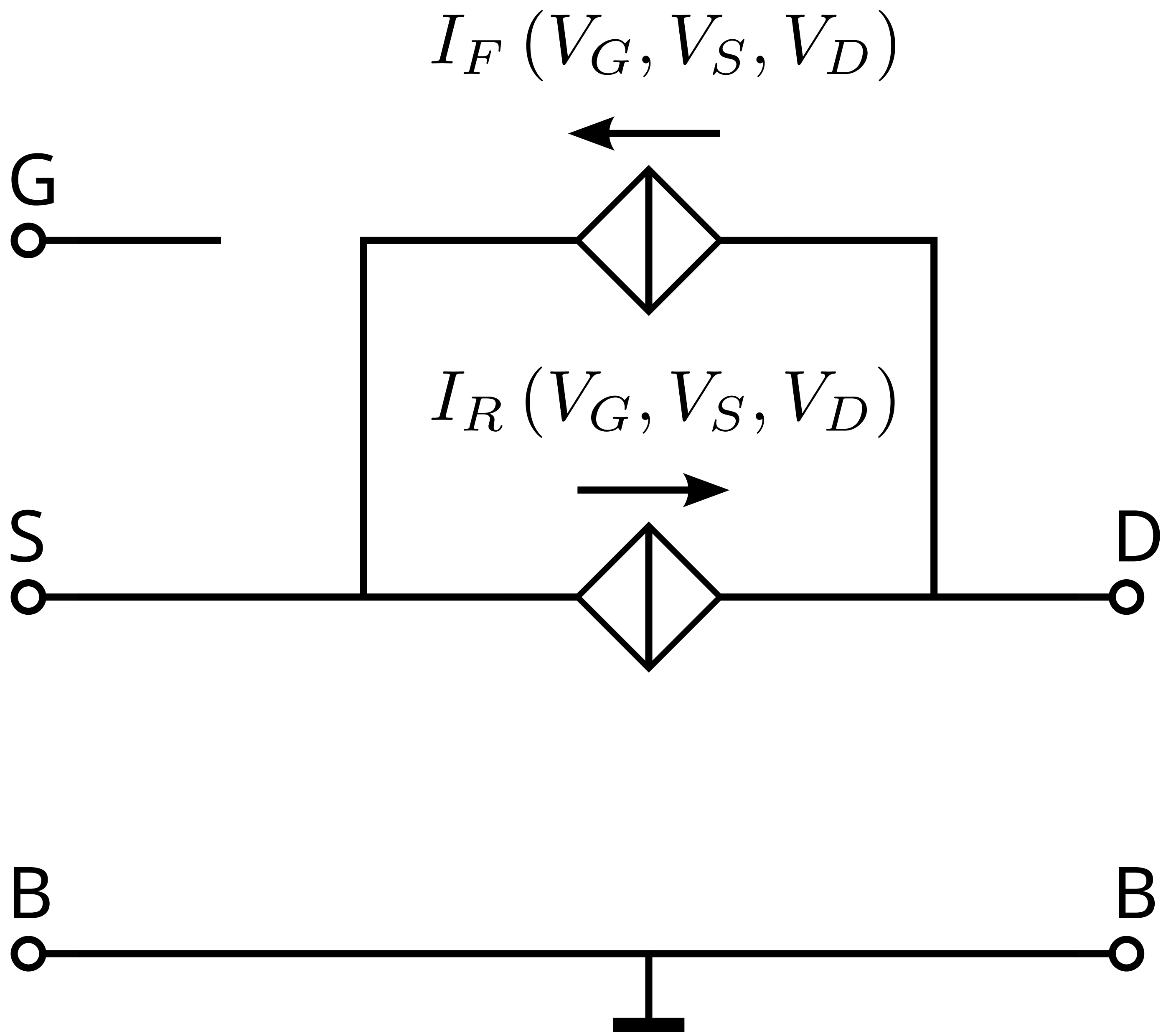
The critical inversion coefficient
is the value of the inversion coefficient
at which the short-channel effects set in

$$IC_{CRIT} \approx \frac{1}{\left(4nU_T\left(\theta+\frac{1}{L\,E_{CRIT}}\right)\right)^2} \quad [-]$$

VFMR coefficient

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



CLM modeled as early voltage
in bipolar transistors

Short-channel effects (VFMR, VS)
modeled as reduction of the
transconductance factor

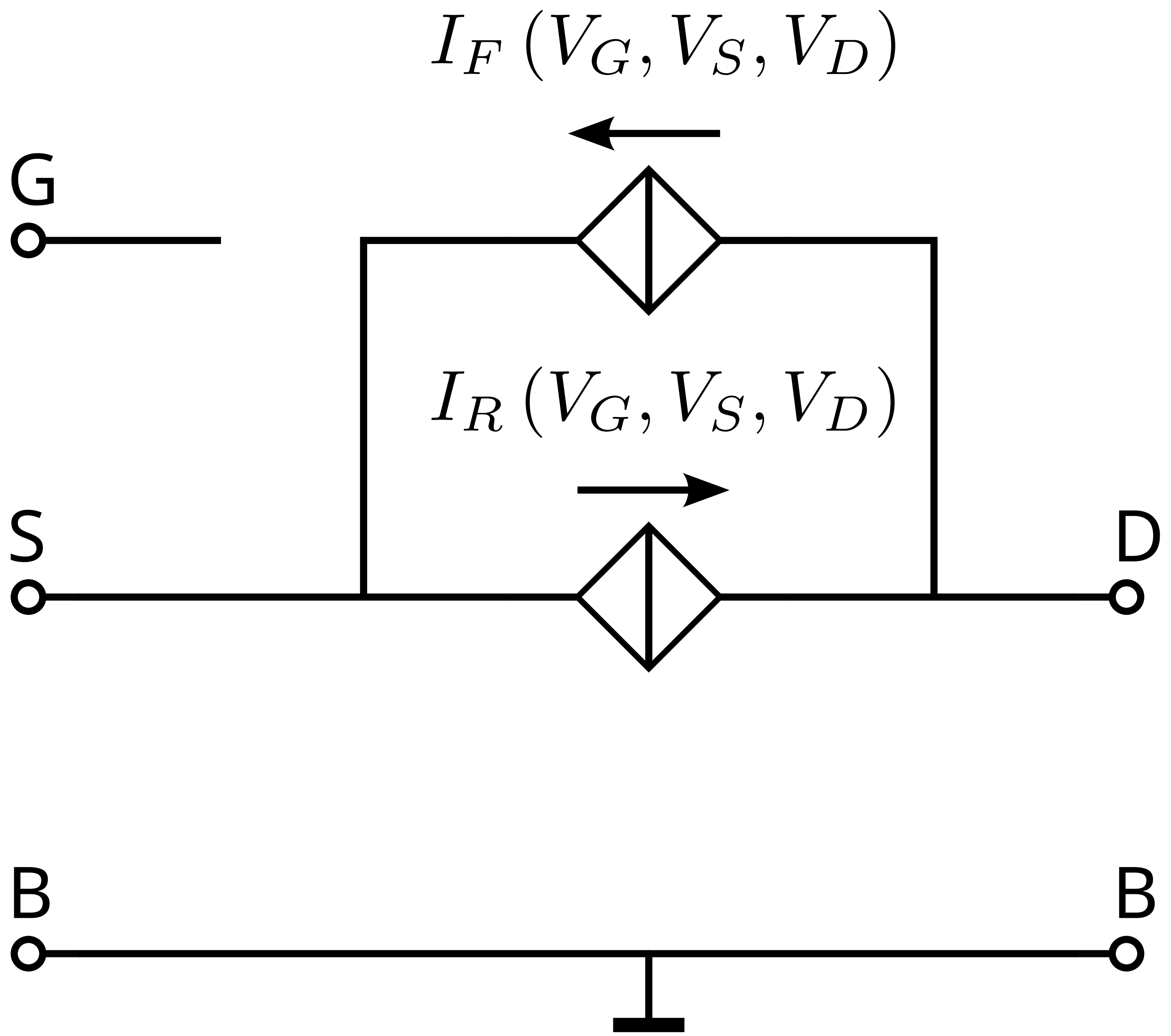
The critical inversion coefficient
is the value of the inversion coefficient
at which the short-channel effects set in

$$IC_{CRIT} \approx \frac{1}{\left(4nU_T\left(\theta + \frac{1}{L\ E_{CRIT}}\right)\right)^2} \quad [\text{-}]$$

VFMR coefficient ↑ ↑critical lateral field strength

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



CLM modeled as early voltage
in bipolar transistors

Short-channel effects (VFMR, VS)
modeled as reduction of the
transconductance factor

The critical inversion coefficient
is the value of the inversion coefficient
at which the short-channel effects set in

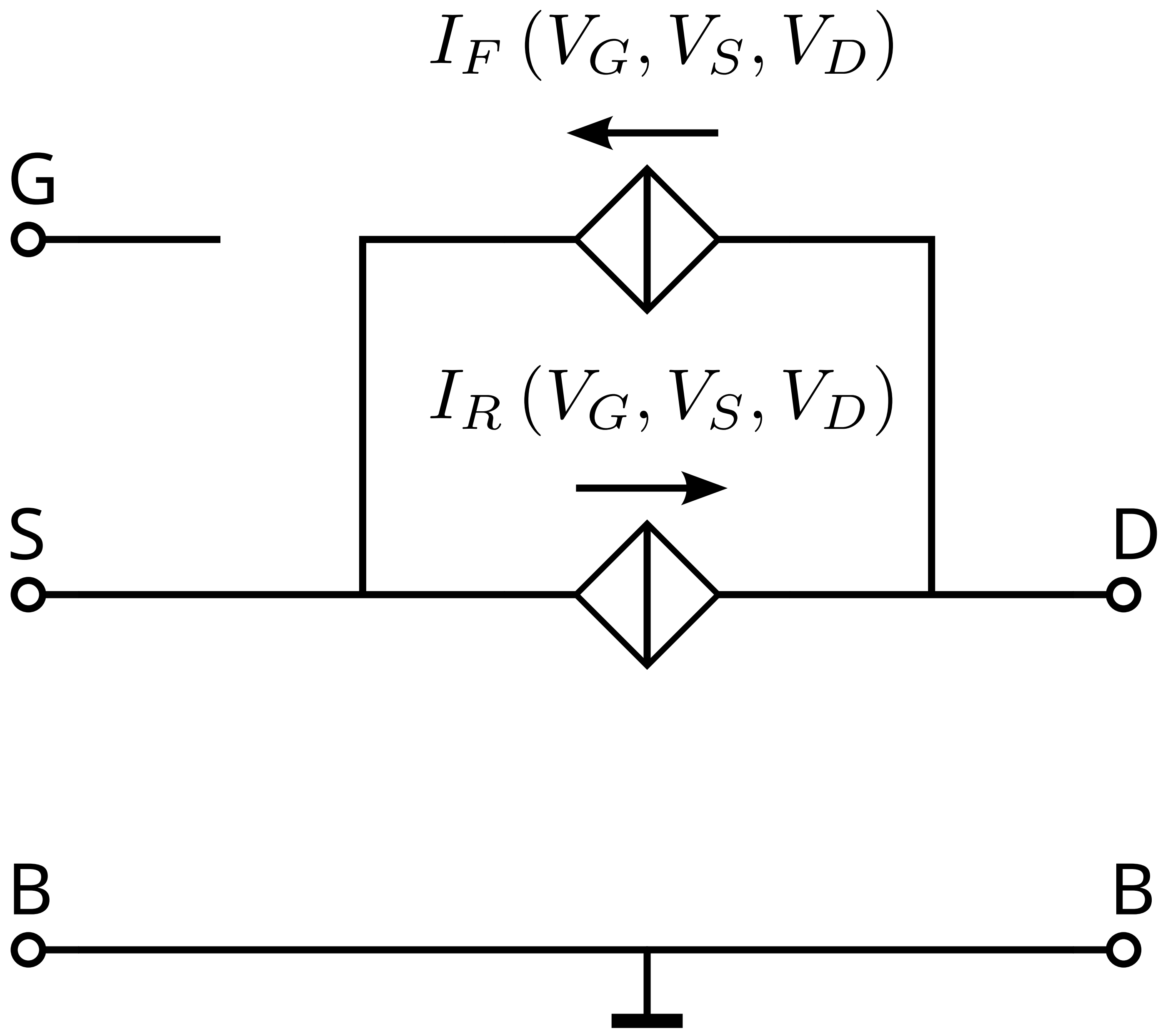
$$IC_{CRIT} \approx \frac{1}{\left(4nU_T\left(\theta+\frac{1}{L\,E_{CRIT}}\right)\right)^2} \quad [\text{-}]$$

VFMR coefficient ↑ ↑critical lateral field strength

Above critical inversion the small-signal transconductance
does not longer significantly increase with the drain current

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz



CLM modeled as early voltage
in bipolar transistors

Short-channel effects (VFMR, VS)
modeled as reduction of the
transconductance factor

The critical inversion coefficient
is the value of the inversion coefficient
at which the short-channel effects set in

$$IC_{CRIT} \approx \frac{1}{\left(4nU_T\left(\theta + \frac{1}{L\,E_{CRIT}}\right)\right)^2} \; [\text{-}]$$

VFMR coefficient critical lateral field strength

Above critical inversion the small-signal transconductance
does not longer significantly increase with the drain current

MOS EKV model

MOS EKV model

Small-signal model
parameters can be expressed
in terms of:

MOS EKV model

Small-signal model parameters can be expressed in terms of:

Technology parameters

MOS EKV model

Small-signal model parameters can be expressed in terms of:

- Technology parameters
- Geometry parameters

MOS EKV model

Small-signal model parameters can be expressed in terms of:

- Technology parameters
- Geometry parameters
- Operating conditions

MOS EKV model

Small-signal model parameters can be expressed in terms of:

- Technology parameters
- Geometry parameters
- Operating conditions

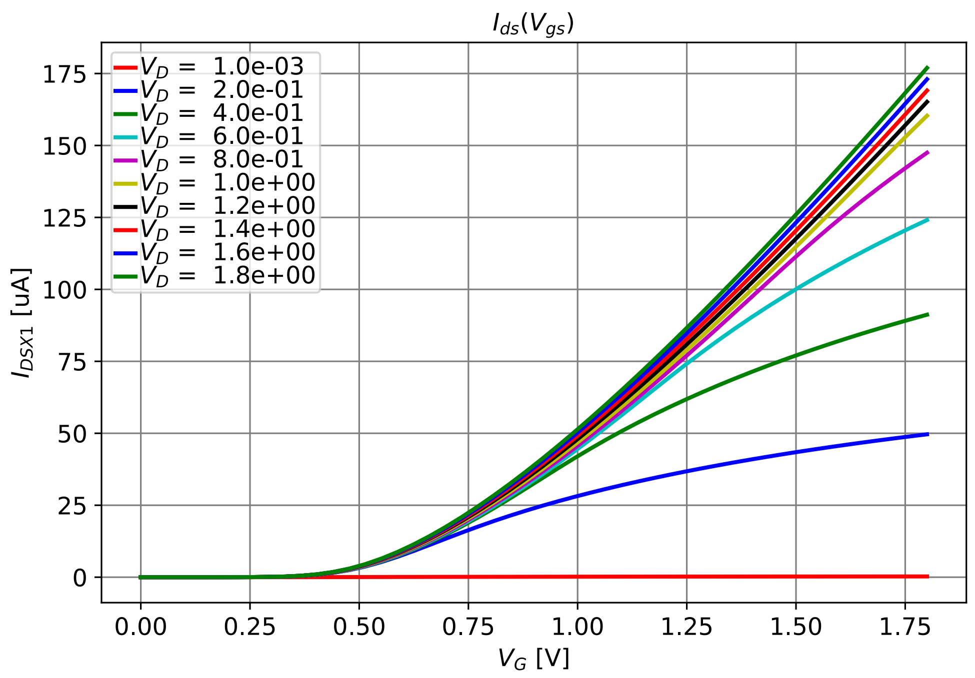
Binkley:
Tradeoffs and Optimization in Analog CMOS Design

MOS EKV model

Small-signal model parameters can be expressed in terms of:

- Technology parameters
- Geometry parameters
- Operating conditions

Binkley:
Tradeoffs and Optimization
in Analog CMOS Design

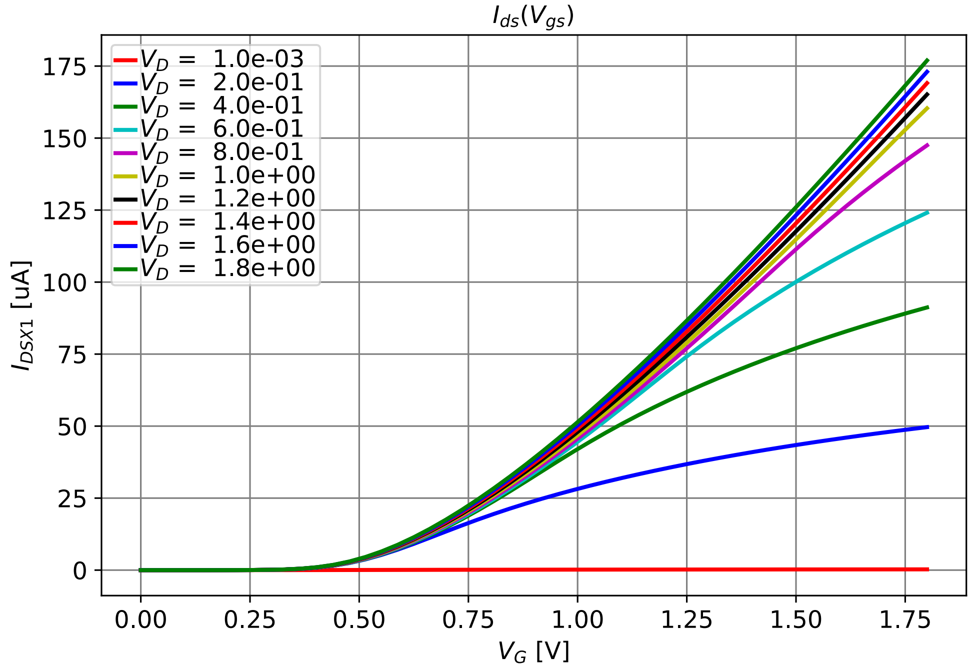


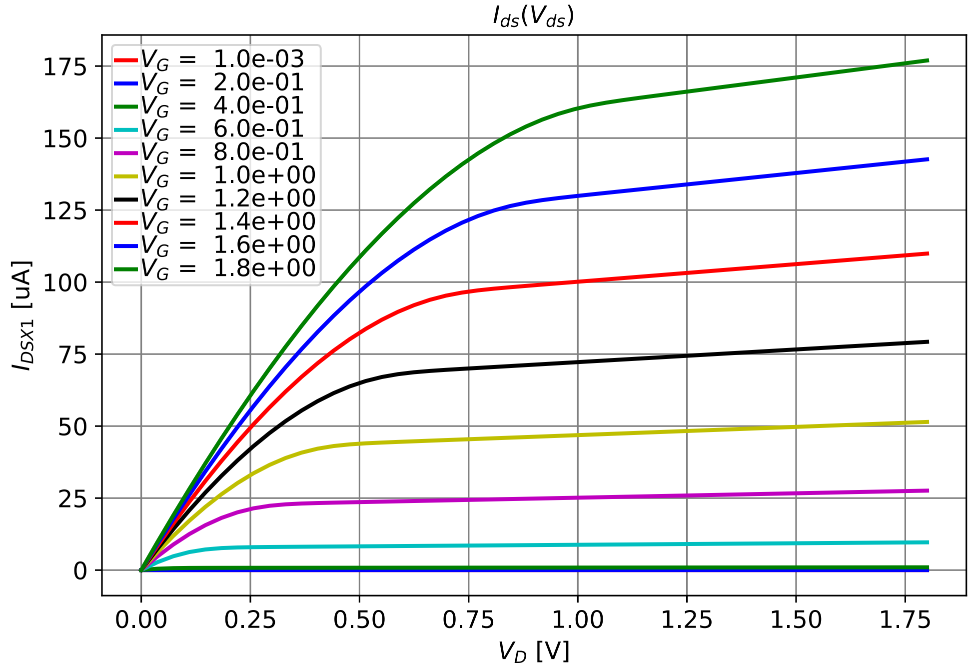
MOS EKV model

Small-signal model parameters can be expressed in terms of:

- Technology parameters
- Geometry parameters
- Operating conditions

Binkley:
Tradeoffs and Optimization in Analog CMOS Design



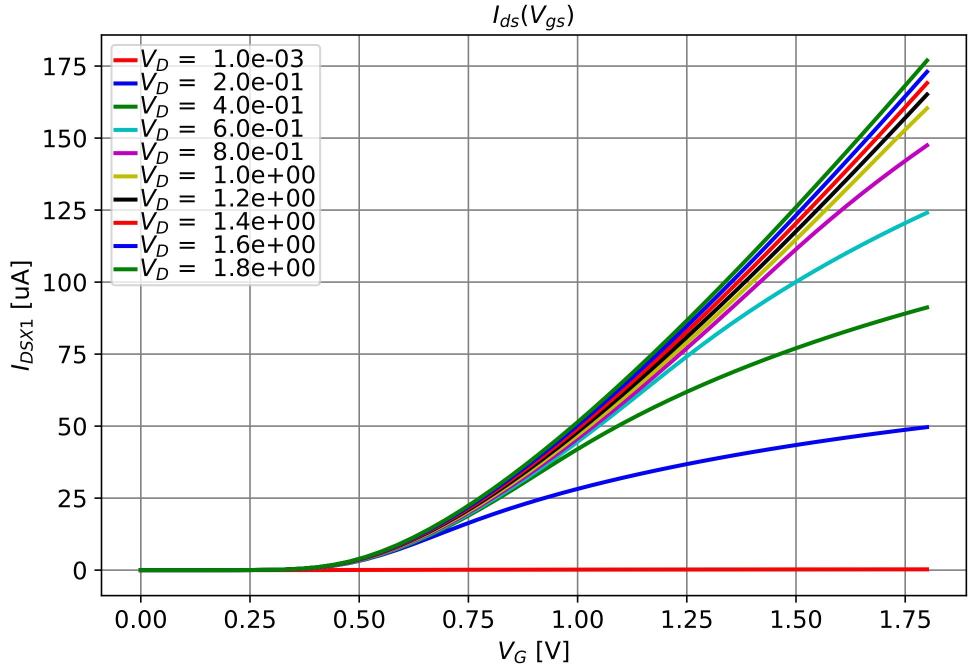


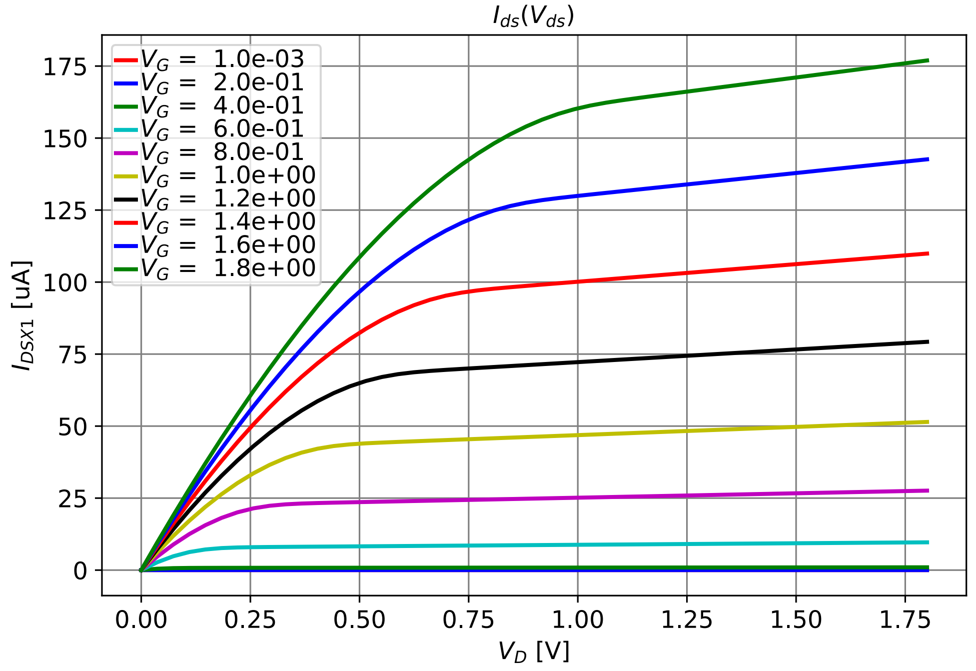
MOS EKV model

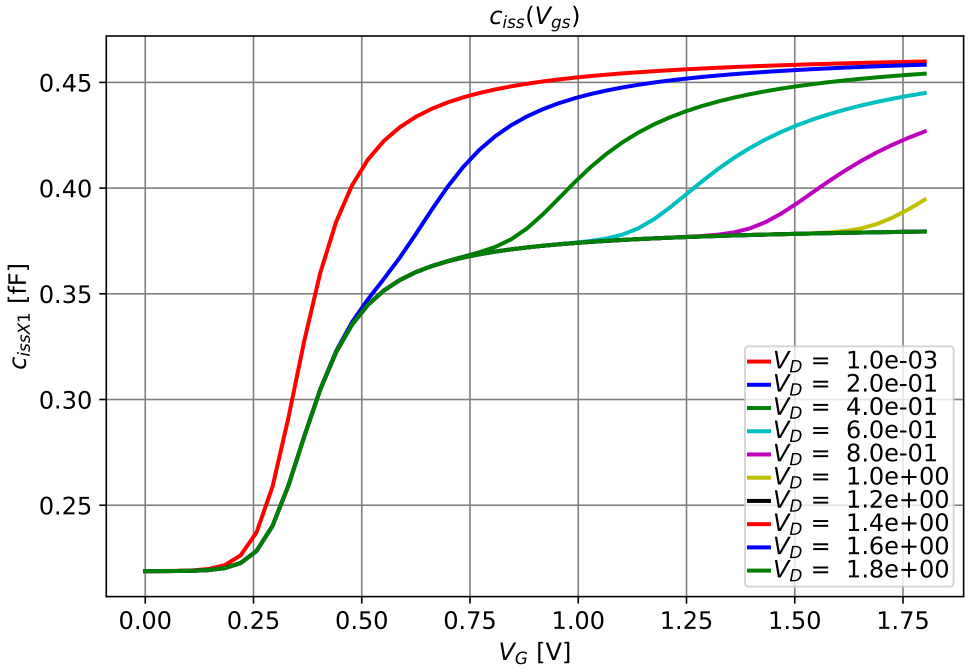
Small-signal model parameters can be expressed in terms of:

- Technology parameters
- Geometry parameters
- Operating conditions

Binkley:
Tradeoffs and Optimization in Analog CMOS Design





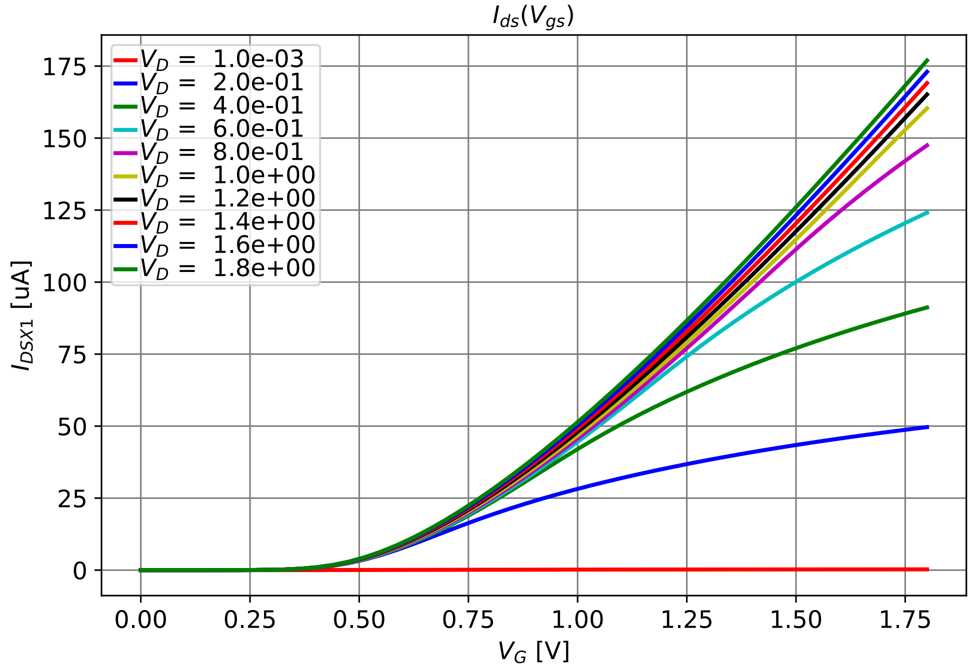


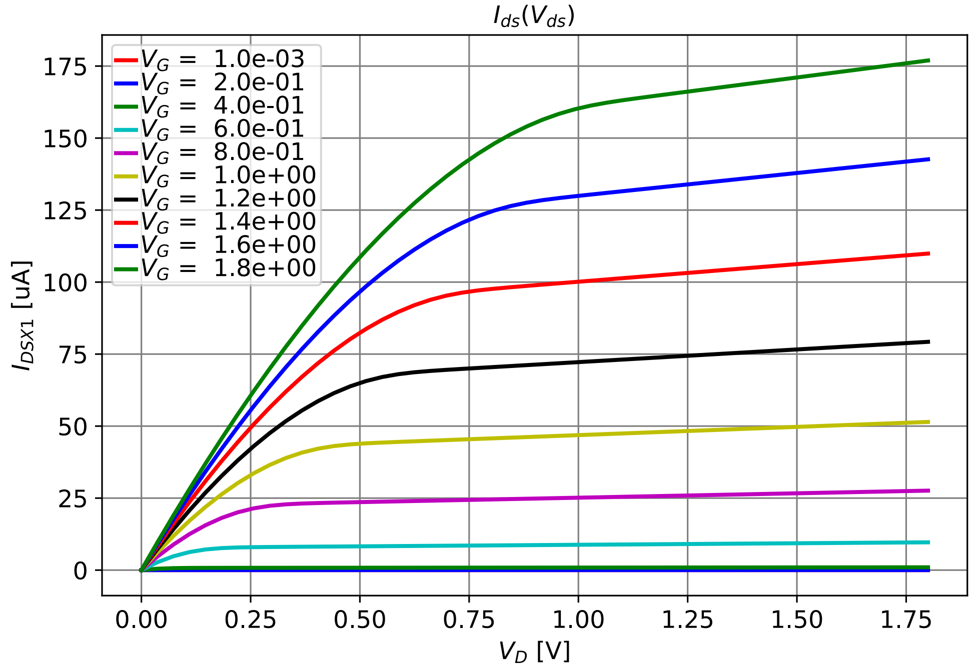
MOS EKV model

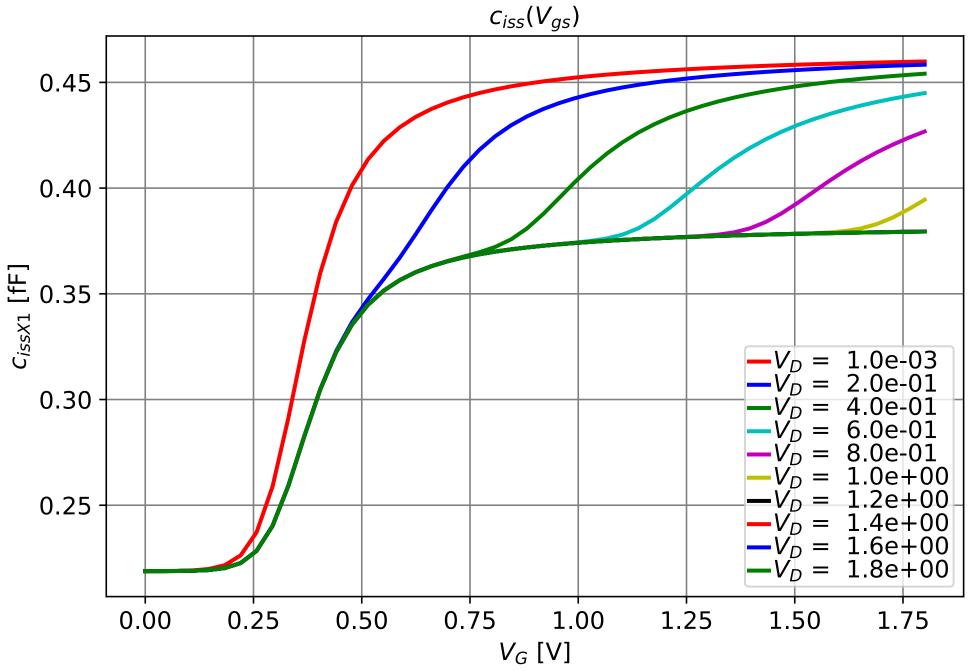
Small-signal model parameters can be expressed in terms of:

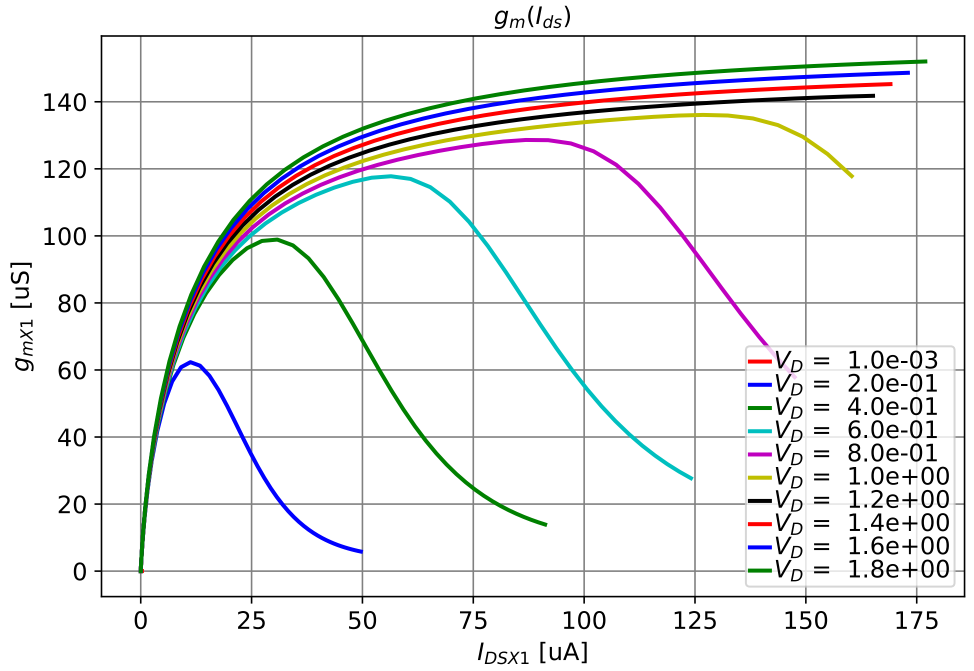
- Technology parameters
- Geometry parameters
- Operating conditions

Binkley:
Tradeoffs and Optimization in Analog CMOS Design







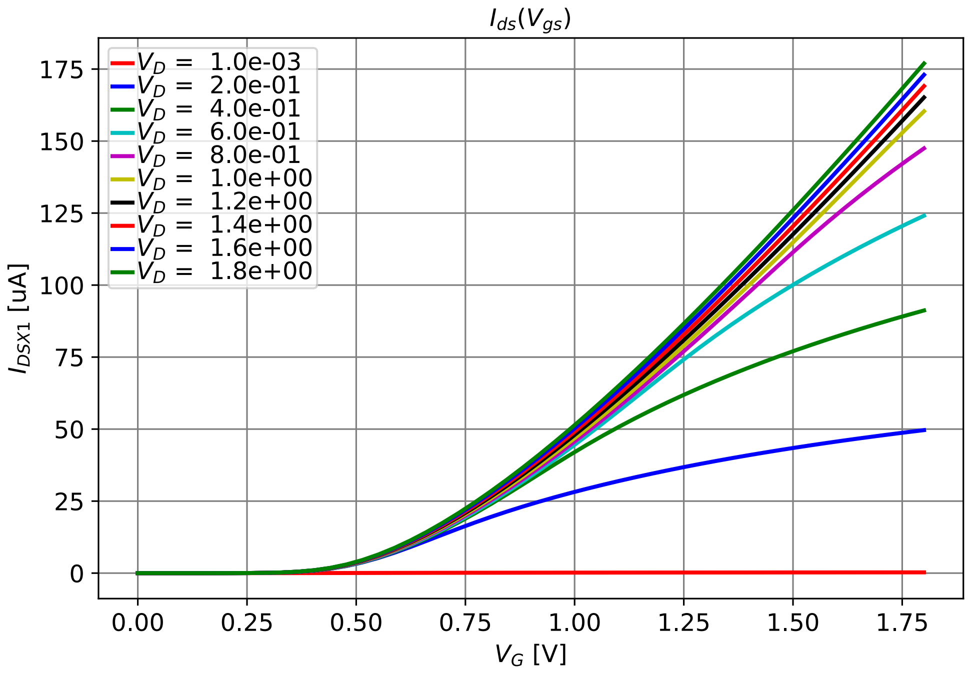


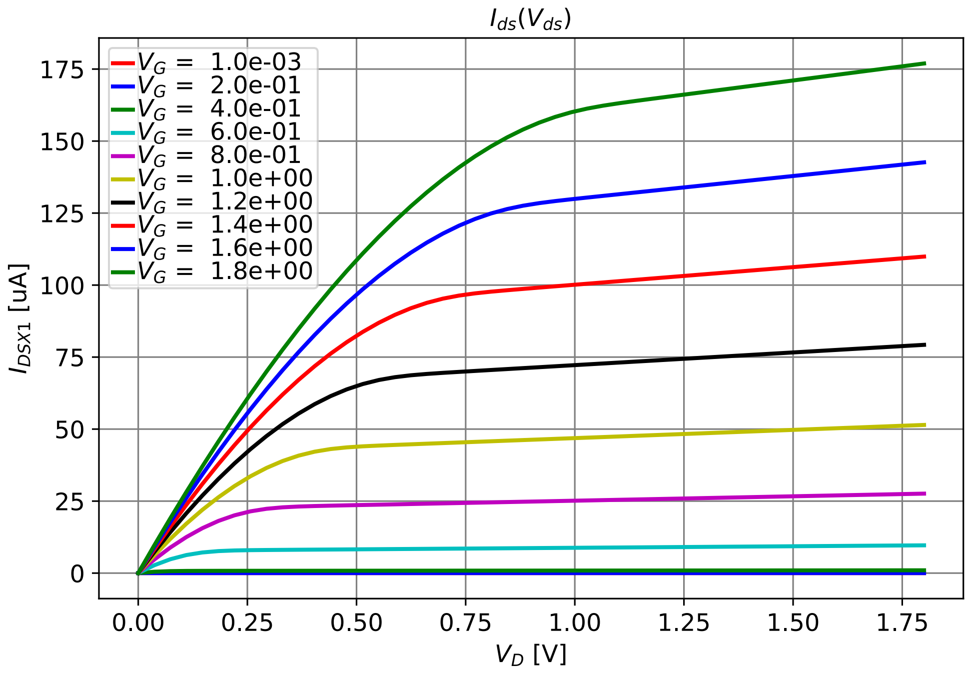
MOS EKV model

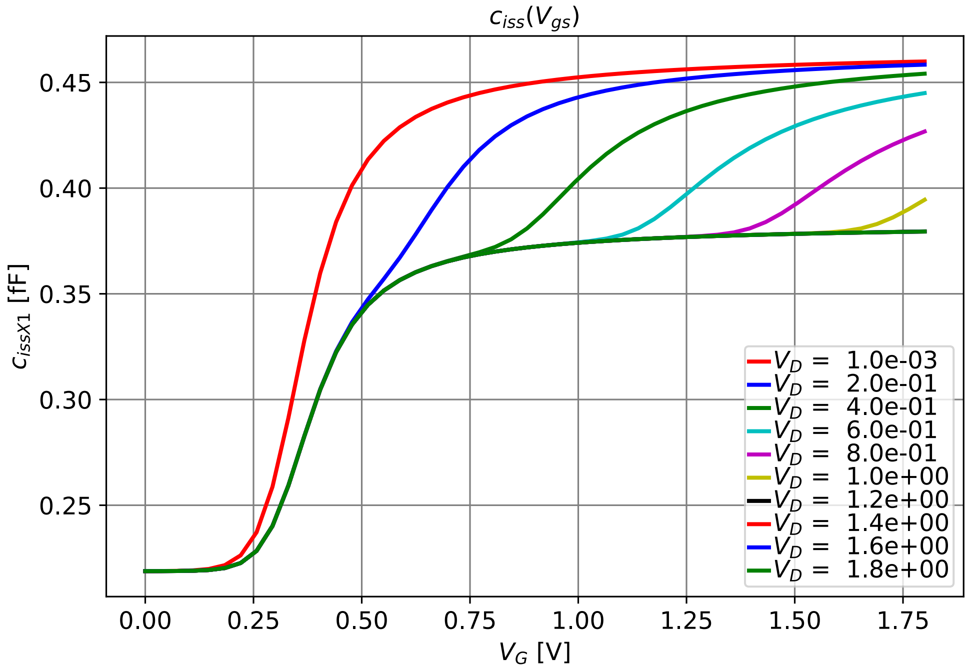
Small-signal model parameters can be expressed in terms of:

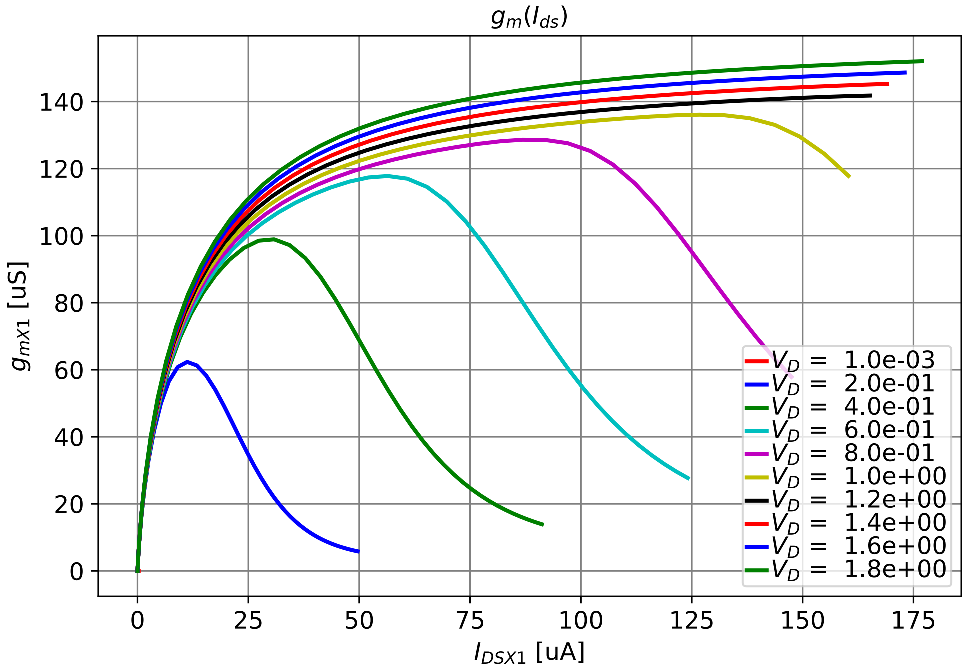
- Technology parameters
- Geometry parameters
- Operating conditions

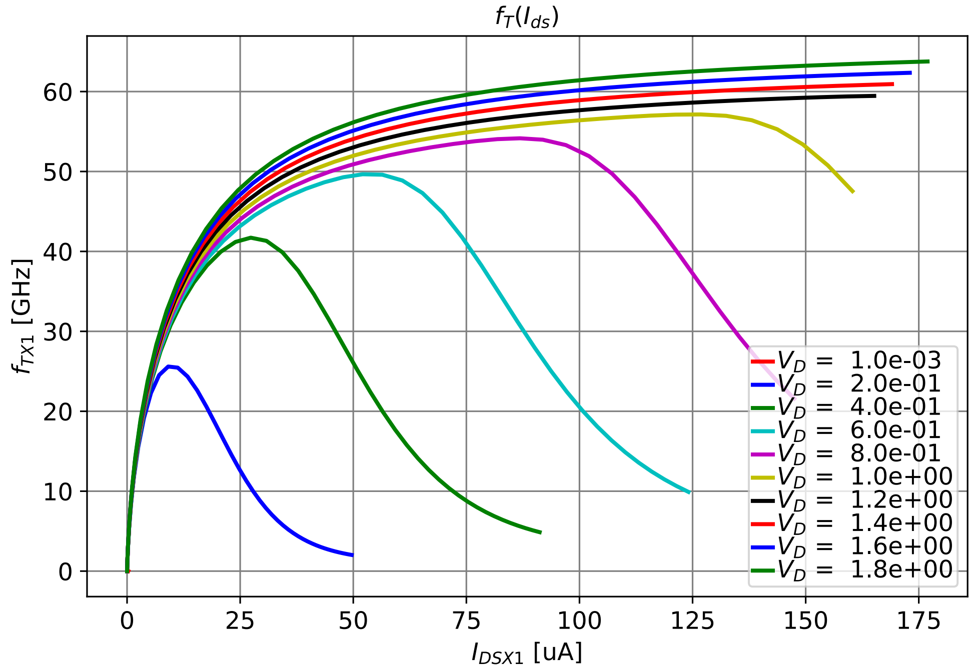
Binkley:
Tradeoffs and Optimization in Analog CMOS Design





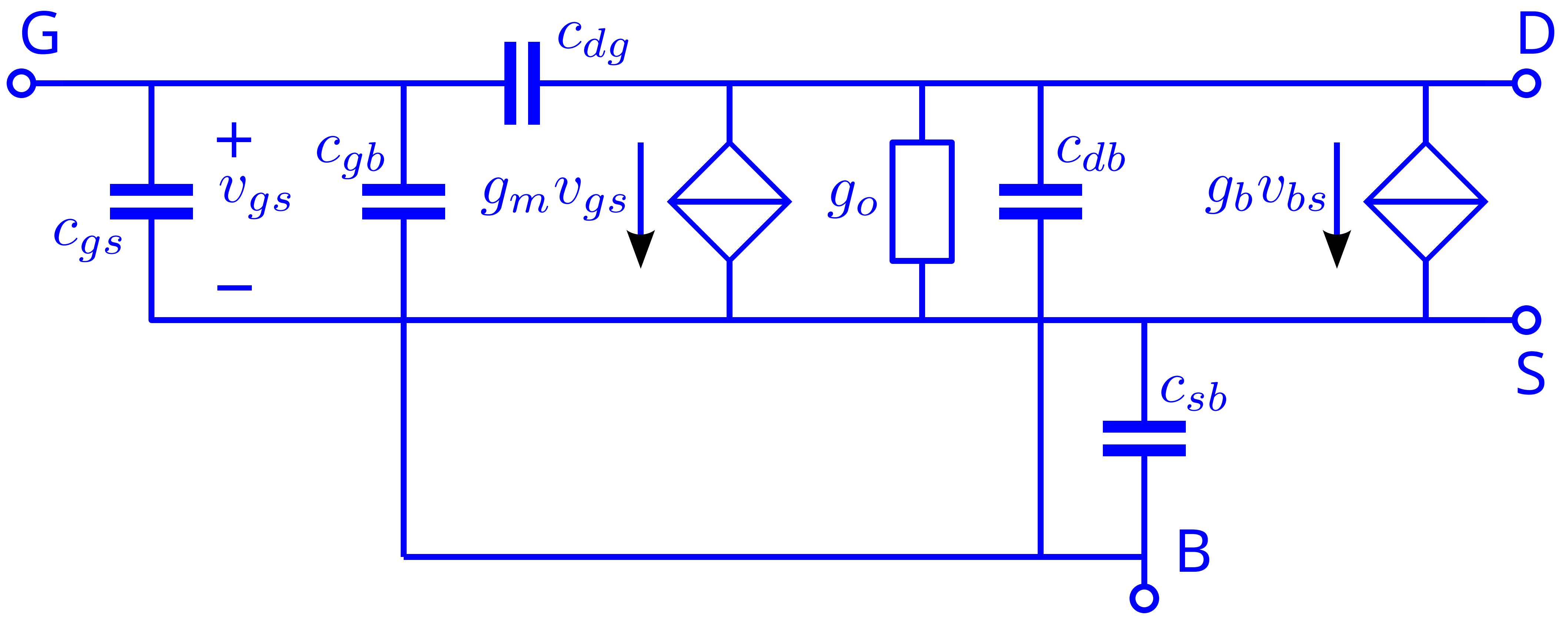




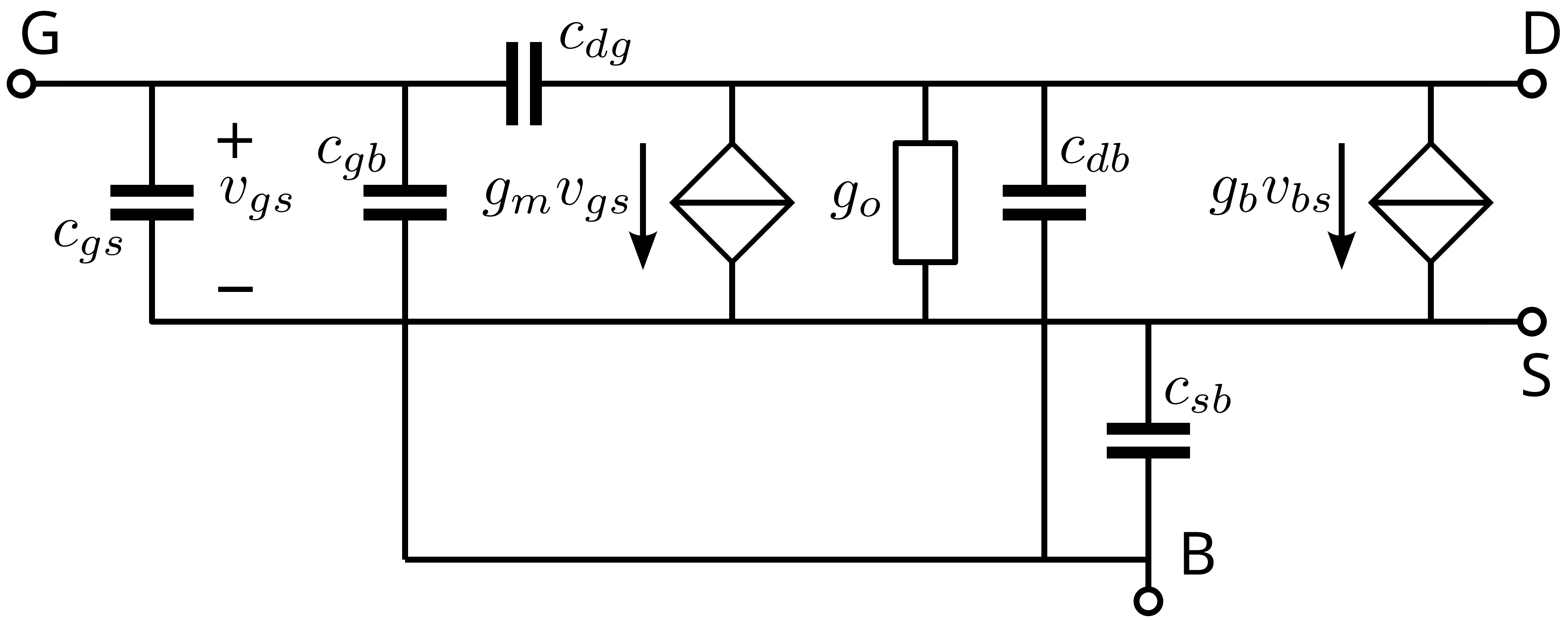


SLiCAP MOS small-signal model

SLiCAP MOS small-signal model

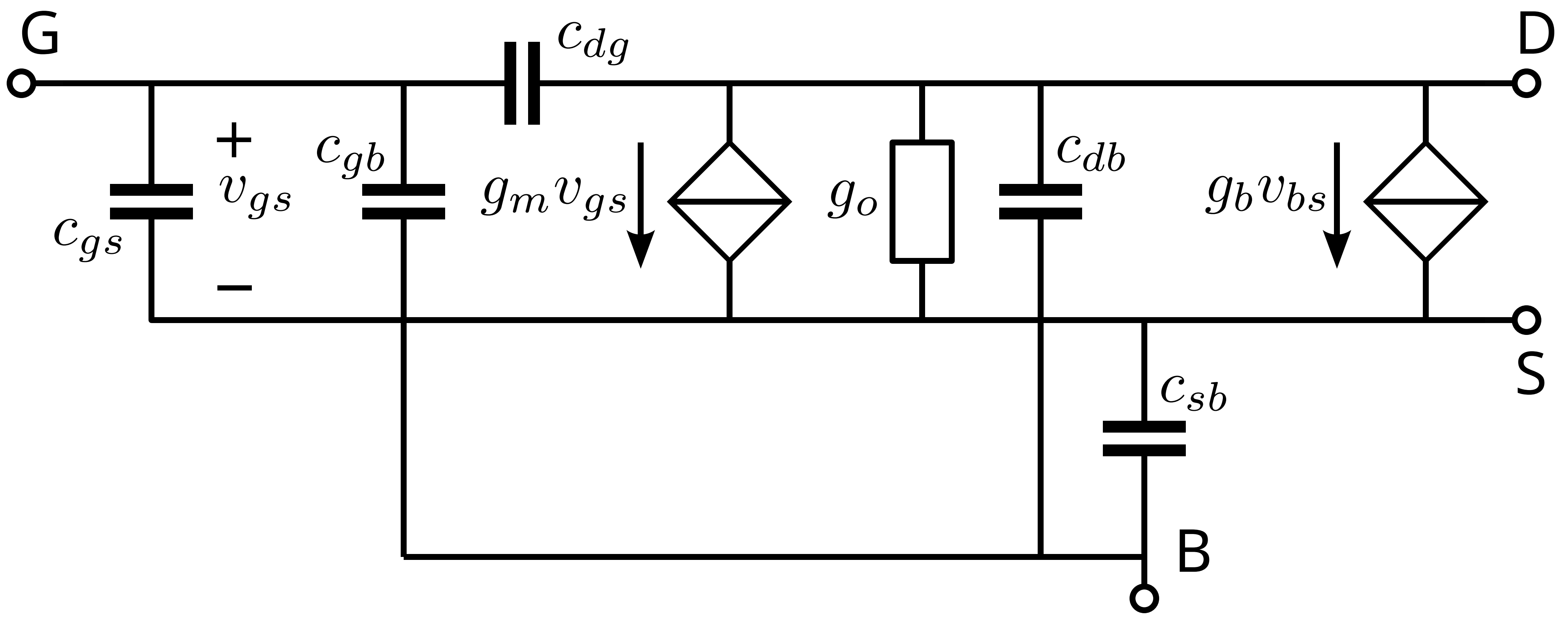


SLiCAP MOS small-signal model



Physical constants in SLiCAPmodels.lib

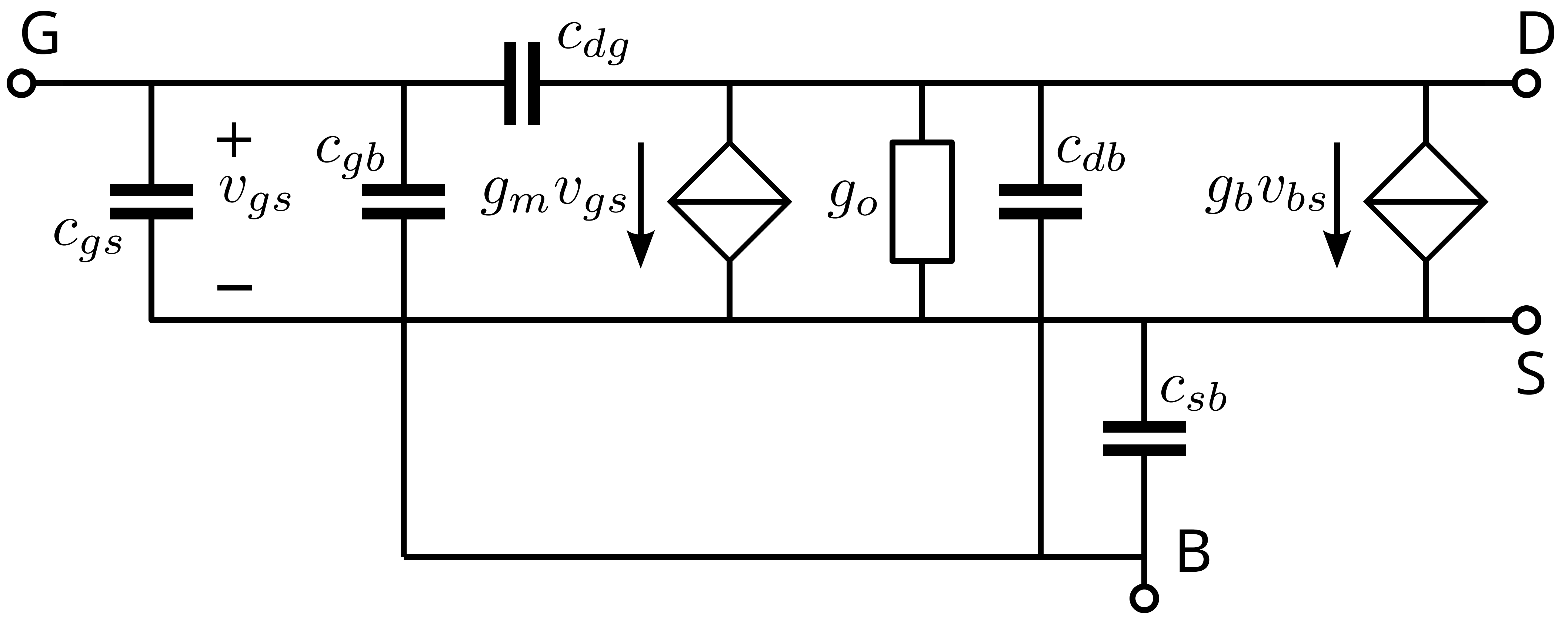
SLiCAP MOS small-signal model



Physical constants in SLiCAPmodels.lib

CMOS18 technology parameters in SLiCAPmodels.lib

SLiCAP MOS small-signal model

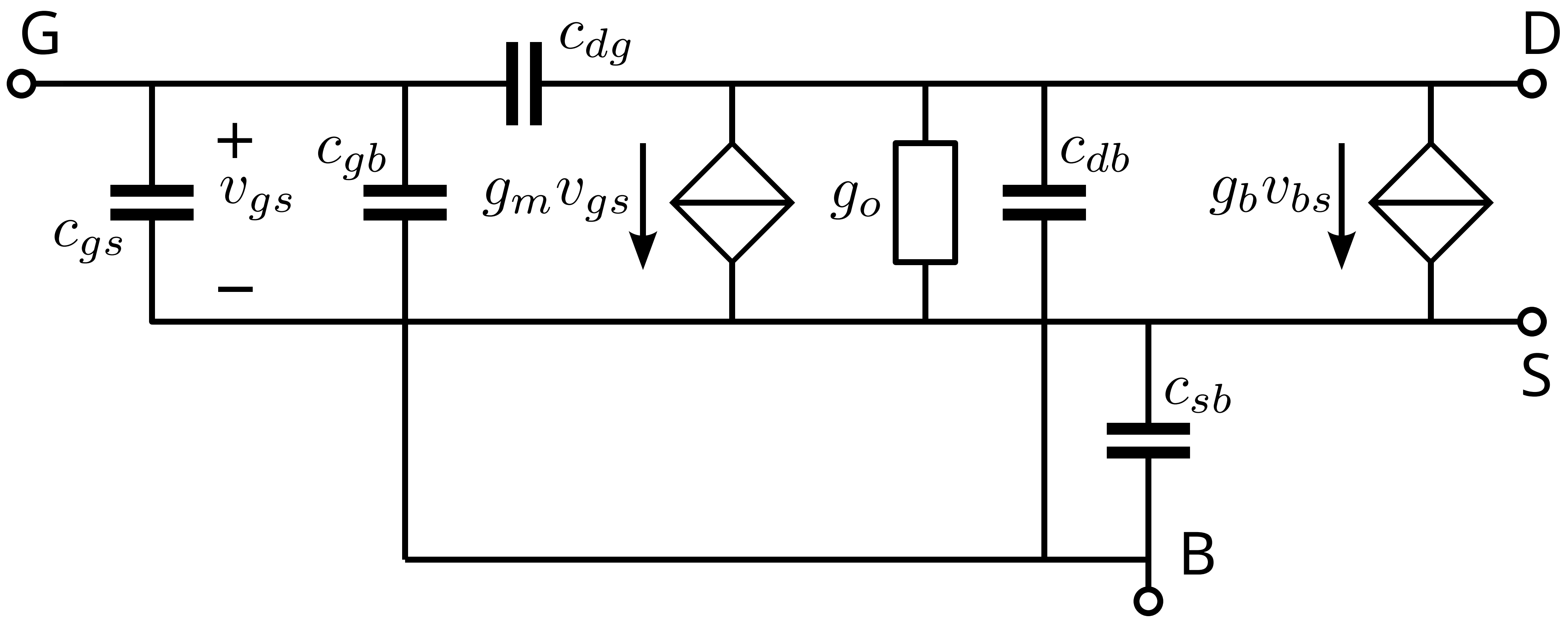


Physical constants in SLiCAPmodels.lib

CMOS18 technology parameters in SLiCAPmodels.lib

Device equations in subcircuit definition of the small signal model in SLiCAP.lib

SLiCAP MOS small-signal model



Physical constants in SLiCAPmodels.lib

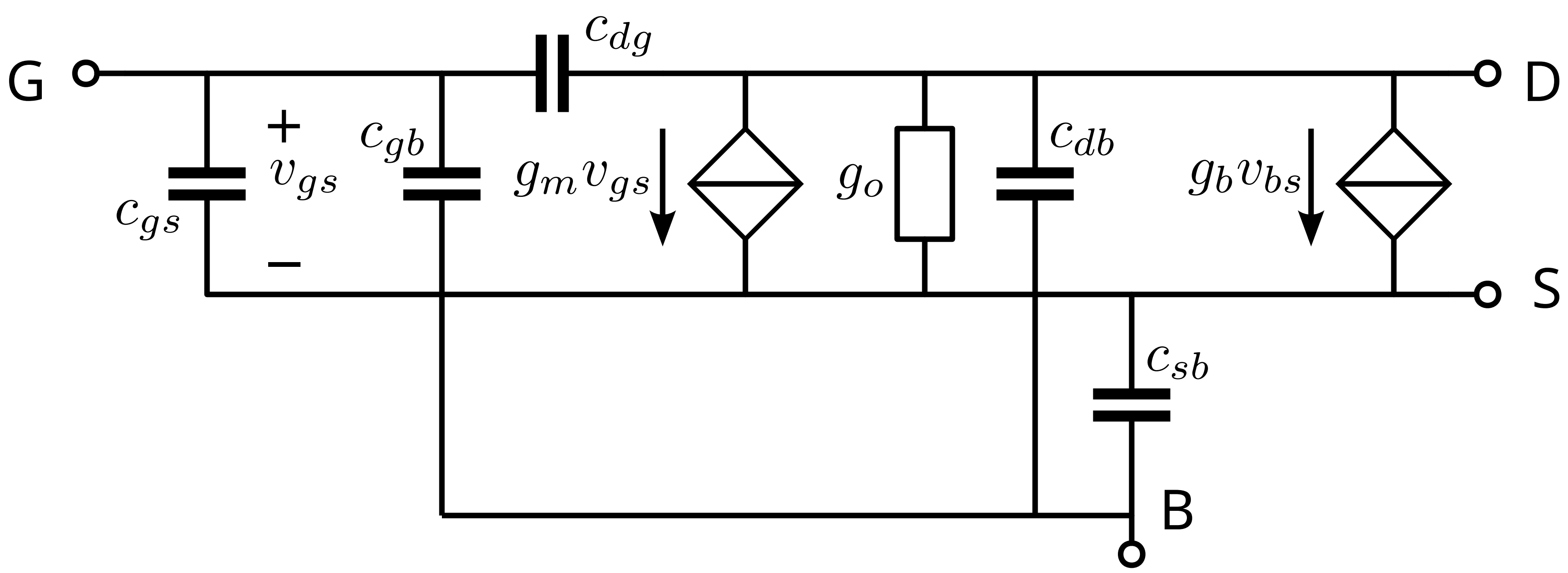
CMOS18 technology parameters in SLiCAPmodels.lib

Device equations in subcircuit definition of the small signal model in SLiCAP.lib

SLiCAP MOS small-signal model

Technology parameters: $n, C_{OX}, I_0, V_{AL}, \Theta, E_{CRIT}, C_{GSO}, C_{GBO}, C_{JBO}$

Circuit parameters: ID, W, L



$$IC' = \frac{ID}{I_0}\frac{W}{L}$$

$$IC = IC'\sqrt{\left(1 + \frac{IC'}{IC_{CRIT}}\right)}$$

$$IC_{CRIT} = \frac{1}{\left(4nU_T\left(\Theta + \frac{1}{E_{CRIT}L}\right)\right)^2}$$

$$g_m = \frac{ID}{4nU_T\sqrt{IC\left(1+\frac{IC}{IC_{CRIT}}\right)+0.5\sqrt{IC\left(1+\frac{IC}{IC_{CRIT}}\right)}}}$$

$$g_o = \frac{g_m n U_T\sqrt{1+\frac{IC}{IC_{CRIT}}}}{V_{AL}L}$$

$$g_b = g_m\left(n-1\right)$$

$$c_{gs} = \frac{2-x}{3}C_{OX}WL + C_{GSO}W$$

$$c_{dg} = C_{GSO}W$$

$$c_{gb} = \frac{1-x}{3}C_{OX}WL\frac{n-1}{n} + C_{GBO}2L$$

$$c_{db} = C_{JB0}L_{DS}W$$

$$c_{sb} = C_{JB0}L_{DS}W$$

$$x = \frac{\sqrt{IC+0.25}+1.5}{\left(\sqrt{IC+0.25}+0.5\right)^2}$$