Structured Electronic Design

MOS EKV model

Anton J.M. Montagne

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MOS operation

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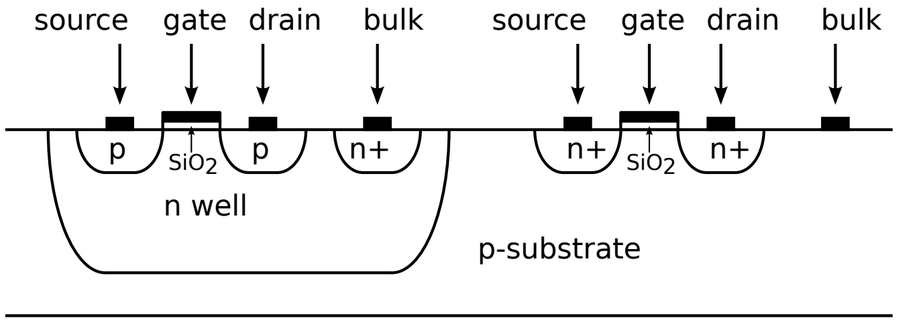
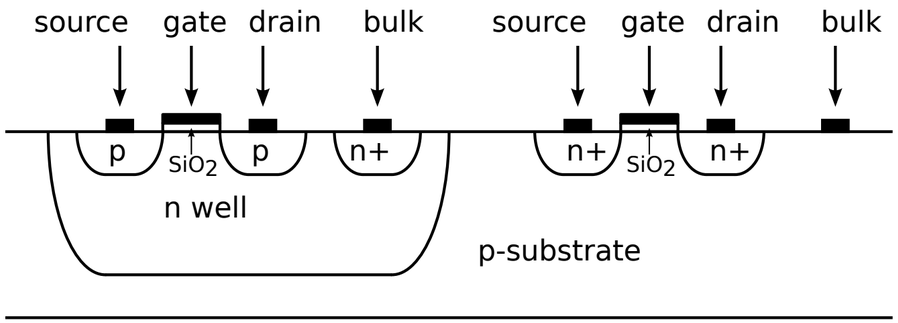
MOS operation



MOS operation

PMOS



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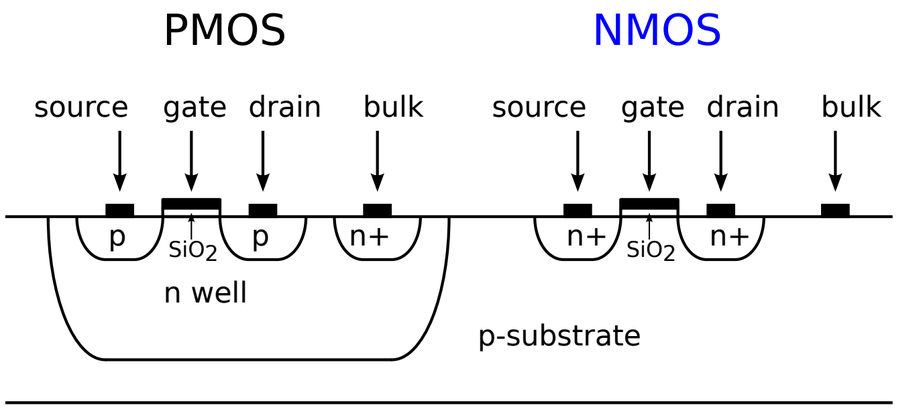

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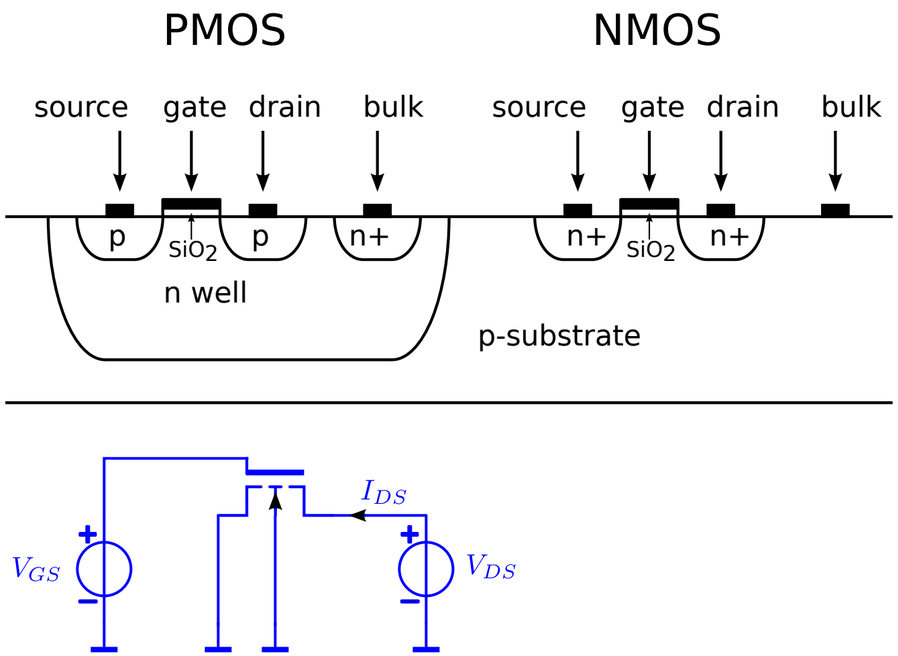

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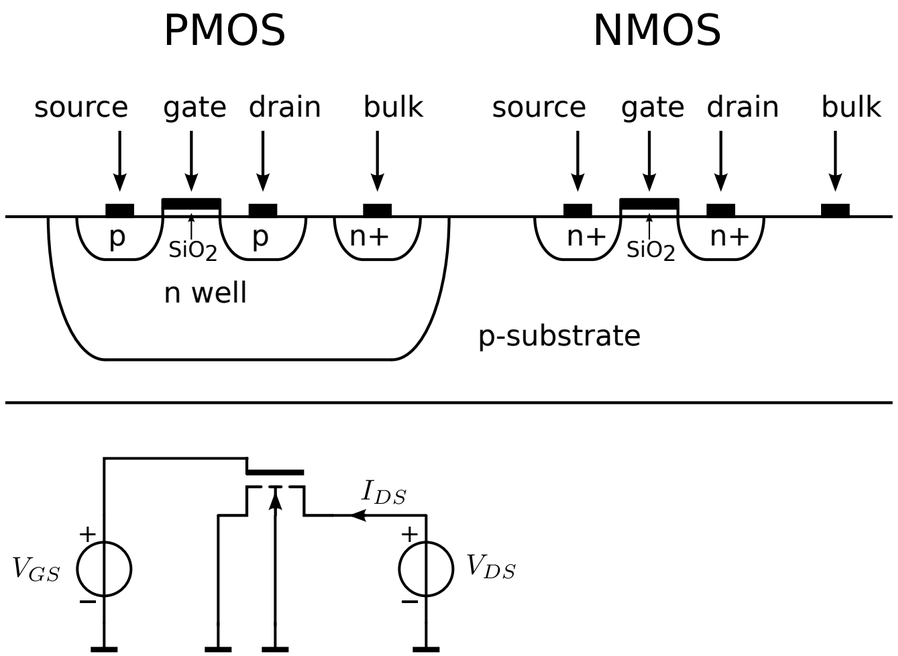
MOS operation

$$V_{GS} = 0,\ V_{DS} > 0$$



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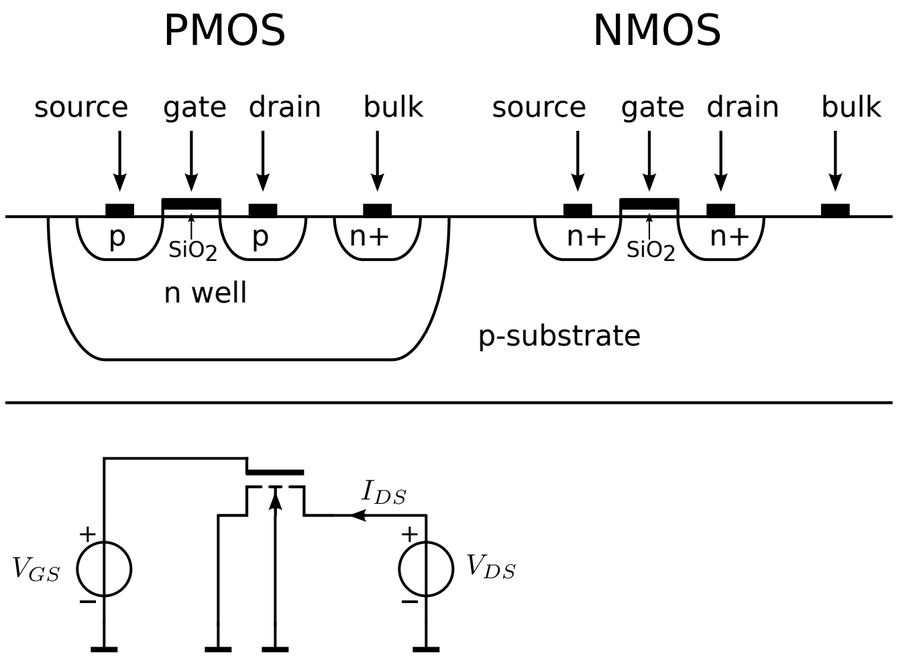

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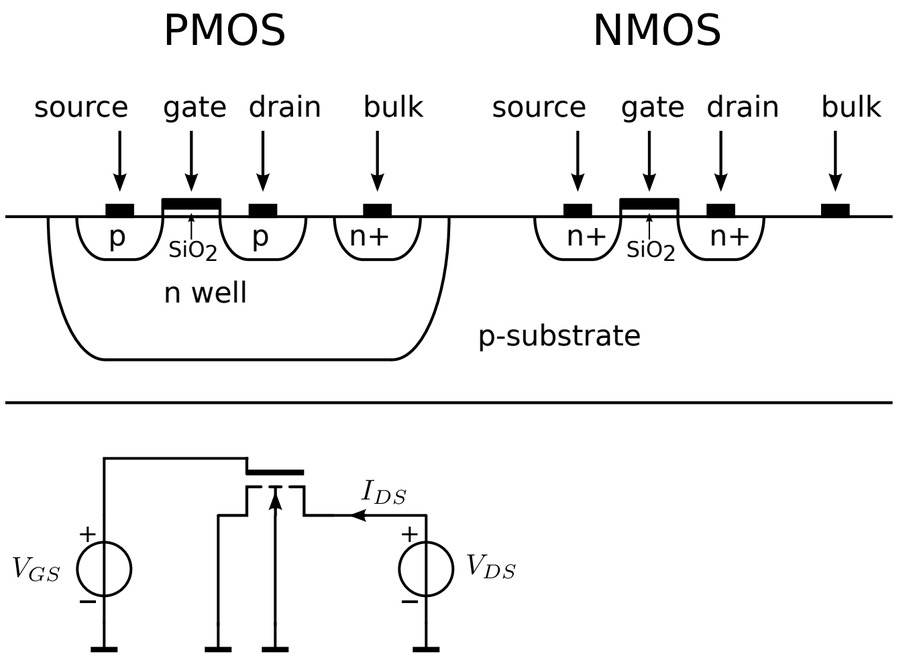

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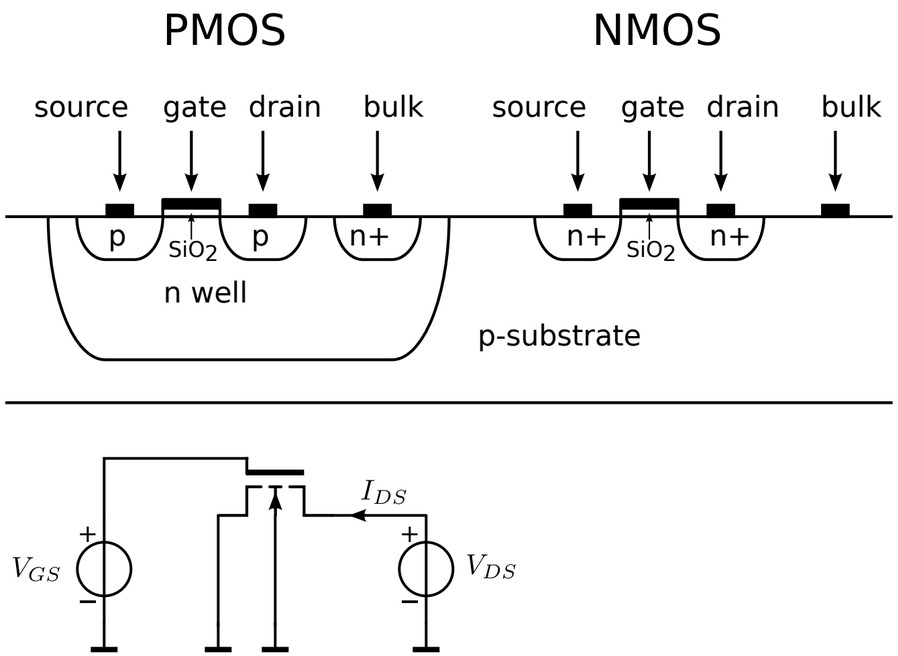

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Surface potential at oxide-Si interface rises

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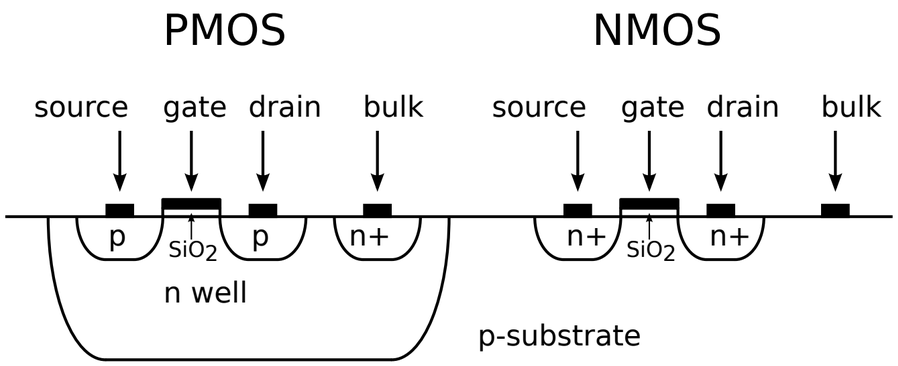

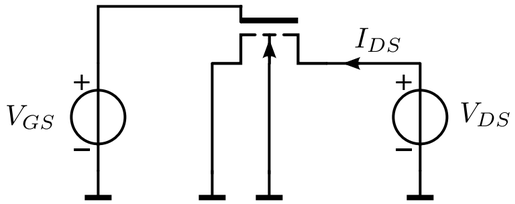

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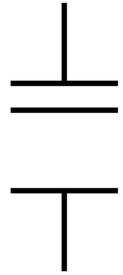
capacitive coupling



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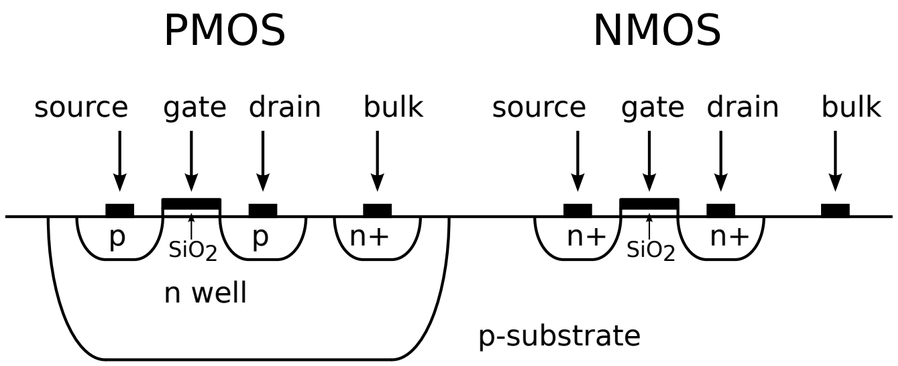

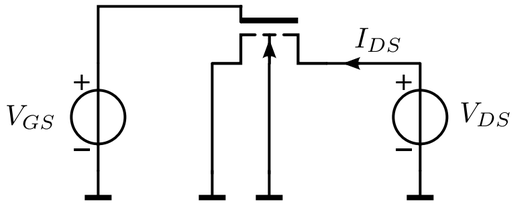

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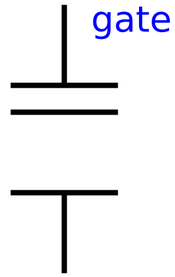

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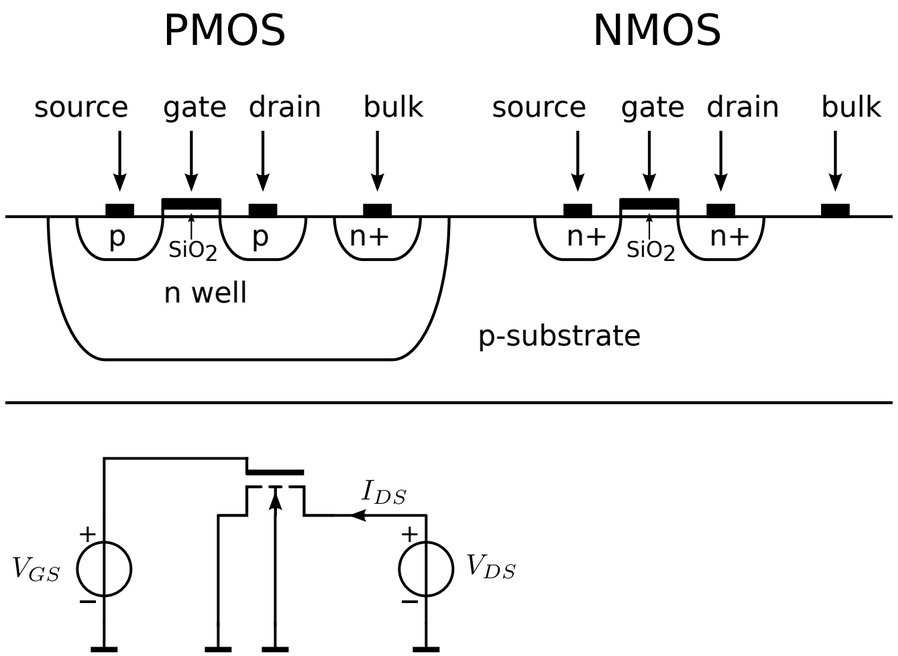

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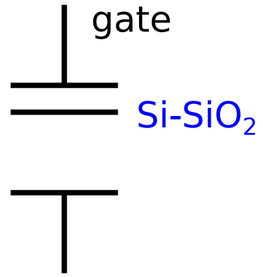

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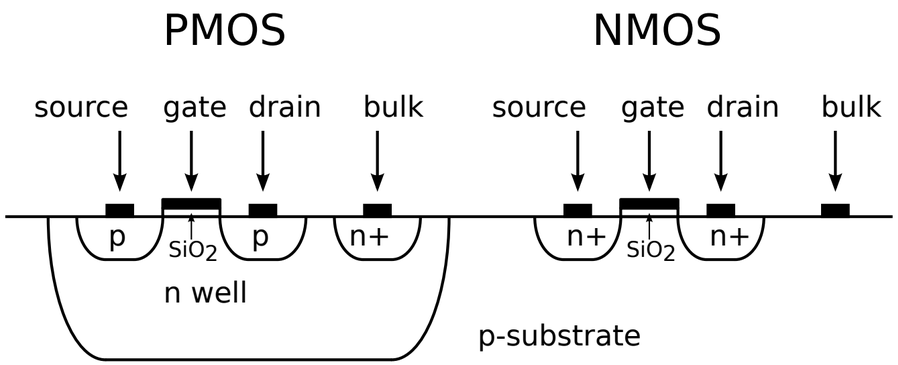

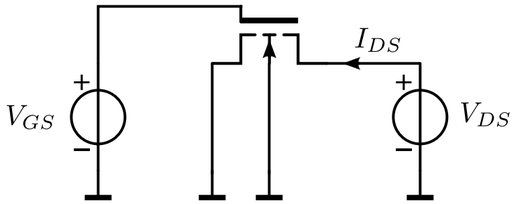

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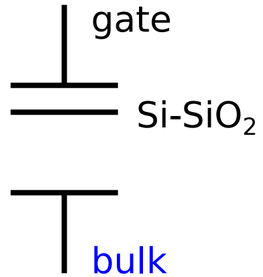
Source injects electrons in p region

capacitive coupling



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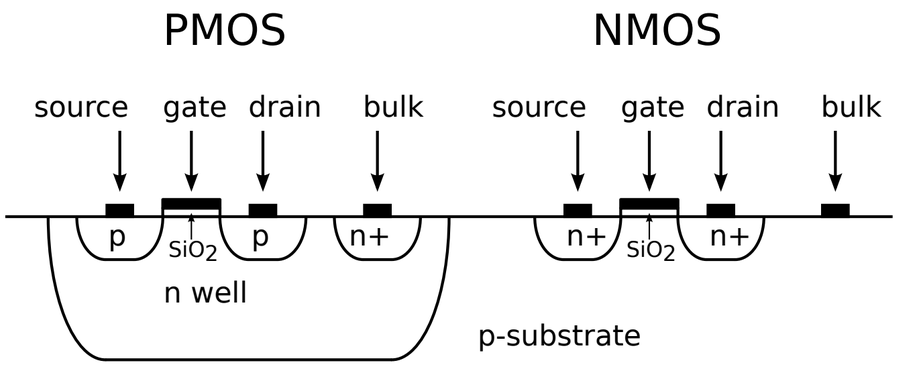

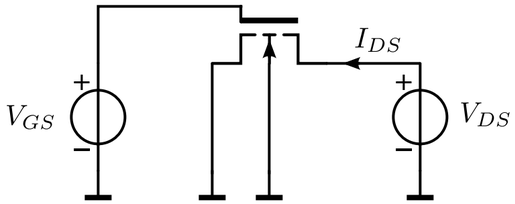

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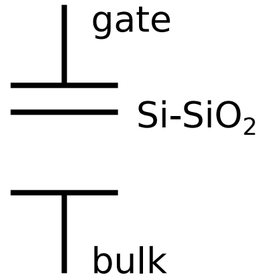

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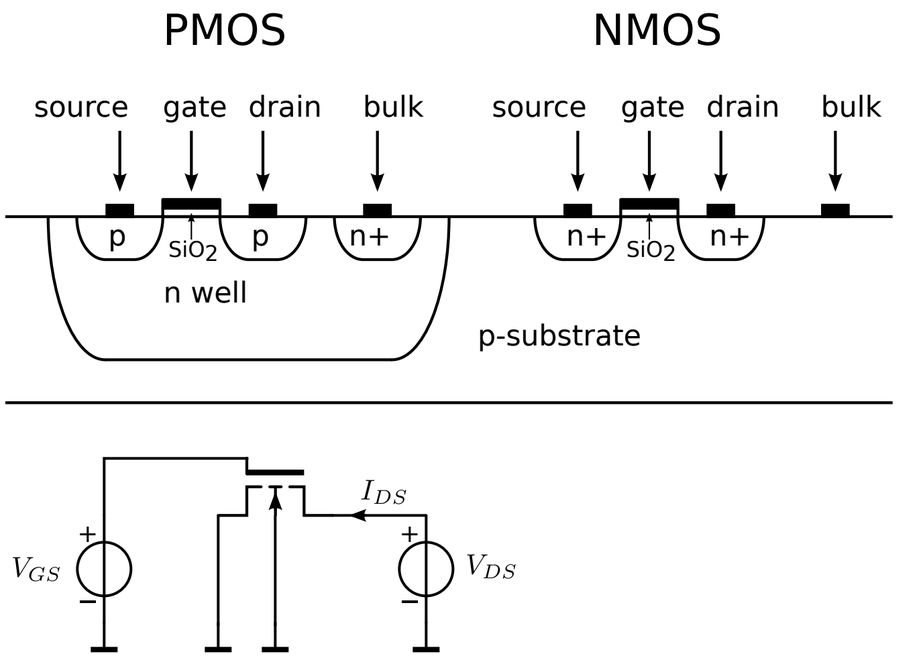

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Drain current increases exponentially with the gate-source voltage

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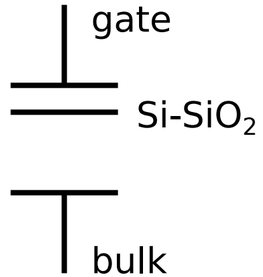

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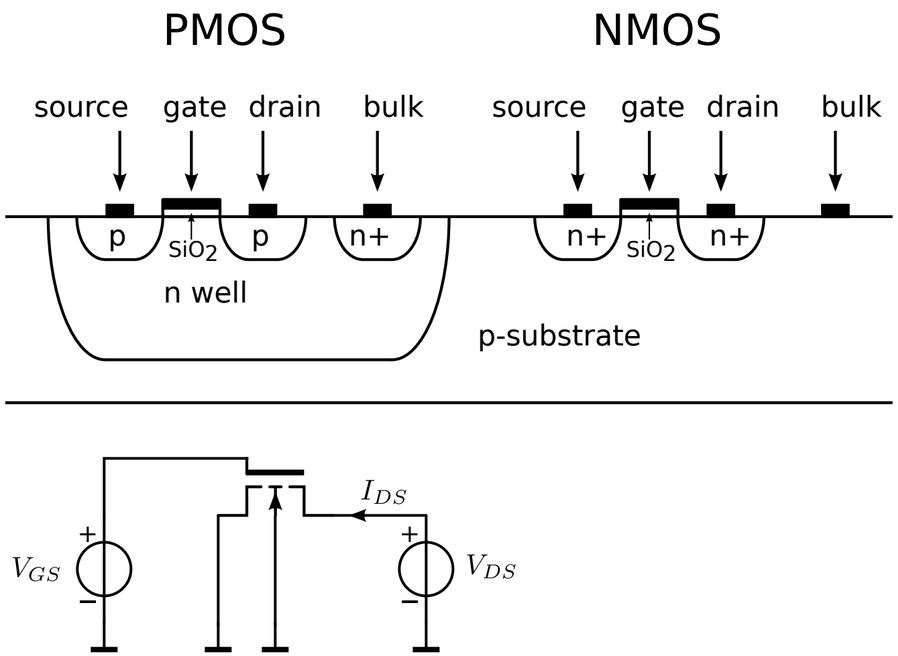

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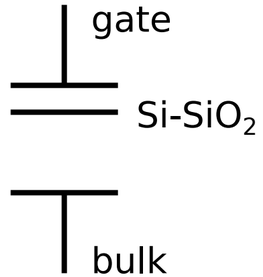

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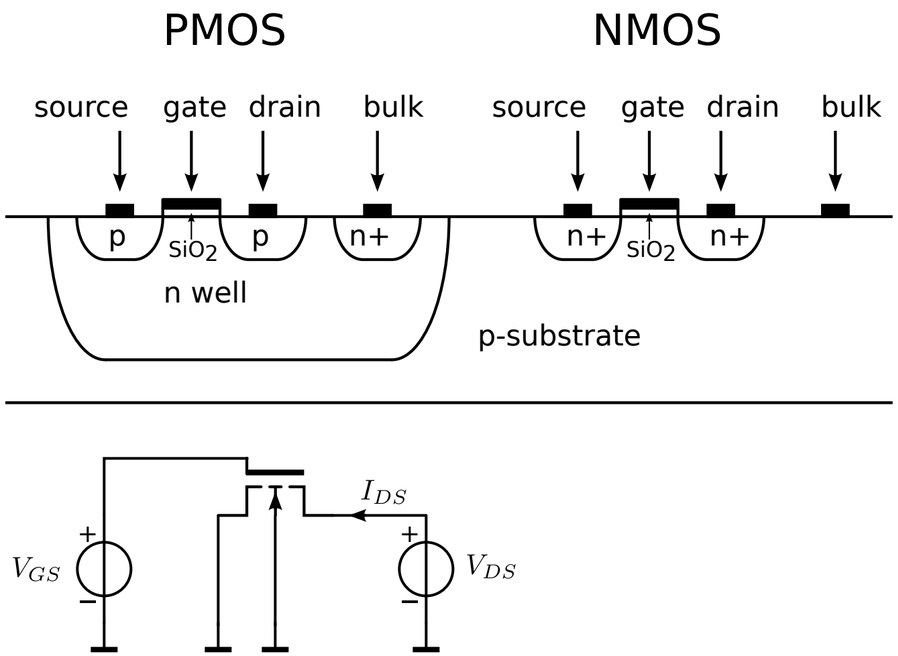

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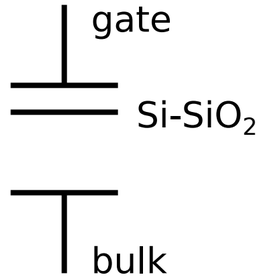

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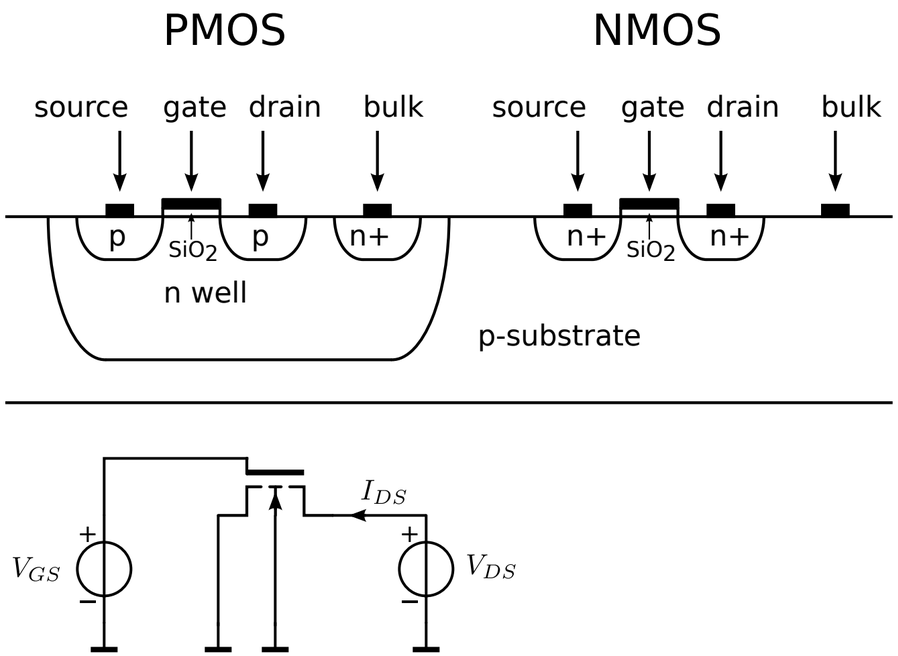

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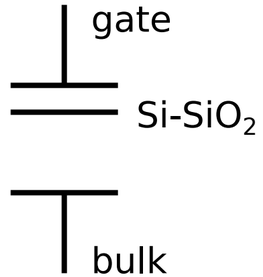

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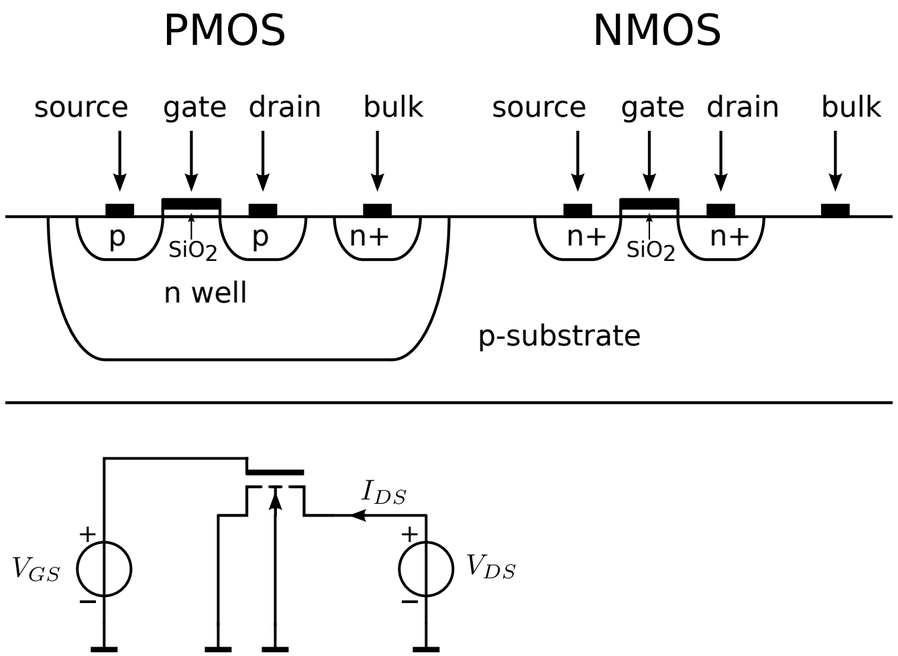

Drain-source voltage dependency

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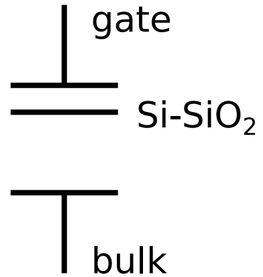

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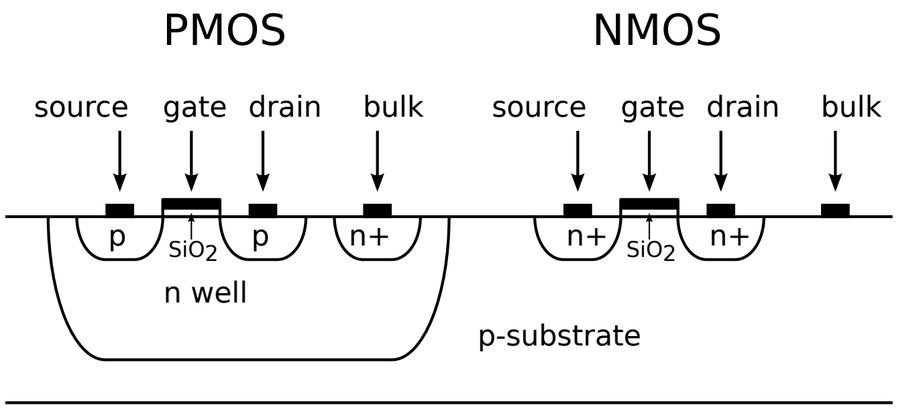

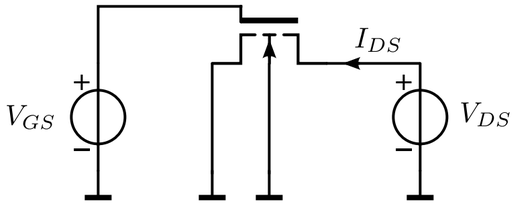

Drain-source voltage dependency

Channel length modulation (CLM)

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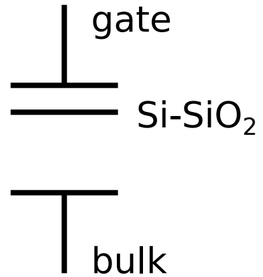

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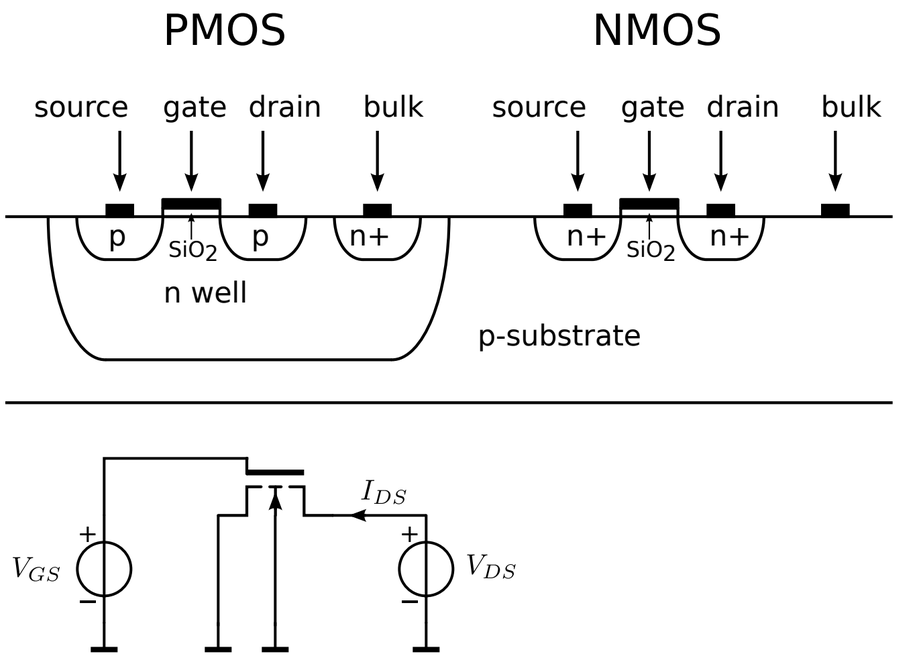

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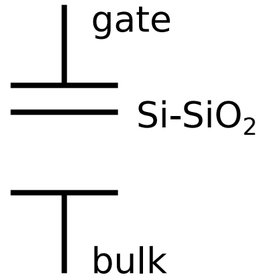

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Drain-source voltage dependency

Channel length modulation (CLM)

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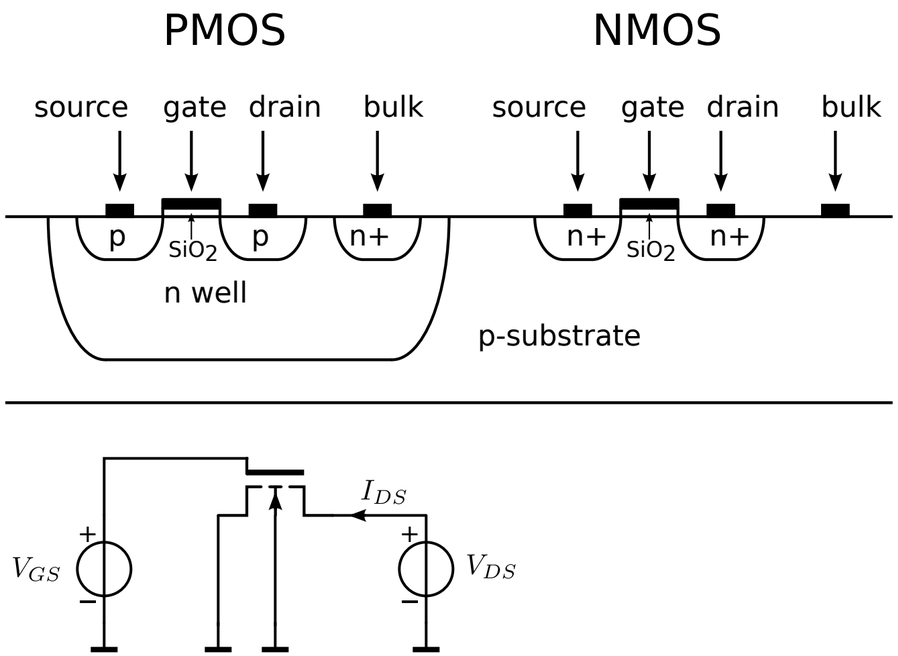

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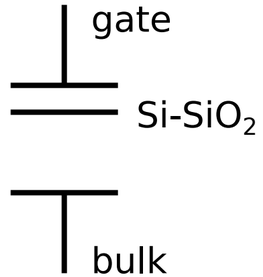

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Drain-source voltage dependency

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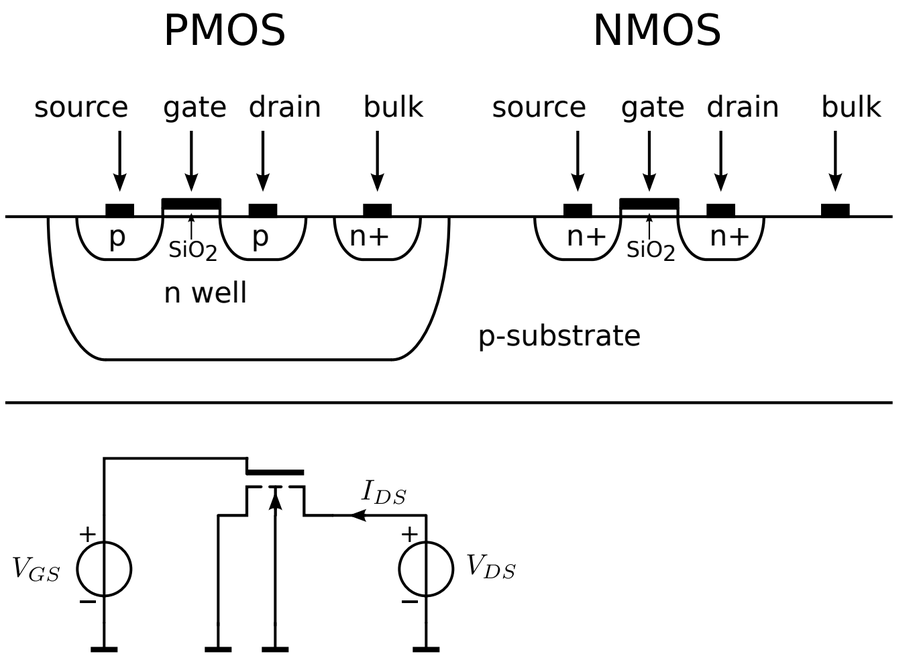
Breakdown

MOS operation



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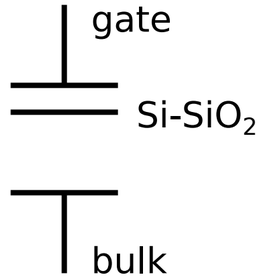

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Breakdown

Short channel effects

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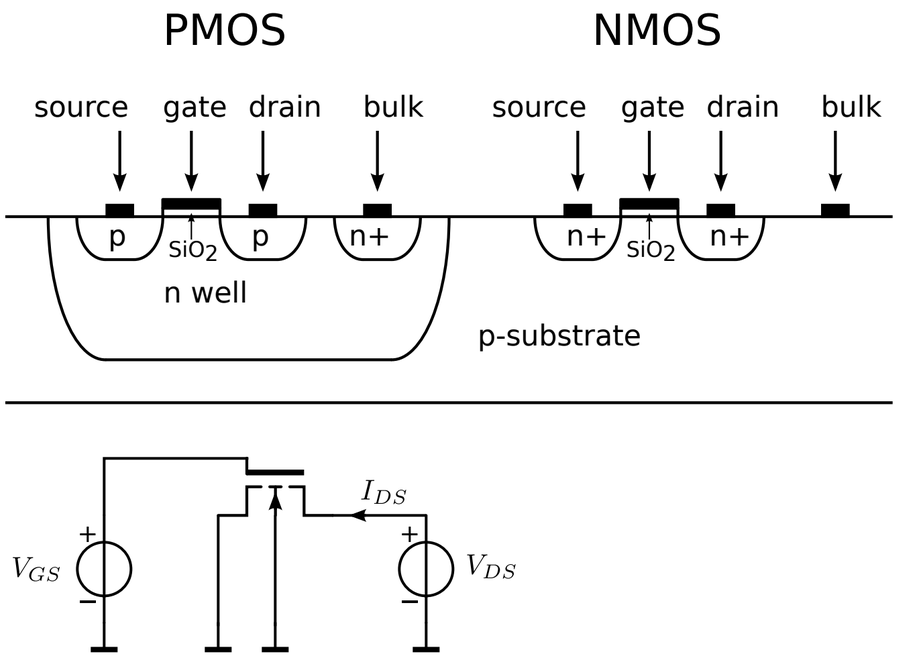

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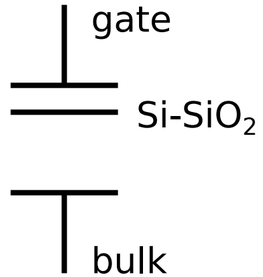

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Drain-source voltage dependency

Channel length modulation (CLM)

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Breakdown

Short channel effects

Vertical field mobility reduction (VFMR)

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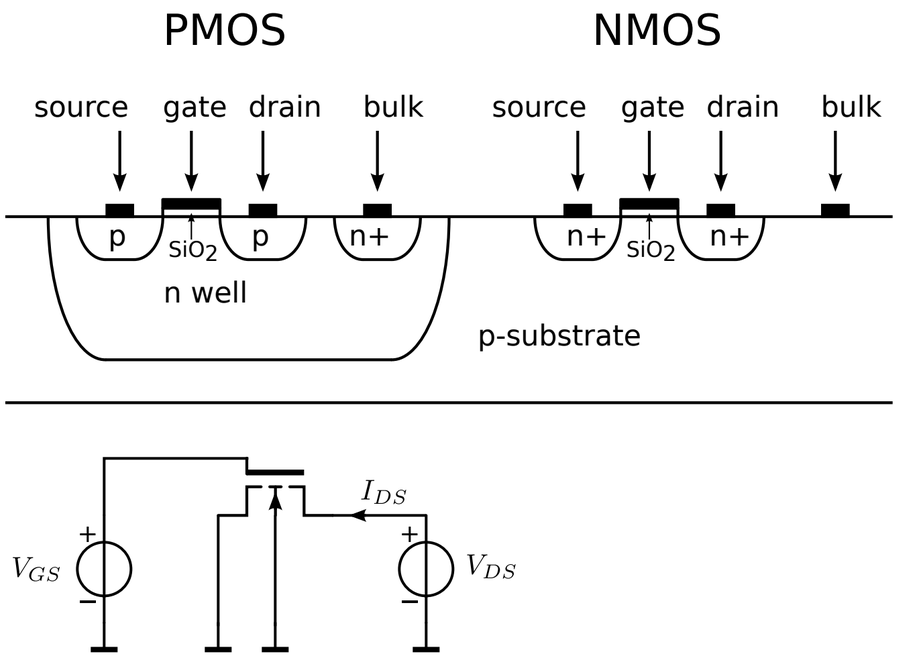

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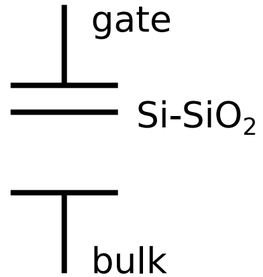

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Velocity saturation (VS)

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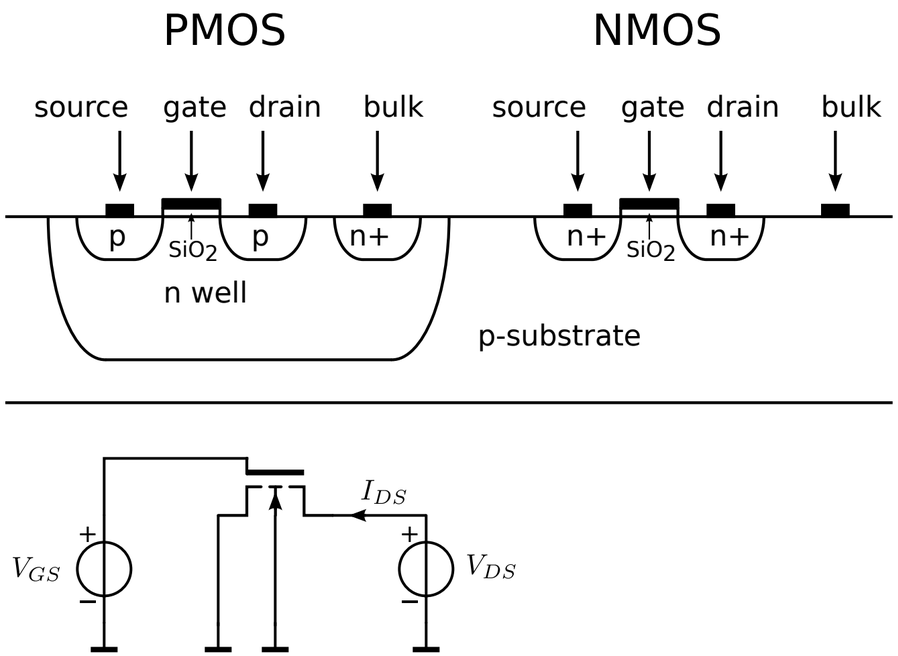
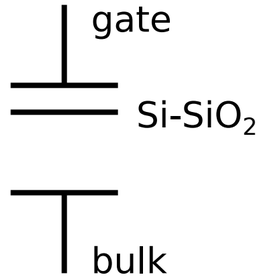
MOS operation



capacitive coupling



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$V_{GS} > 0, V_{DS} >> 0$

Surface potential at oxide-Si interface rises
Source injects electrons in p region
Weak inversion

Drain current increases exponentially with the gate-source voltage

$V_{GS} > V_{th}, V_{DS} > V_{GS} - V_{th}$

An n-channel is established between source and drain

Drain current increases quadratically with the gate-source voltage

Drain-source voltage dependency

Channel length modulation (CLM)

Drain current increases with drain-source voltage

Breakdown

Short channel effects

Vertical field mobility reduction (VFMR)

Velocity saturation (VS)

Drain current increases not longer quadratically with the gate-source voltage

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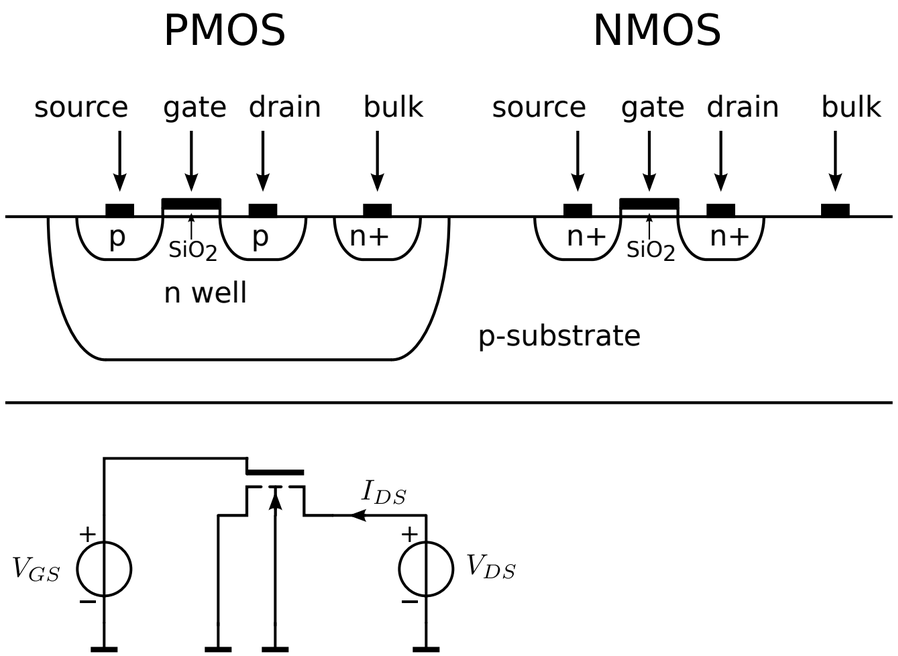

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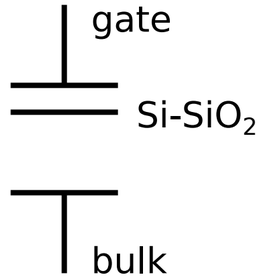

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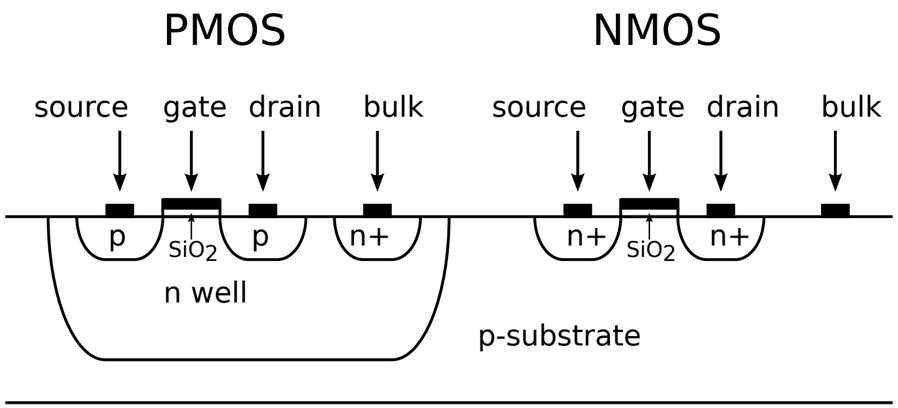
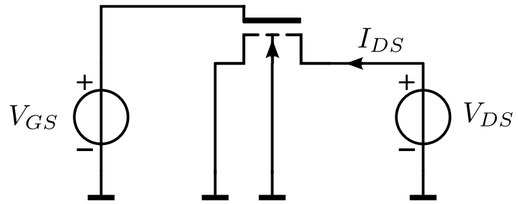
MOS operation





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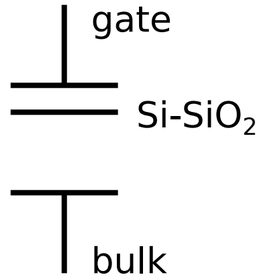

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- Breakdown

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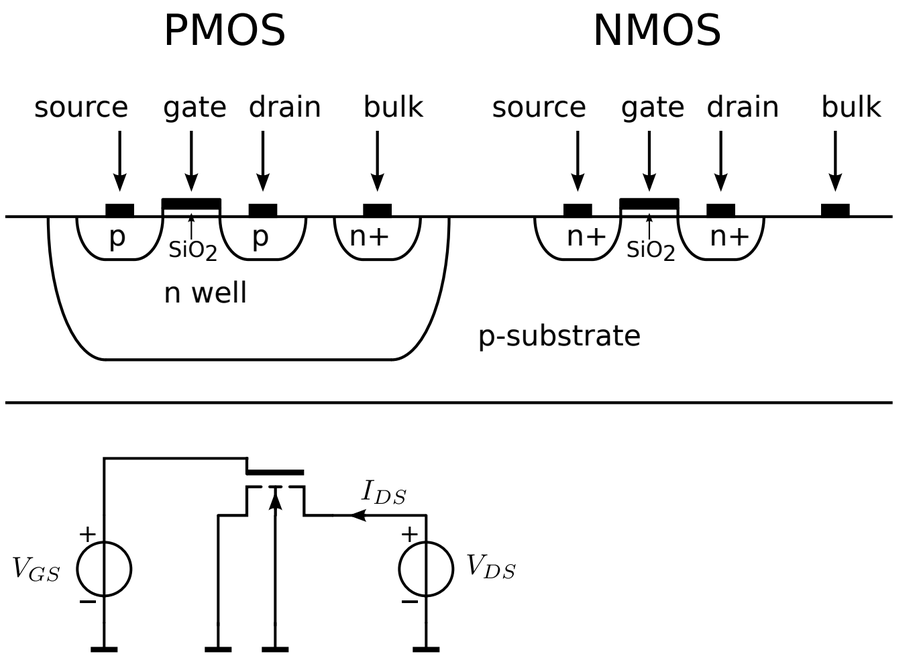
MOS operation



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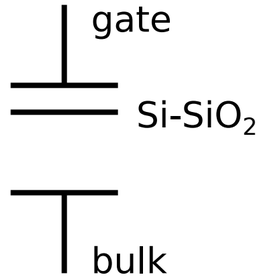

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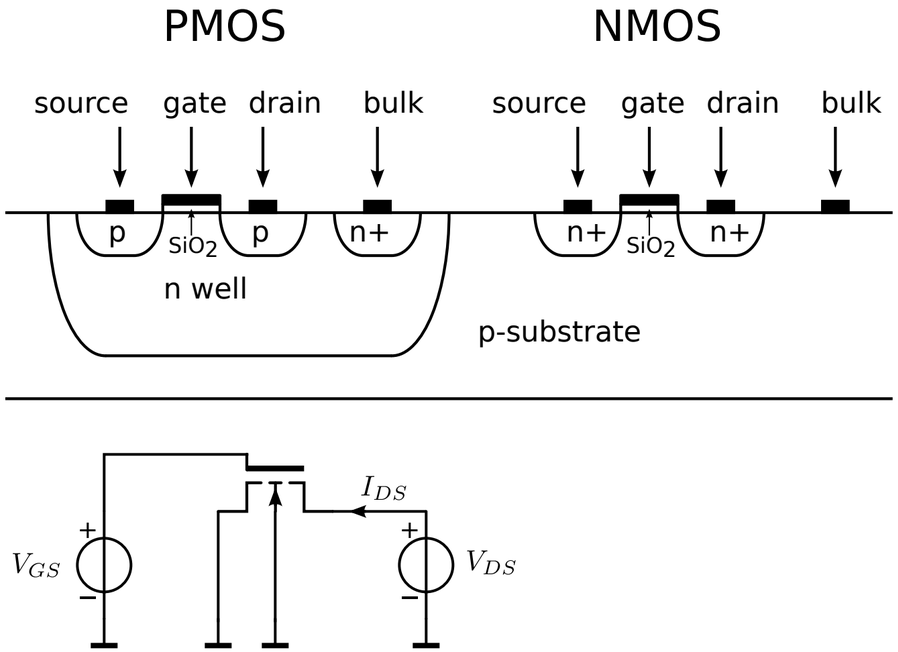

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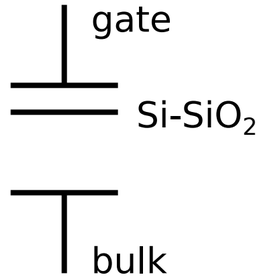

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MOS design

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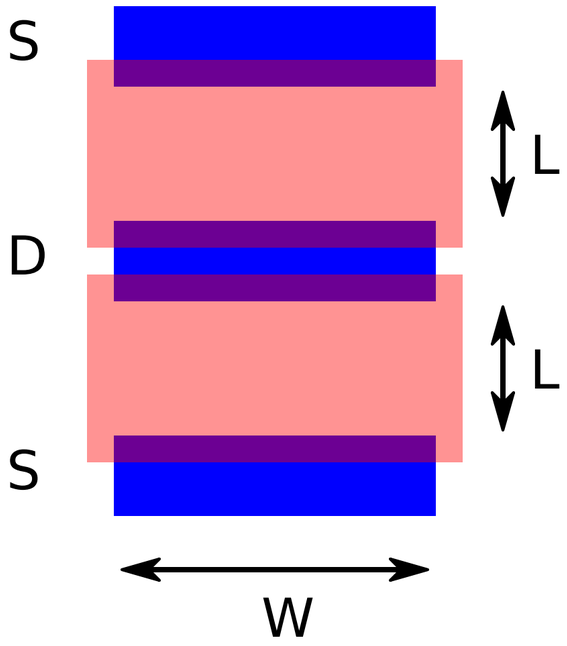

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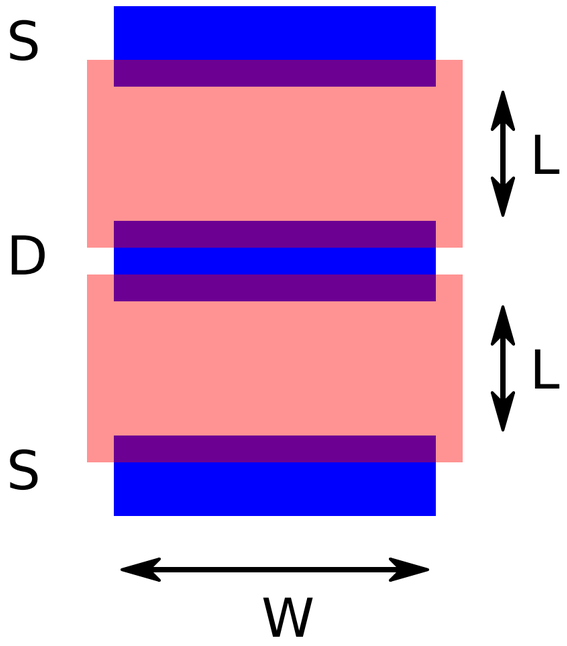
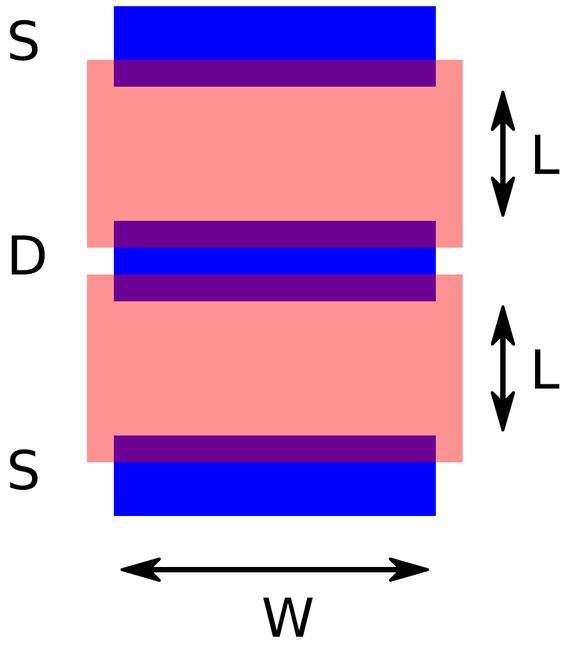


Design question

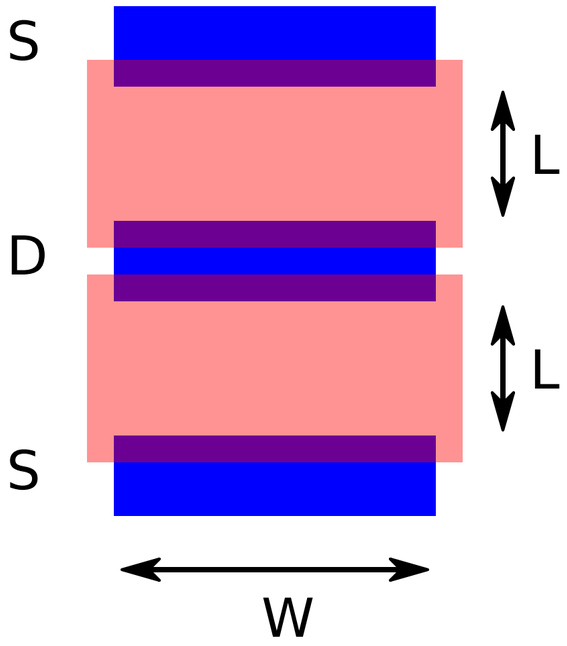
MOS design



Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

MOS design



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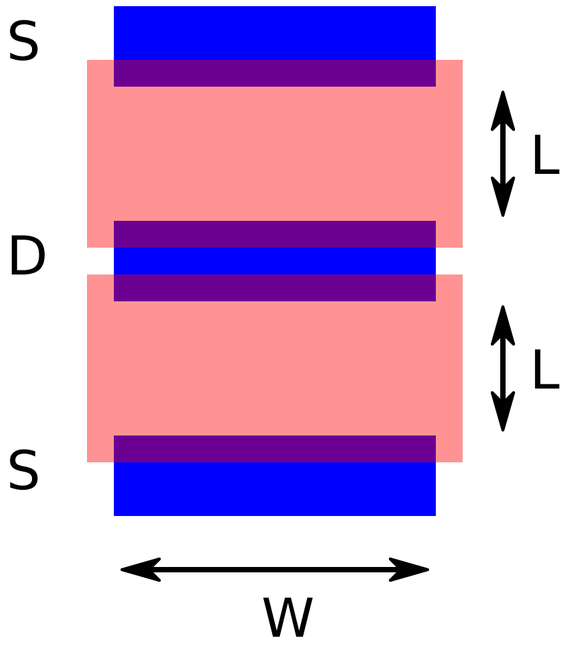
Design parameters available to the designer

MOS design



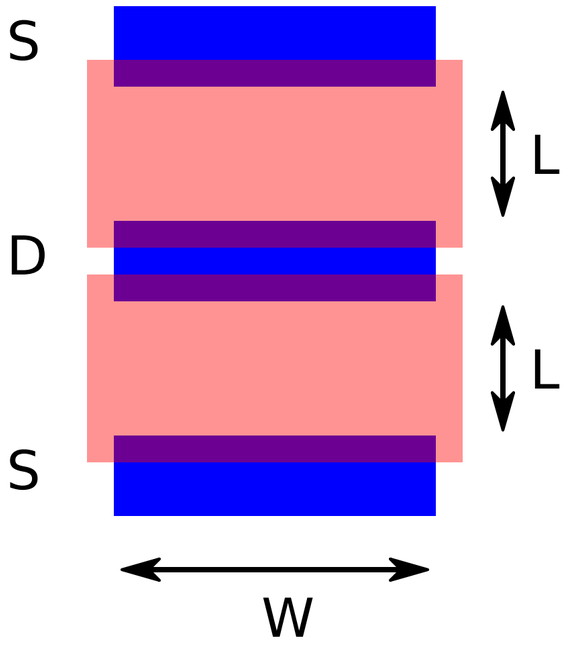
Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

Channel width

MOS design



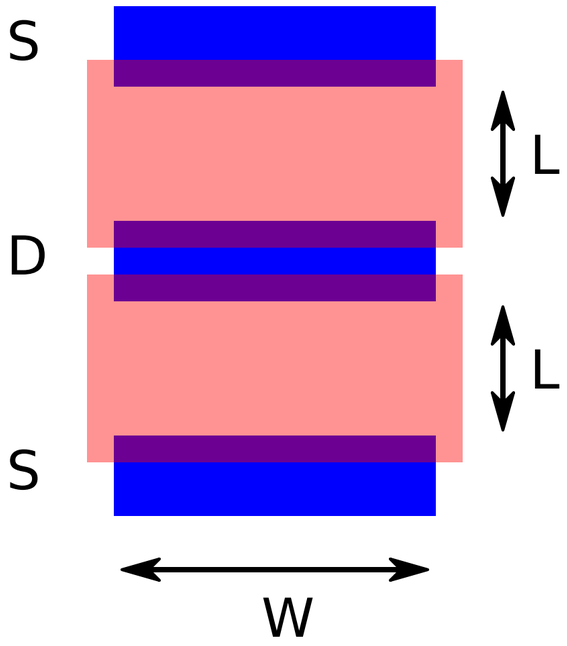
Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

Channel width
Channel length

MOS design



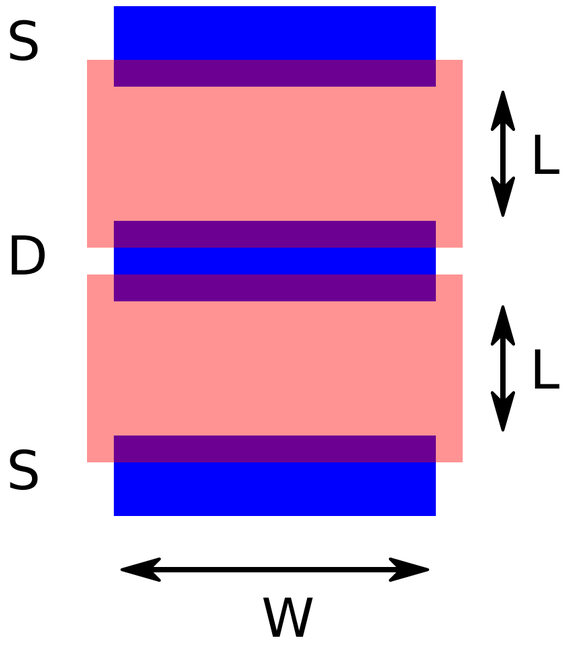
Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

Channel width
Channel length
Number of sections

MOS design



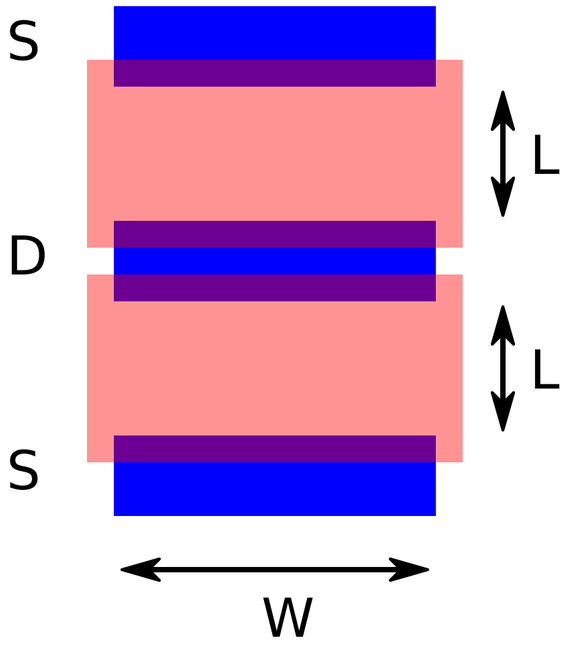
Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Design parameters available to the designer

Channel width
Channel length
Number of sections
Drain current

MOS design



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Design parameters available to the designer

- Channel width
- Channel length
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- Drain current
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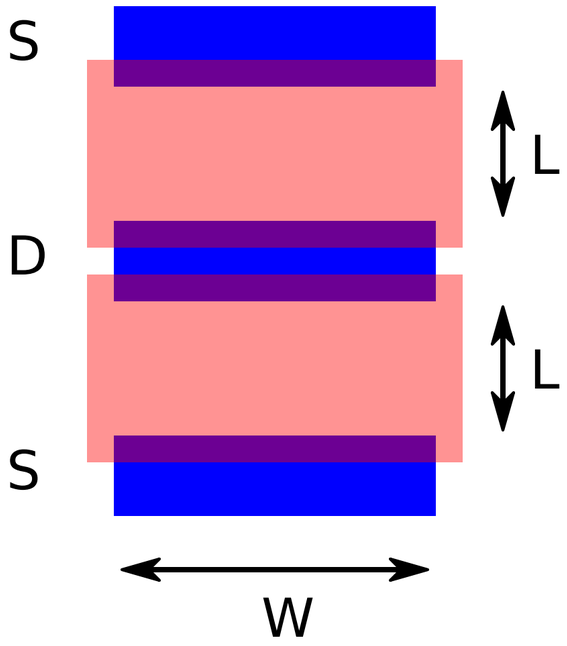
MOS design



Design question

In which way do the performance parameters of a MOS transistor depend on its design parameters

Methods

Design parameters available to the designer

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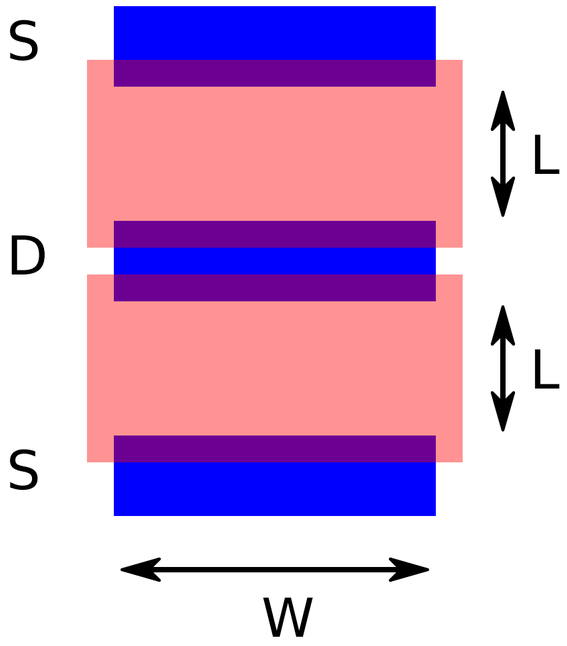
MOS design



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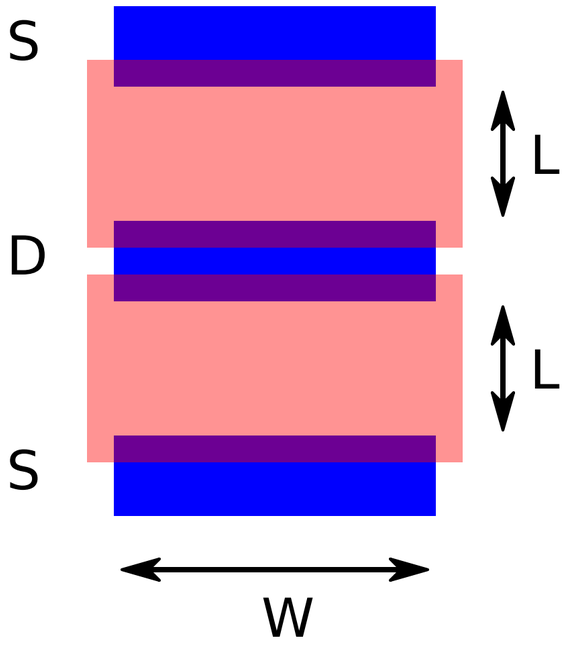
Methods

Use a design manual with graphs and tables and scale devices

MOS design



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Useful, but generally not all situations will be covered

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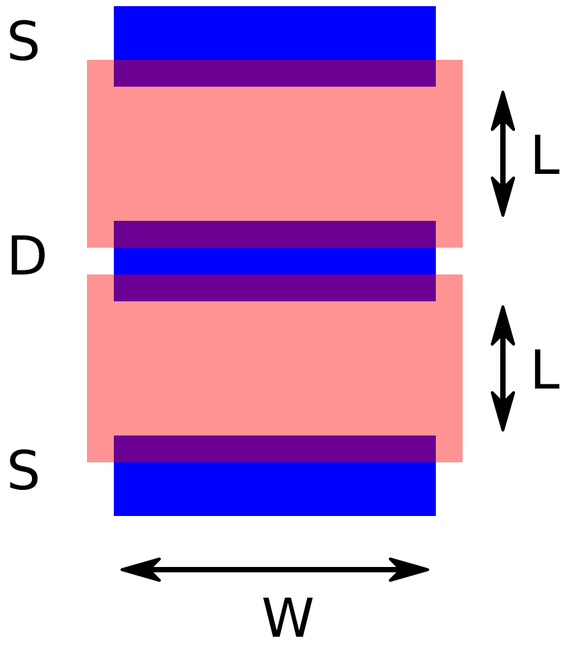
MOS design



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Design a device and study its performance through simulation

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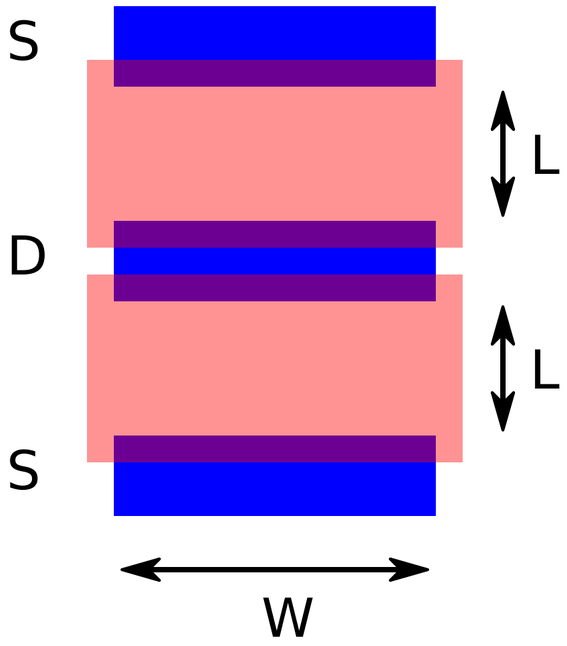

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Useful for finding DC operating conditions and small-signal model parameters

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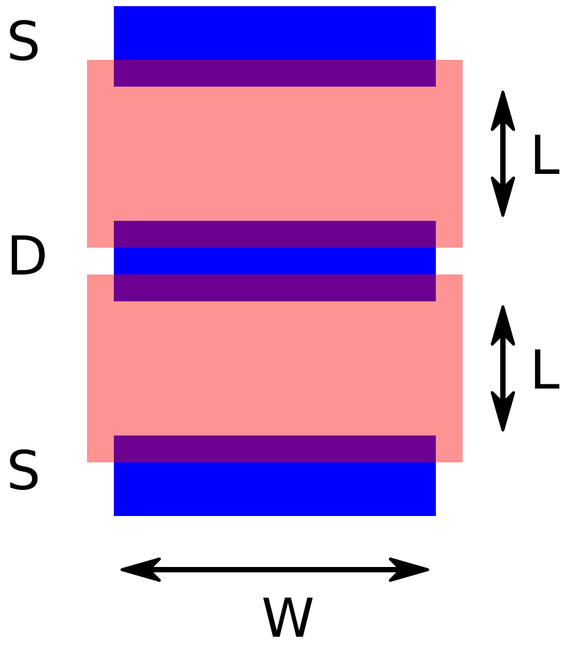

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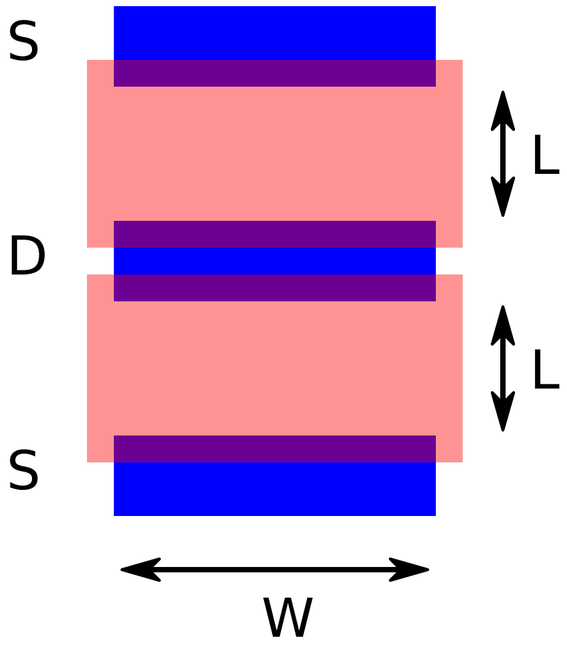

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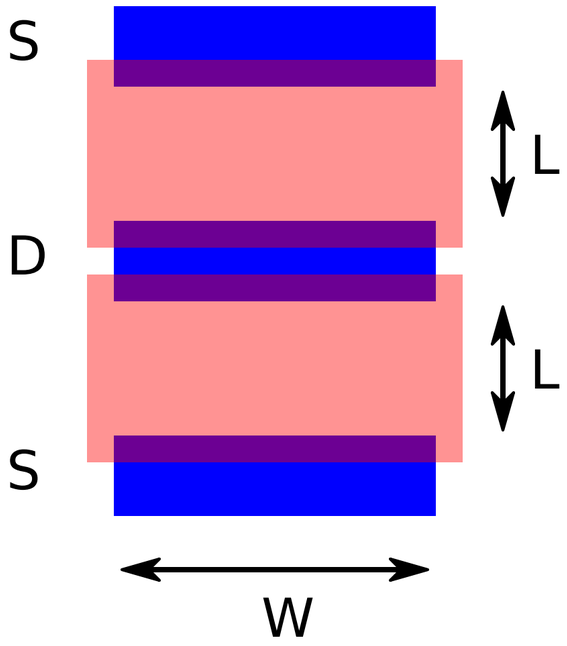

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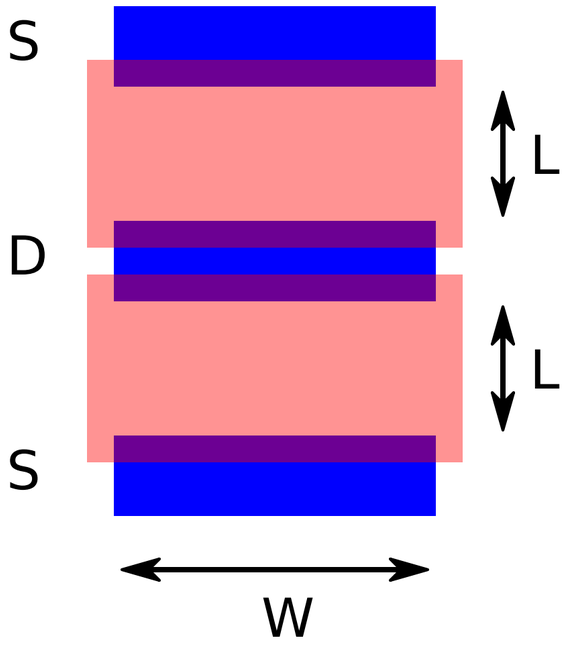

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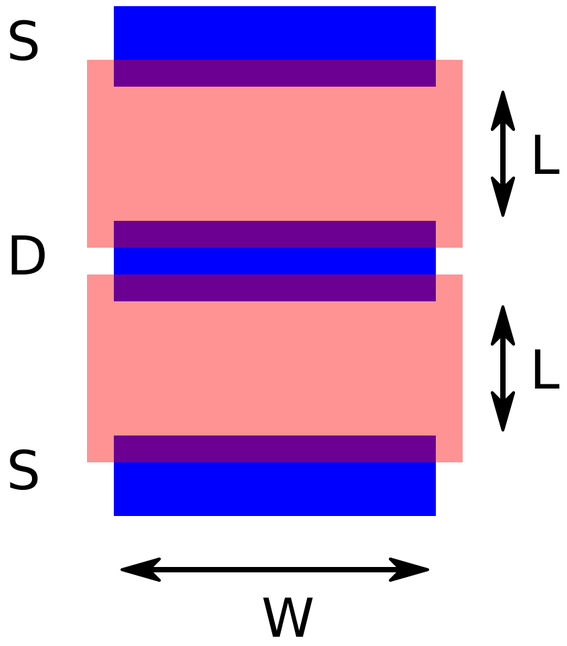

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MOS small-signal model

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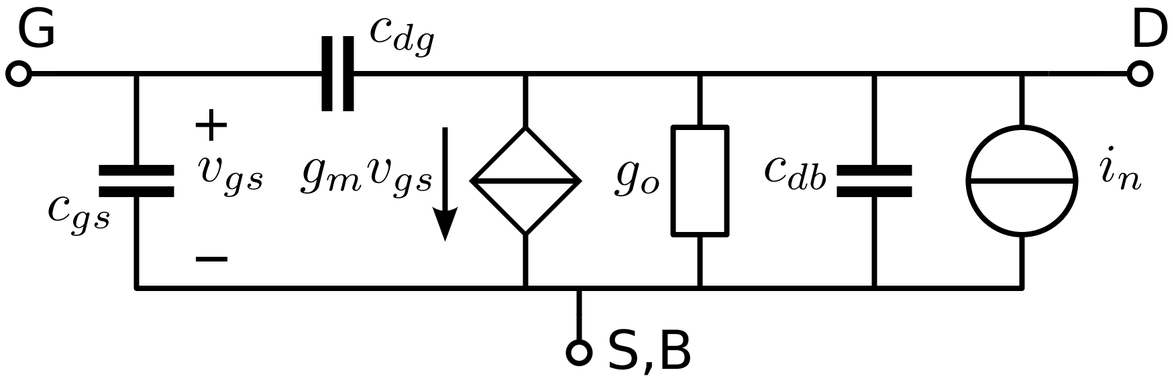

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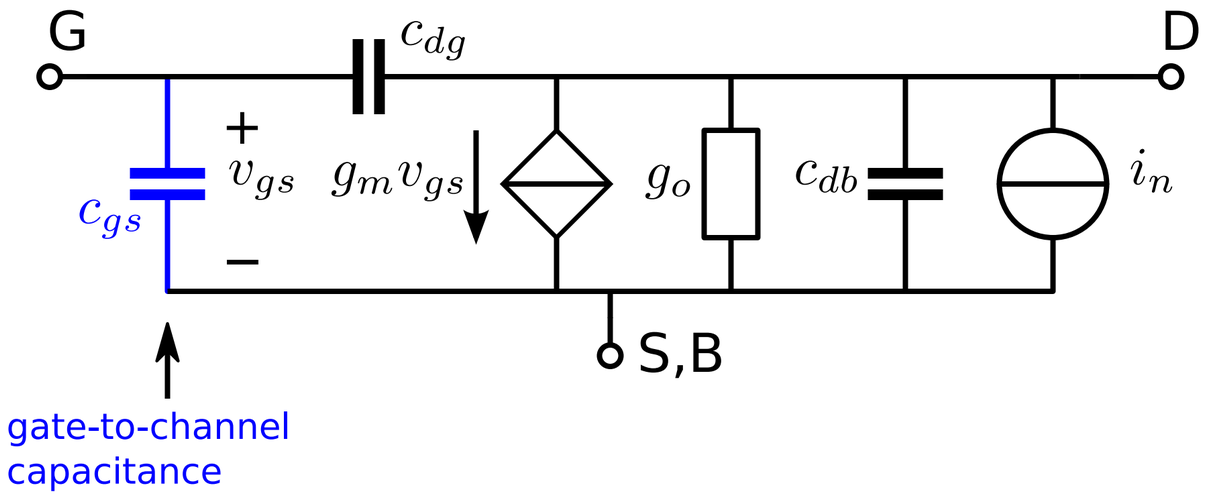

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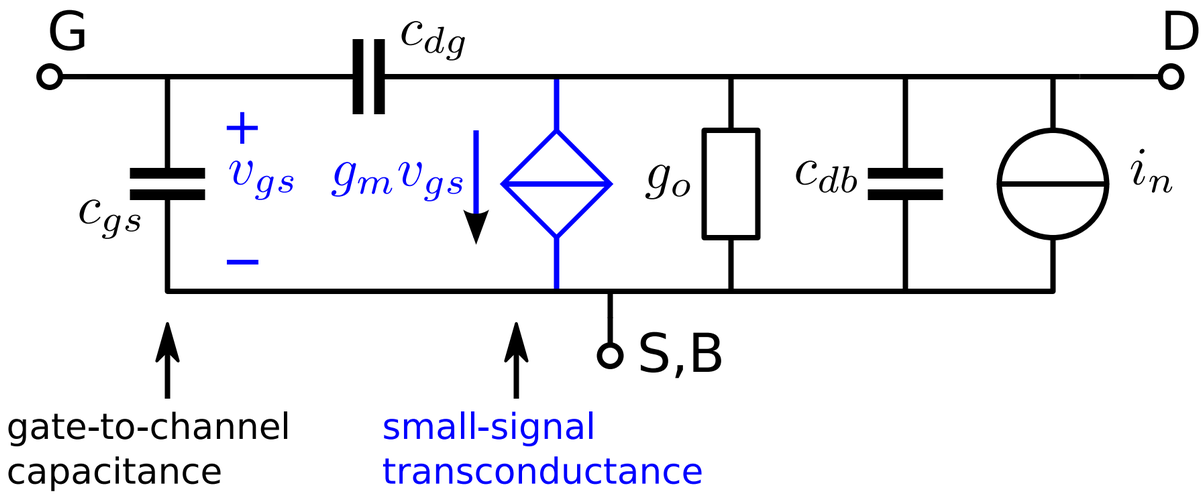

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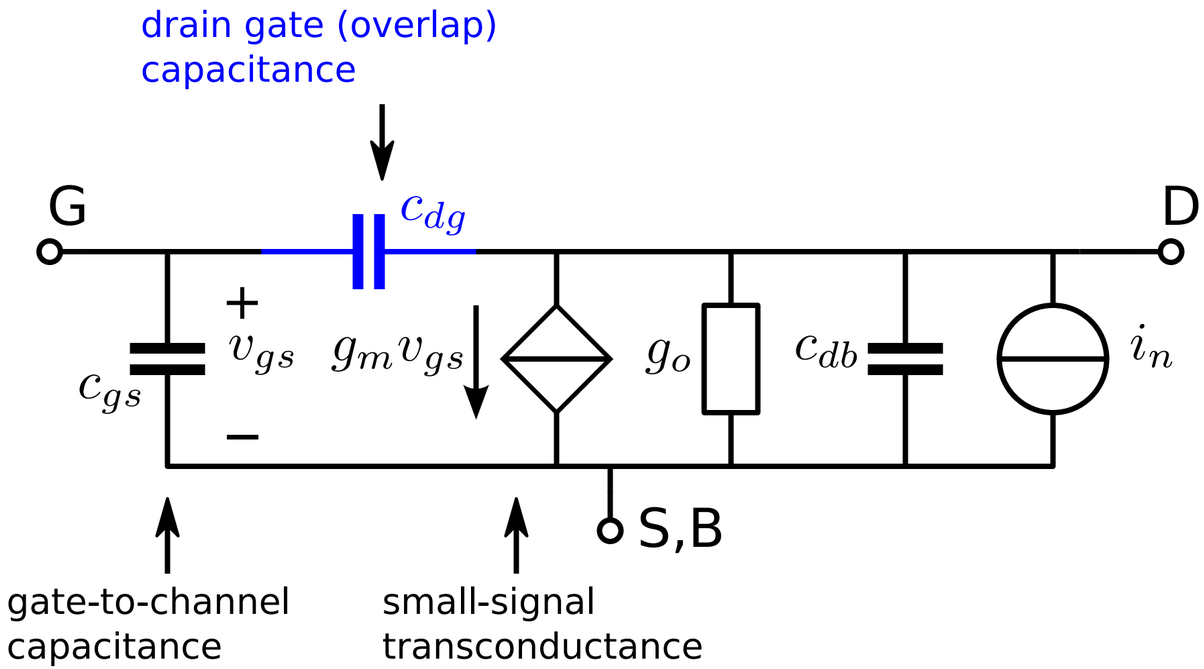

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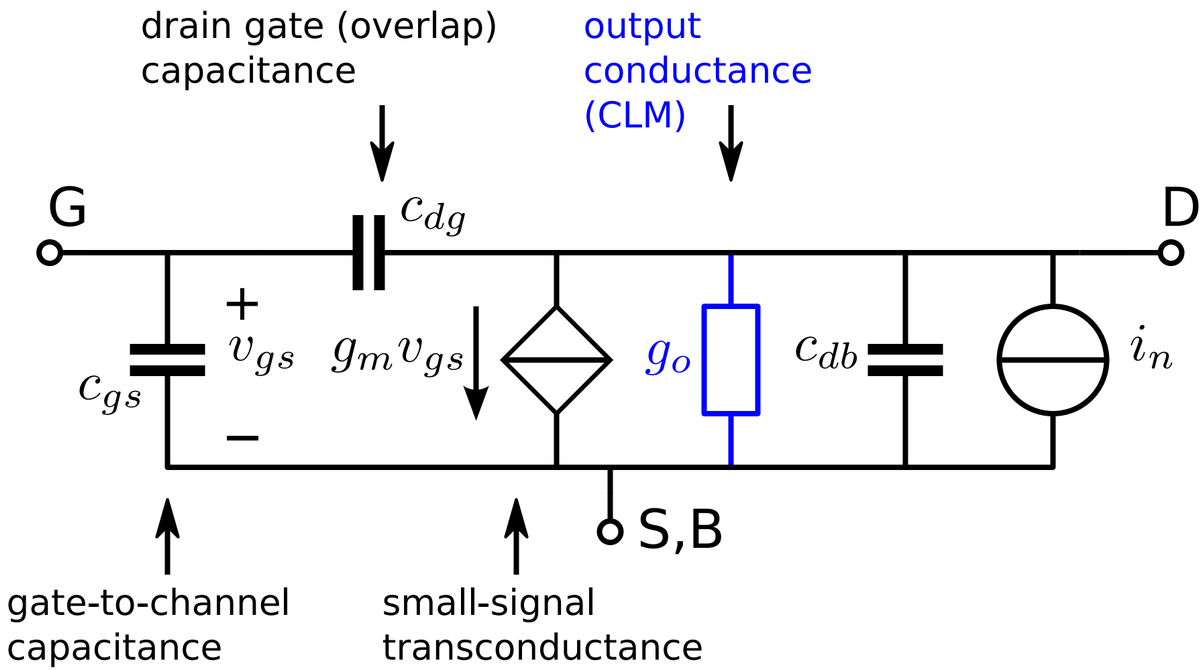

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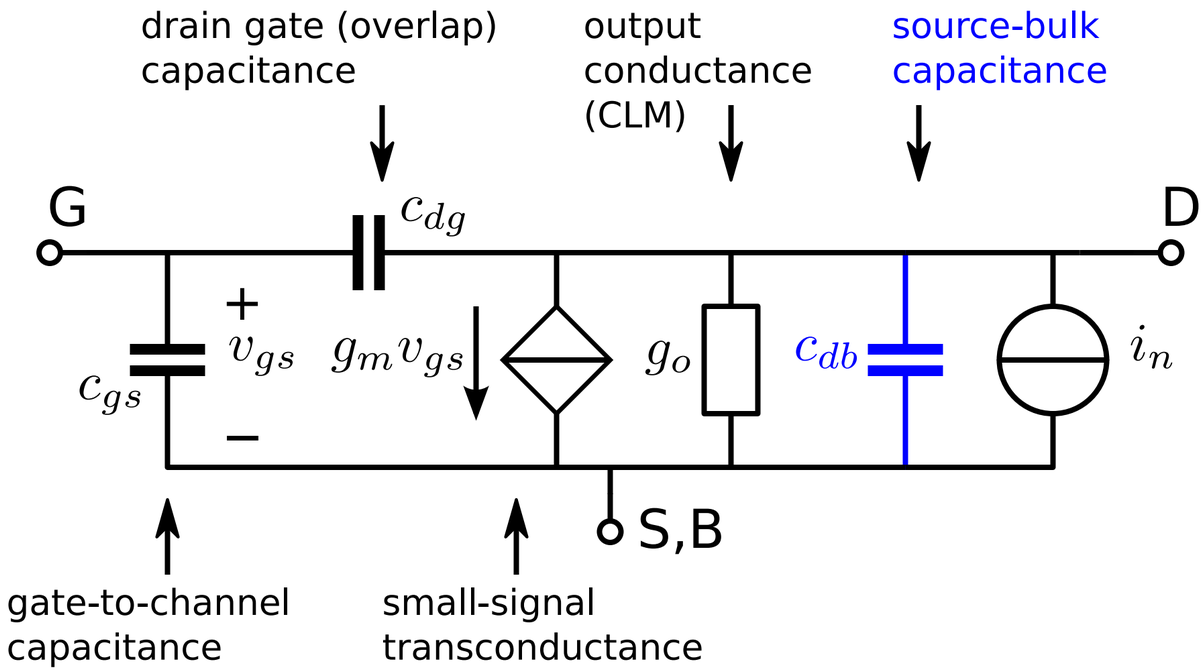

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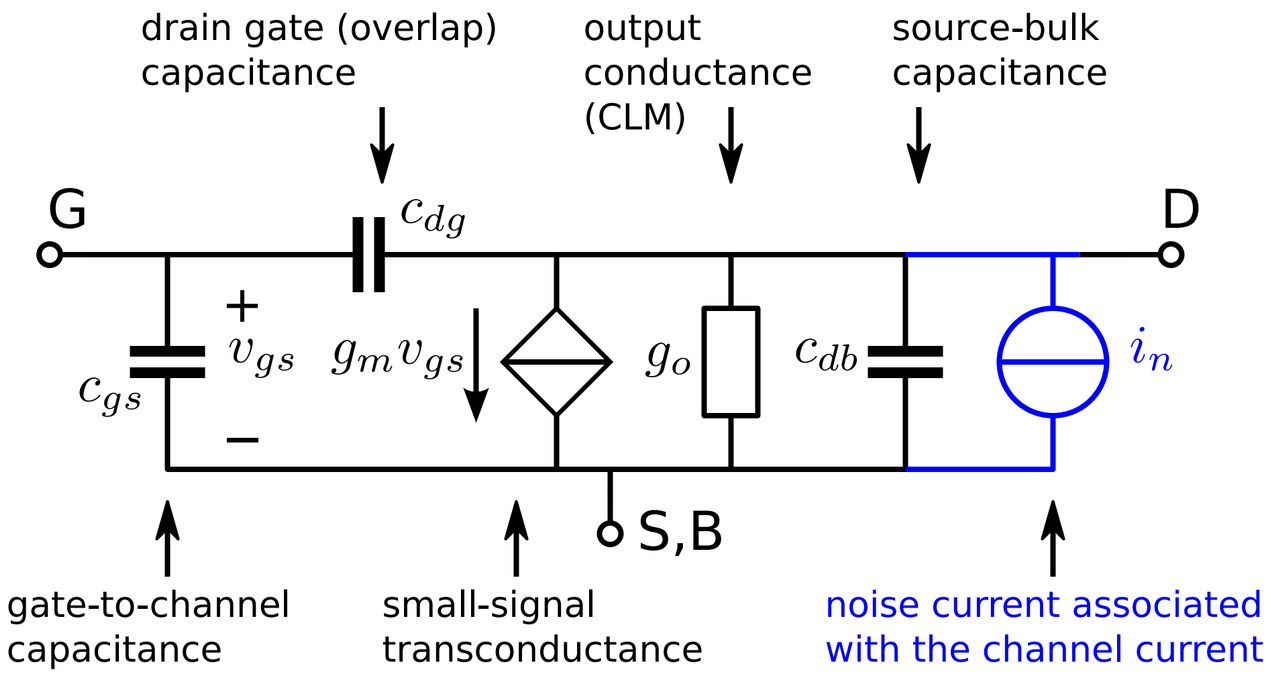

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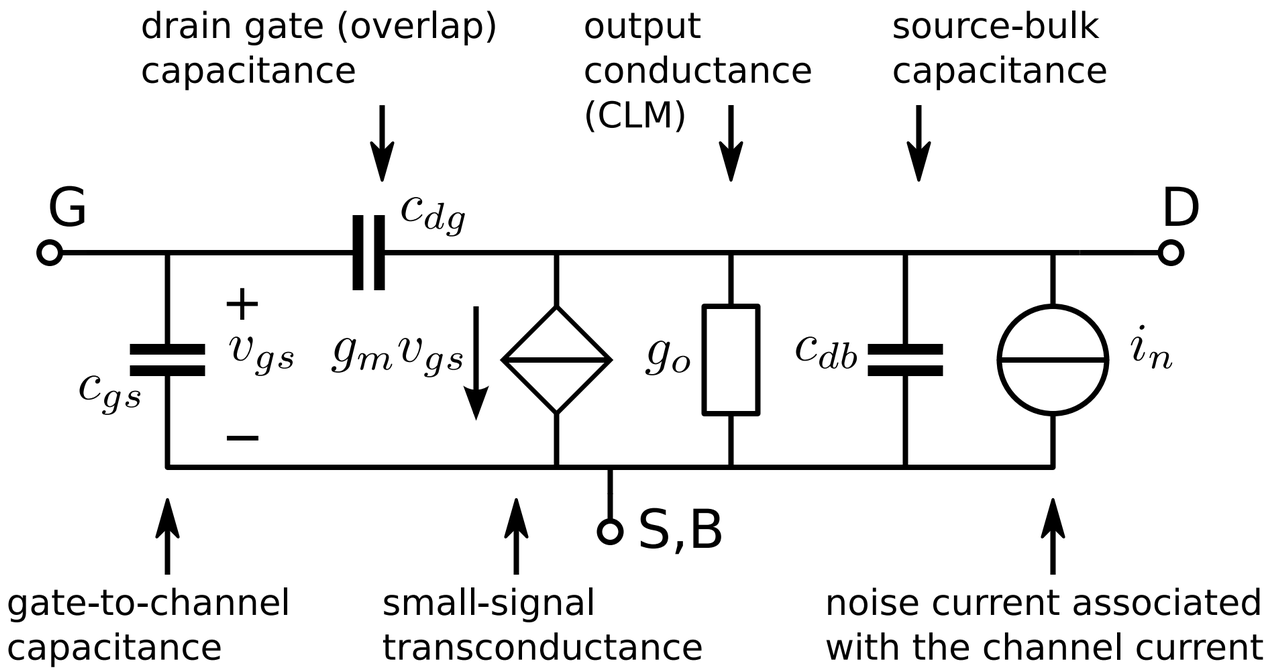
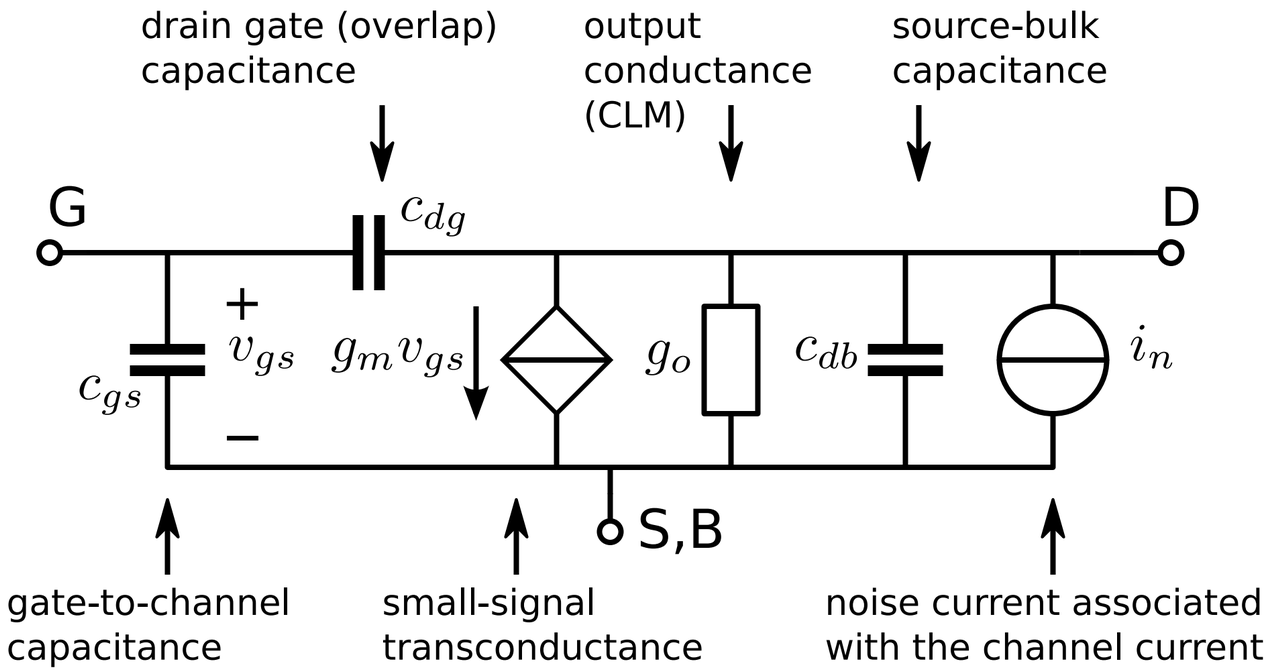


How do these model parameters depend on the device geometry and the operating conditions?

MOS small-signal model



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MOS EKV model

MOS EKV model

1995: C.C. **E**nz, F. **K**rummenacher and E.A. **V**ittoz

MOS EKV model

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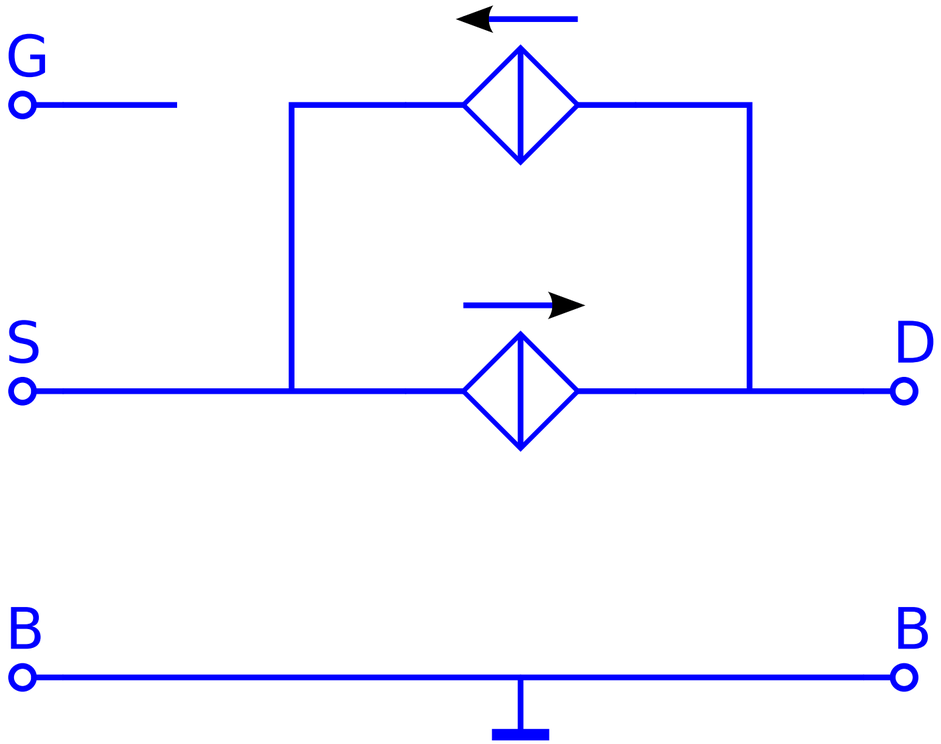

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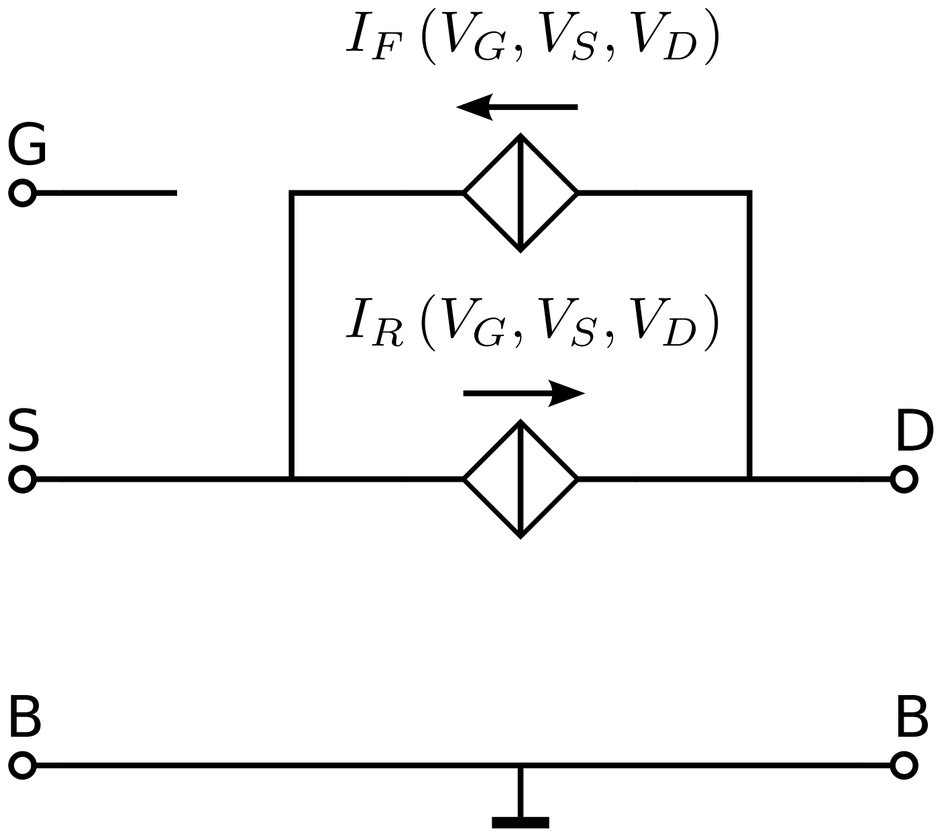

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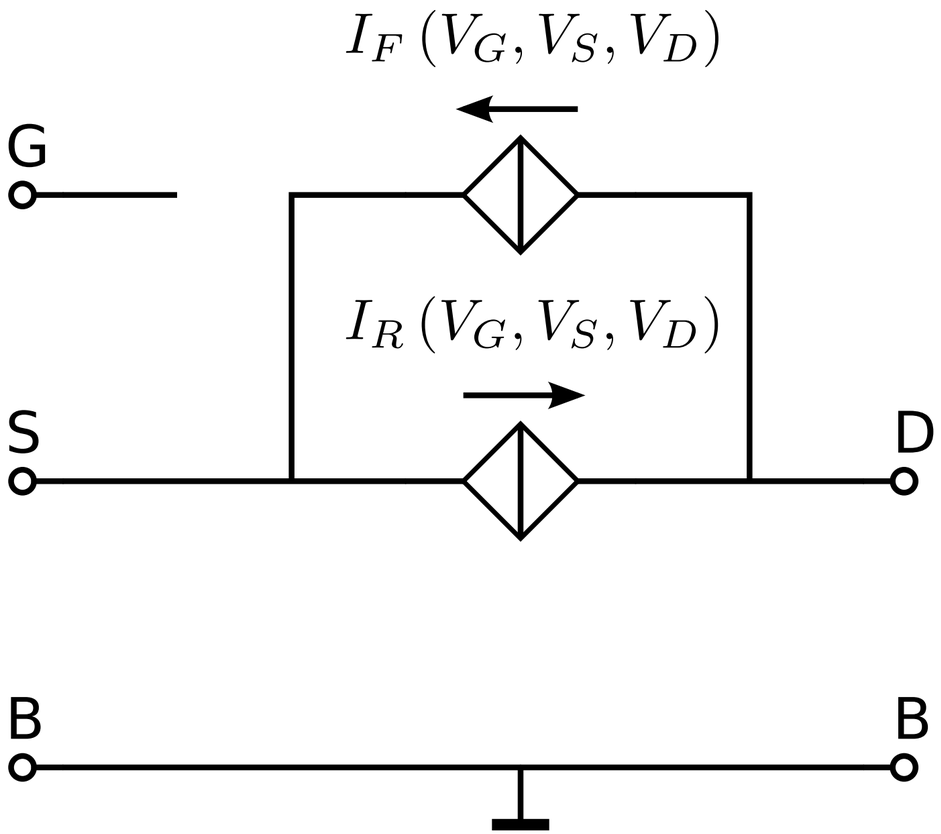

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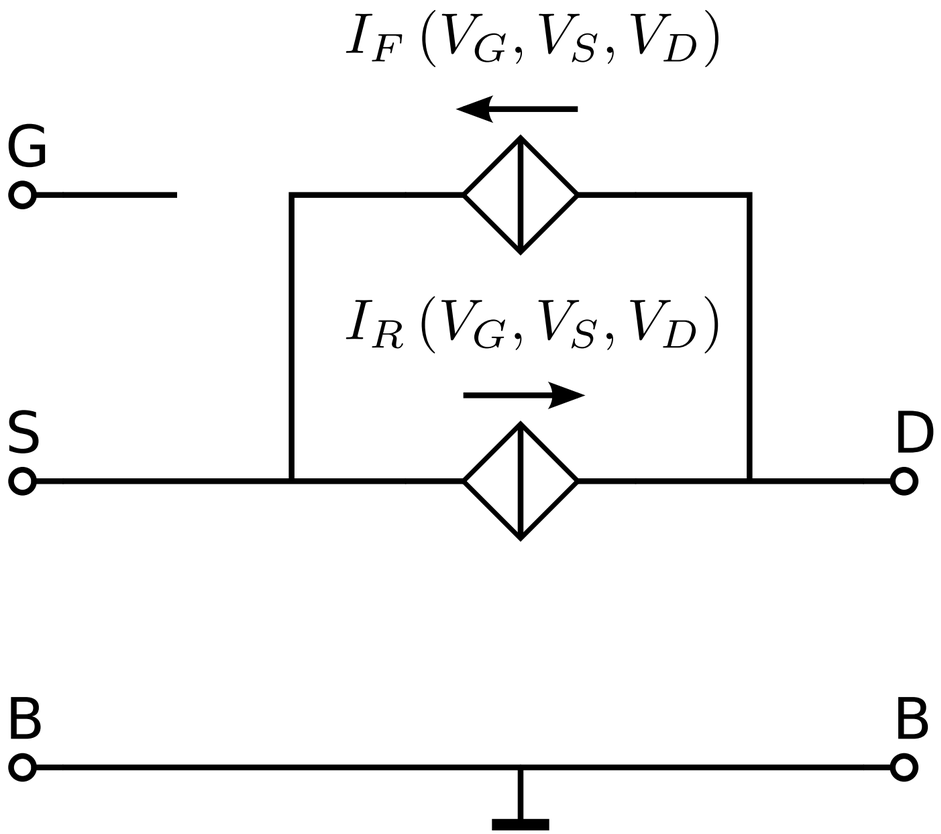

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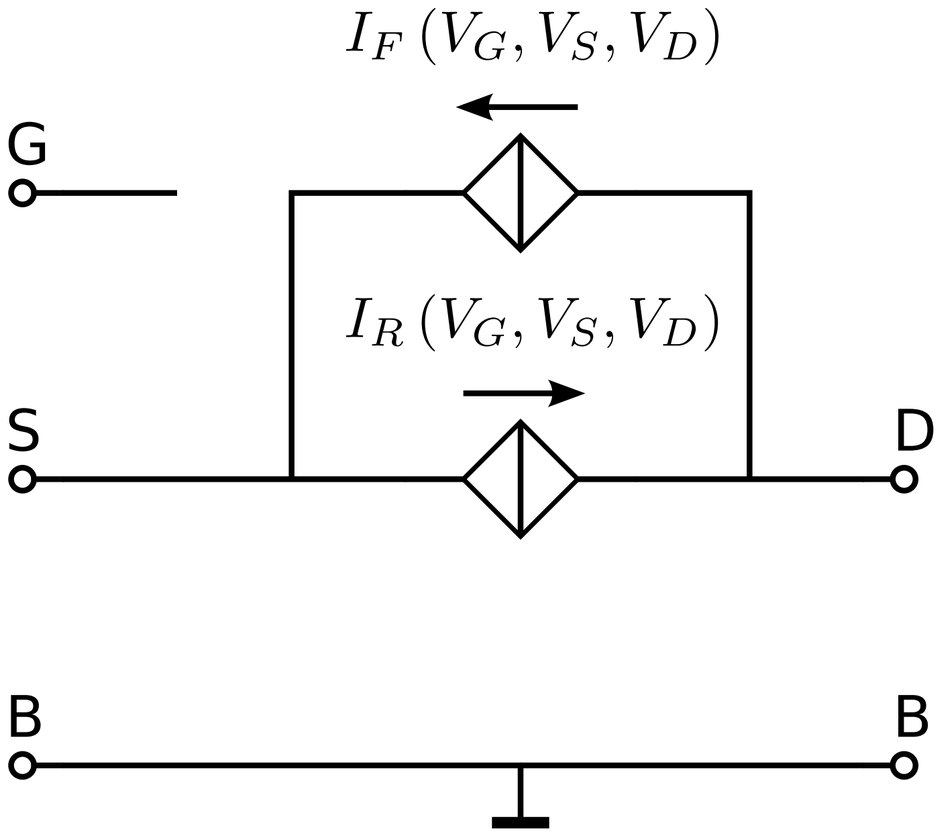

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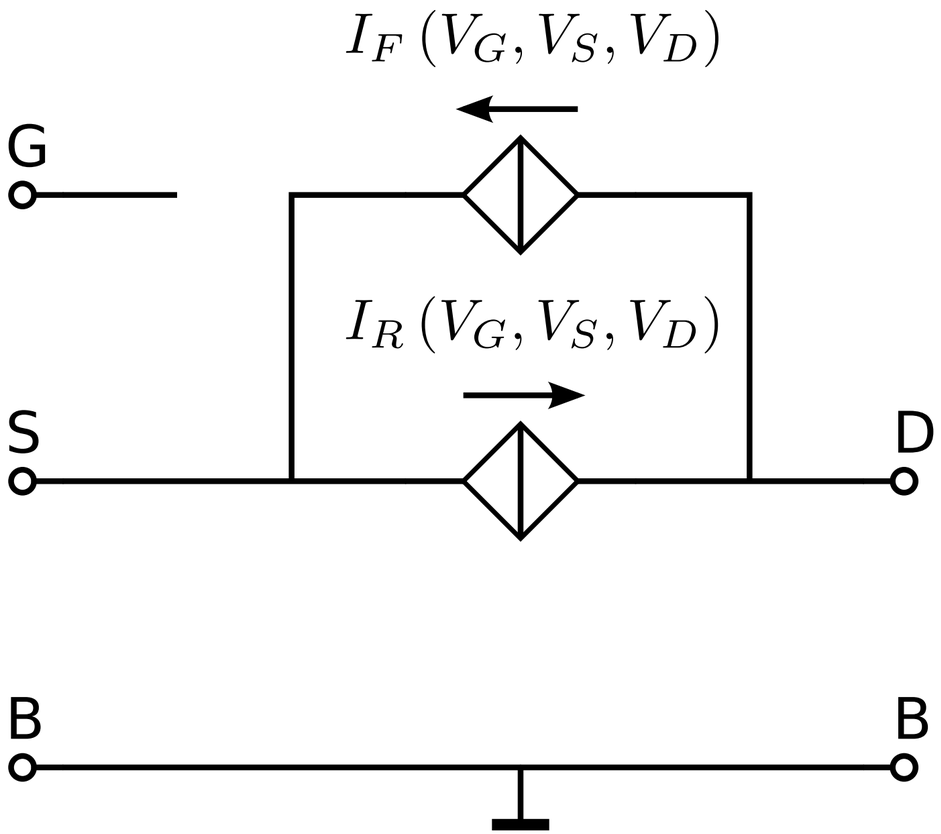

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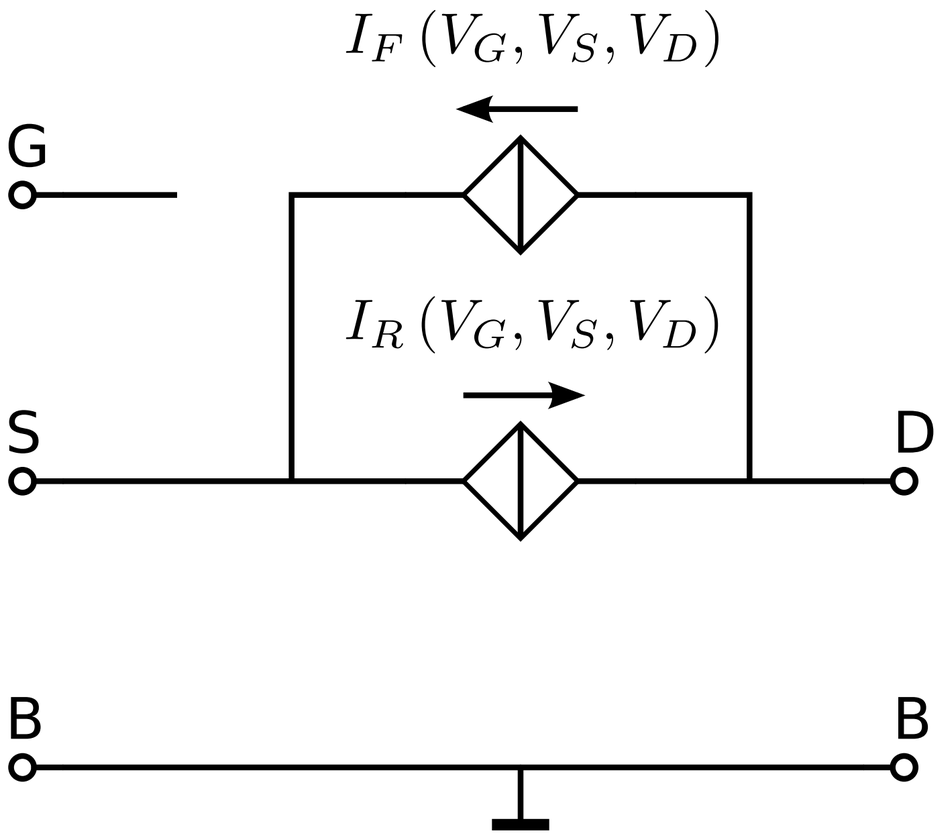

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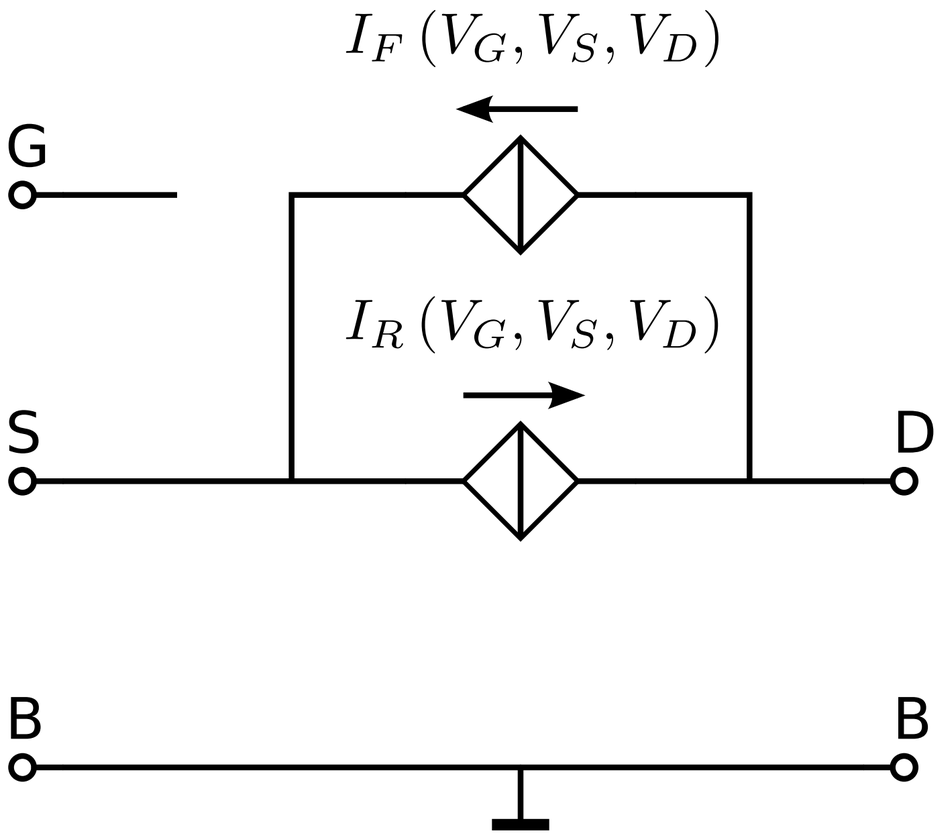

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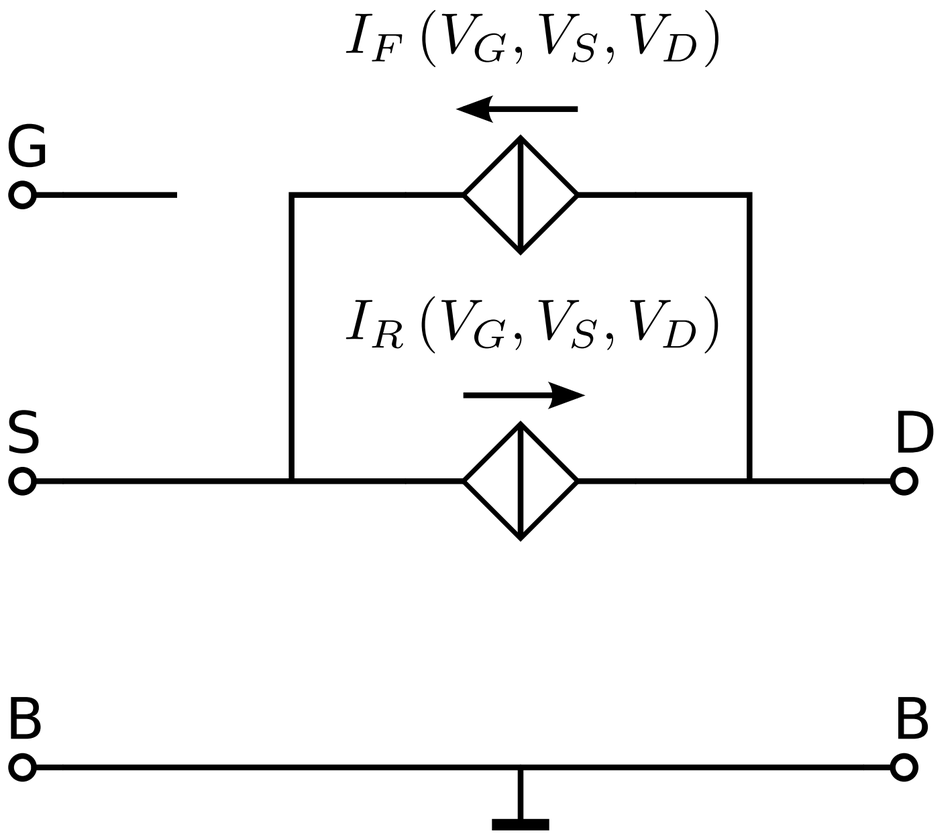

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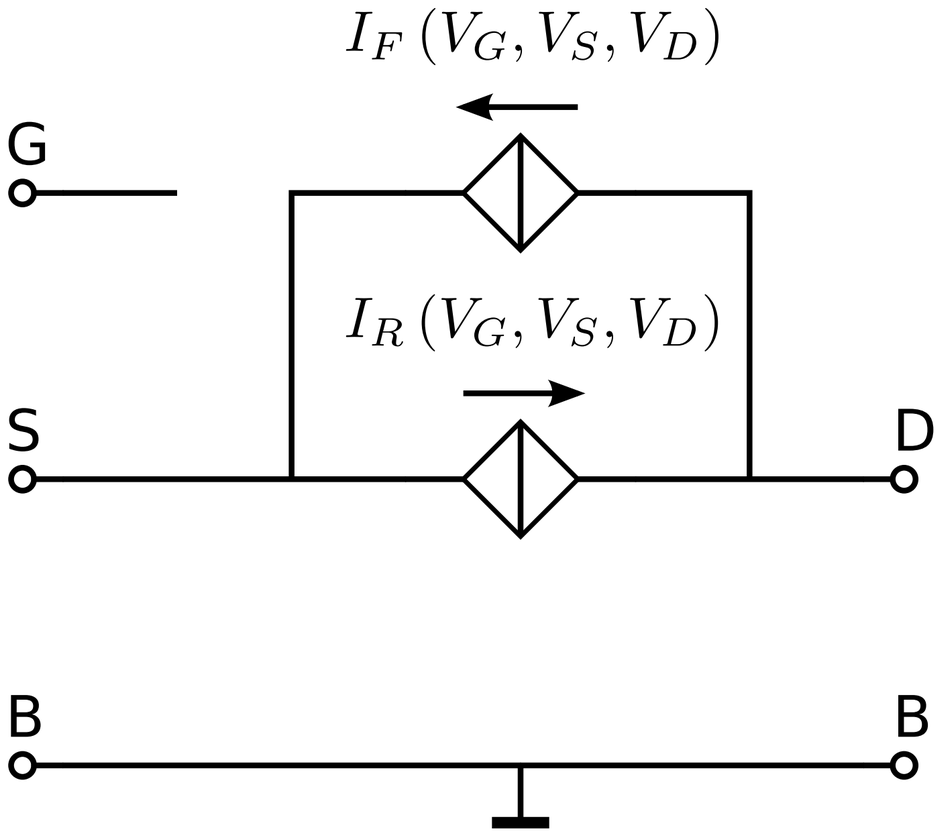

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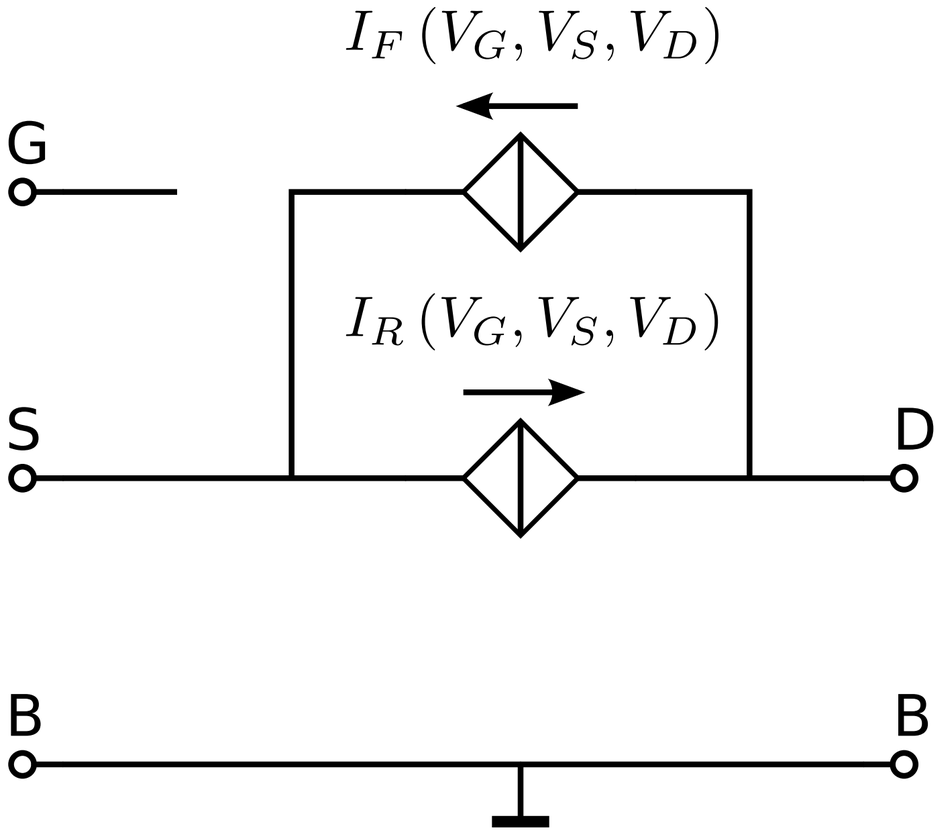

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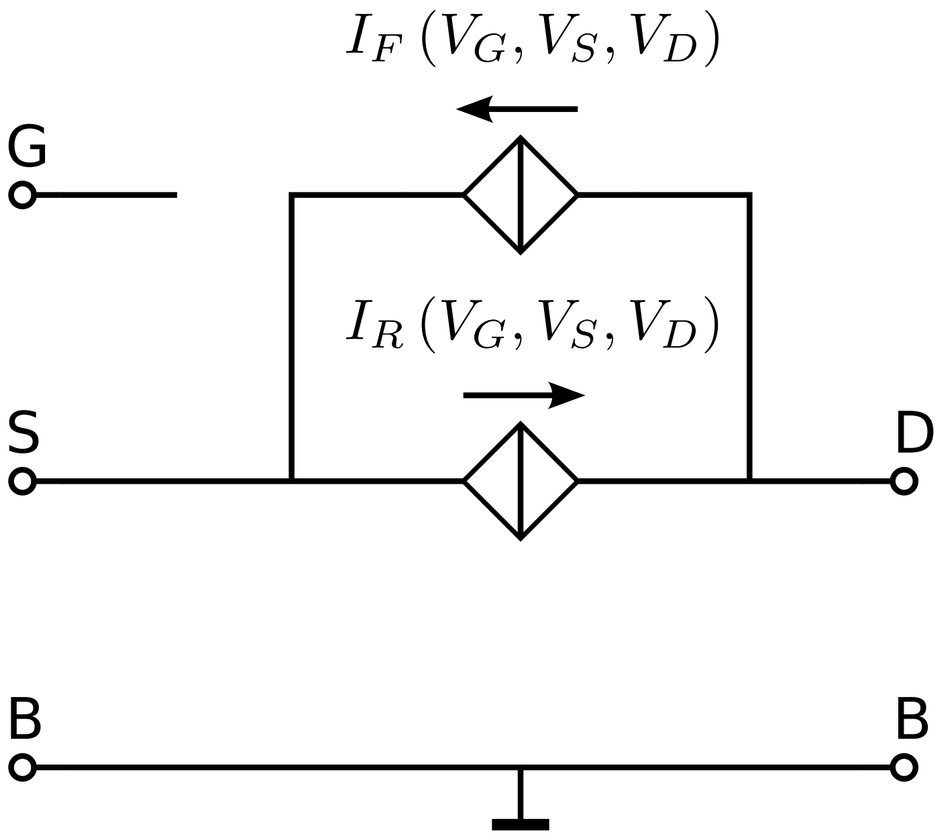

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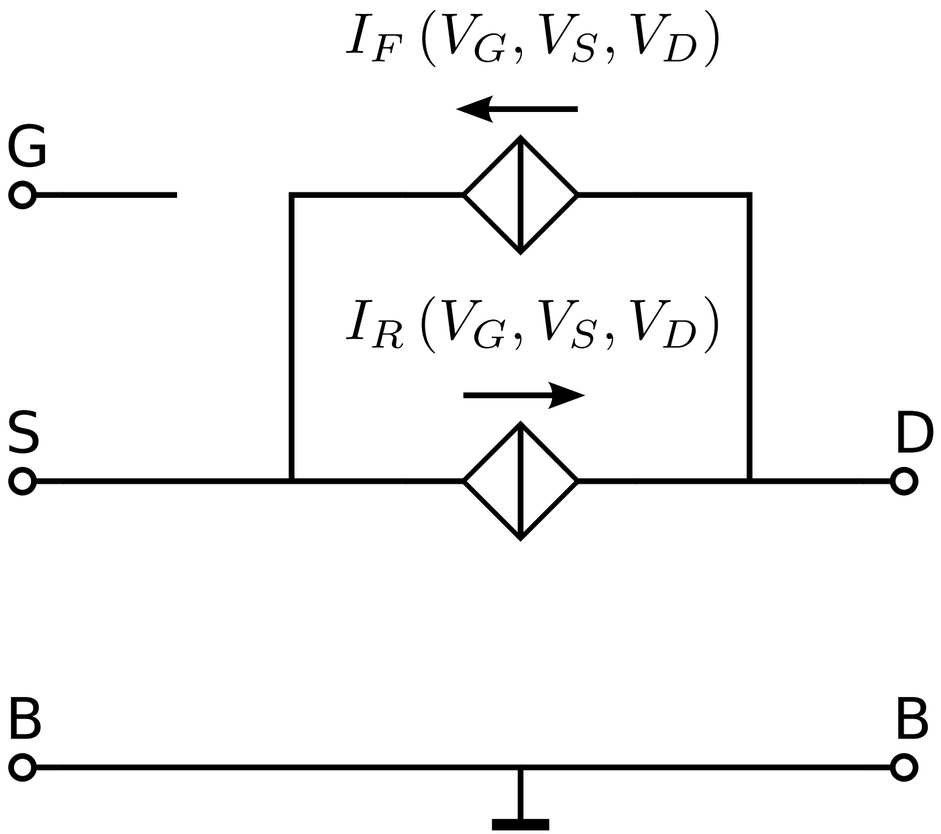

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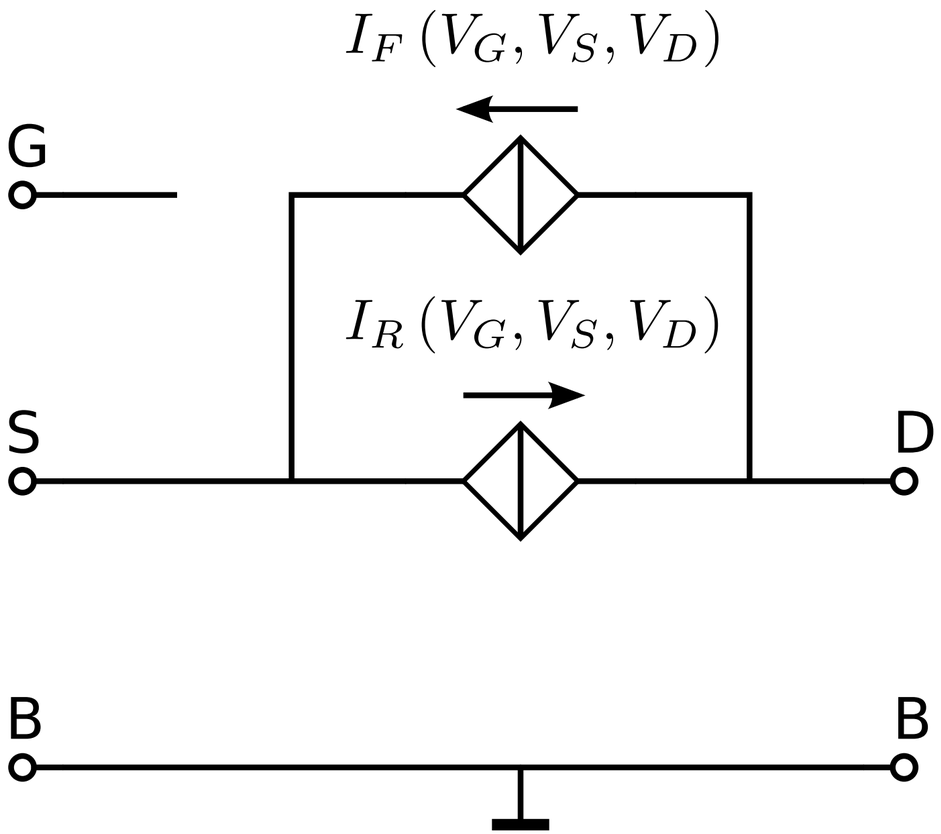

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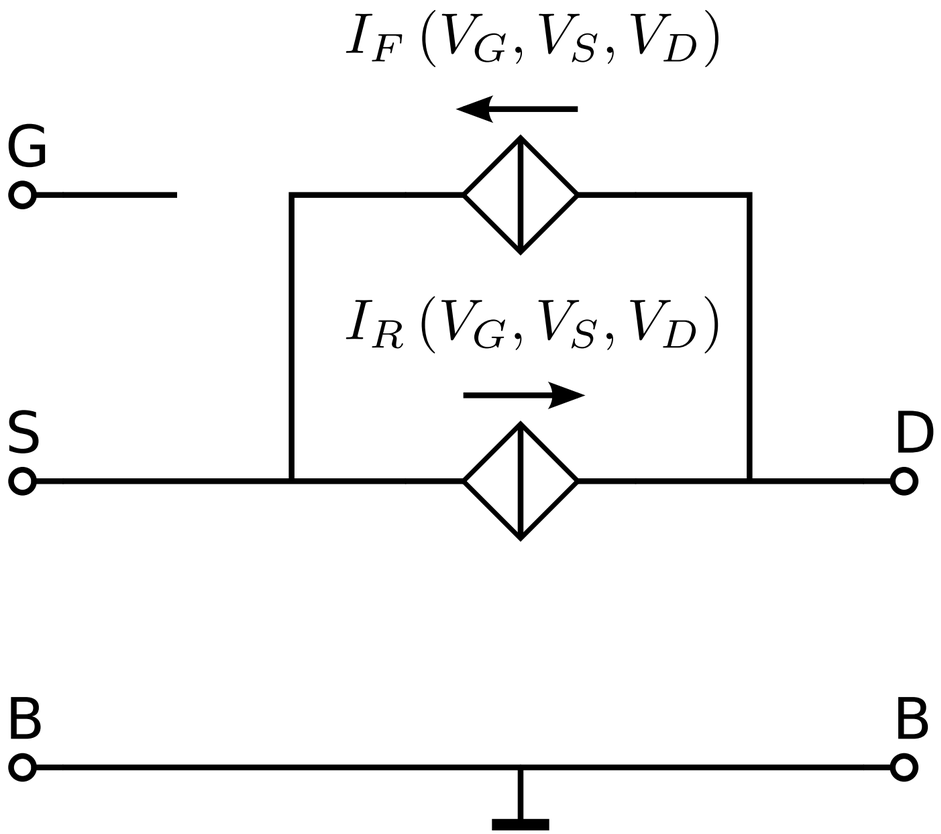

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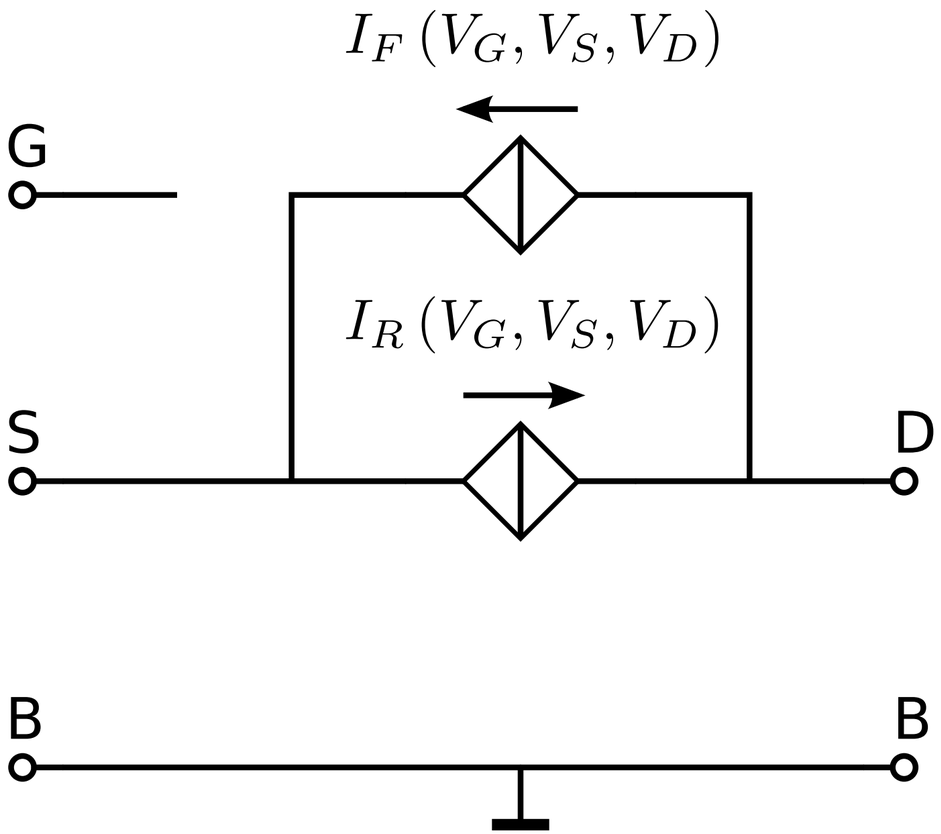

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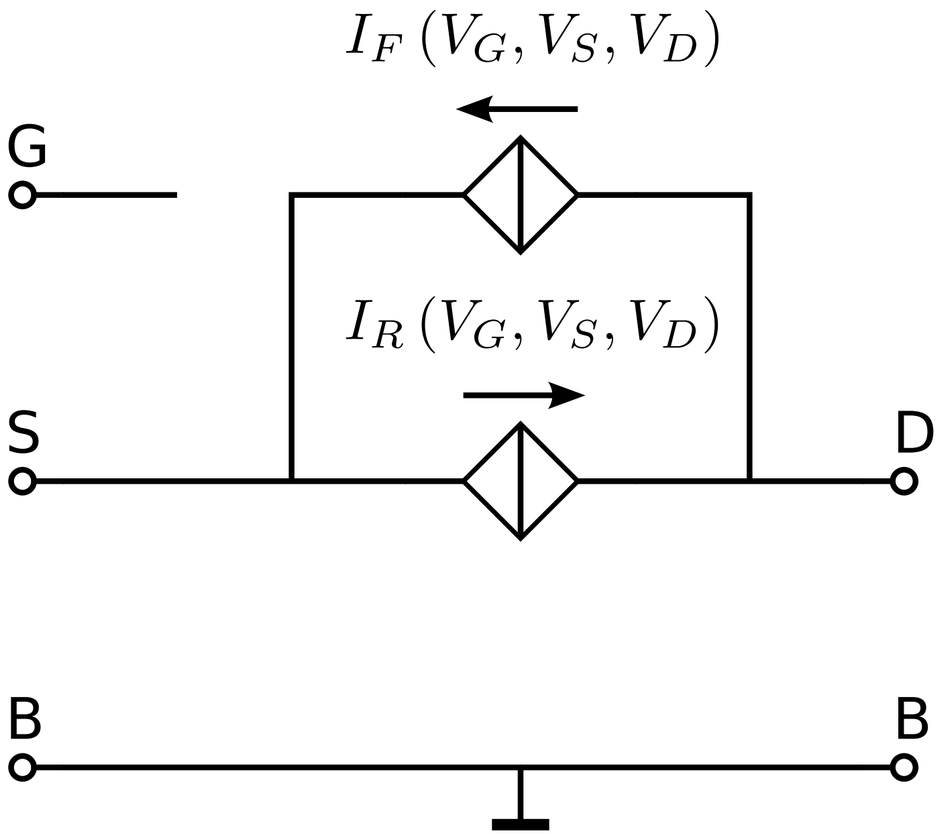

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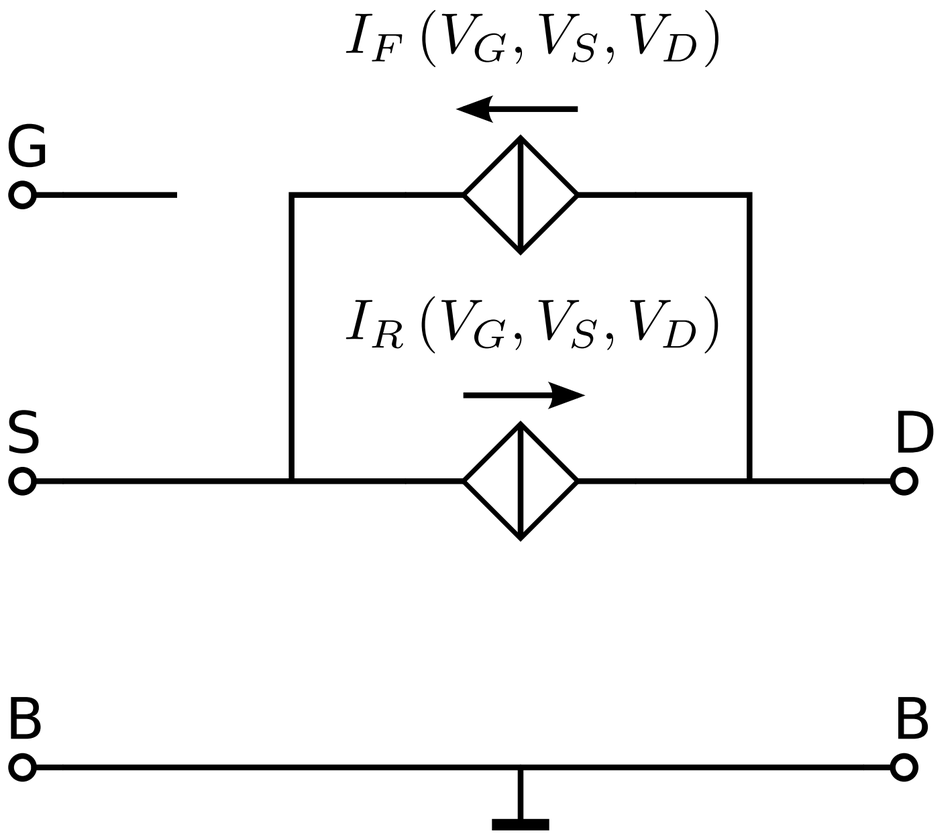

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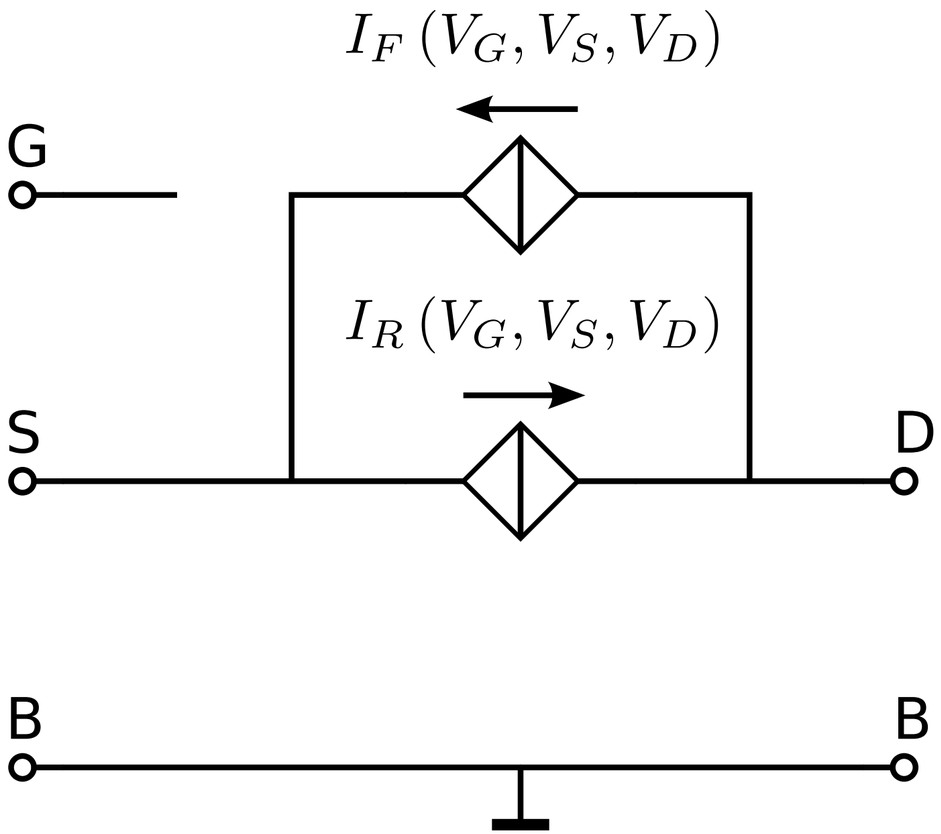

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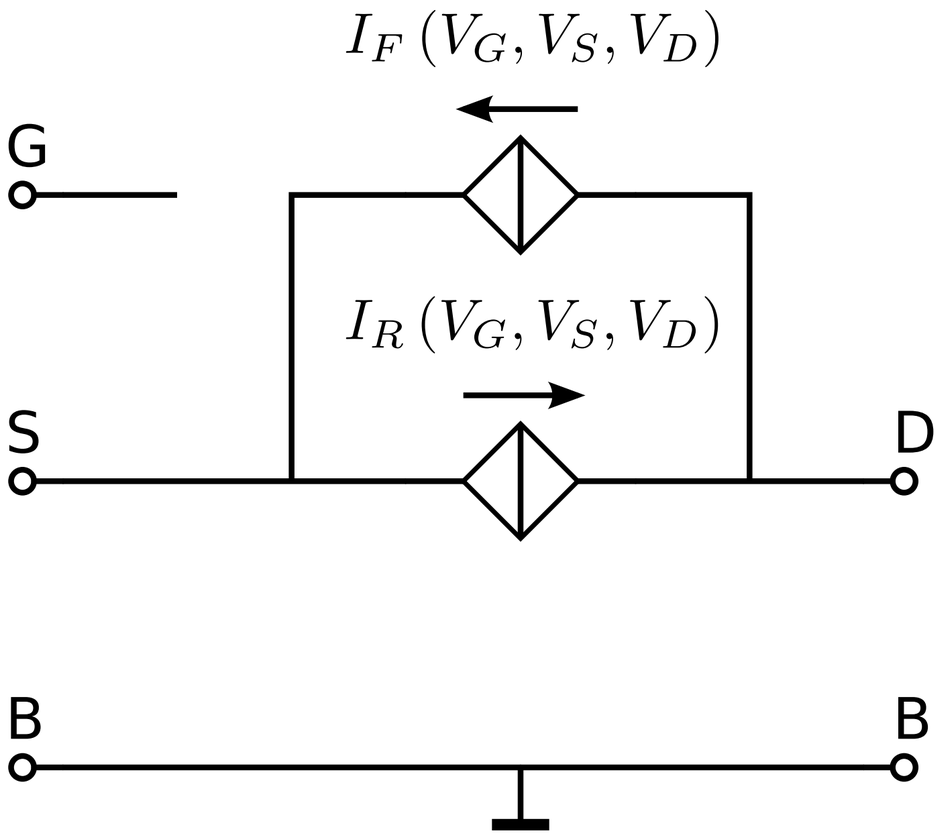

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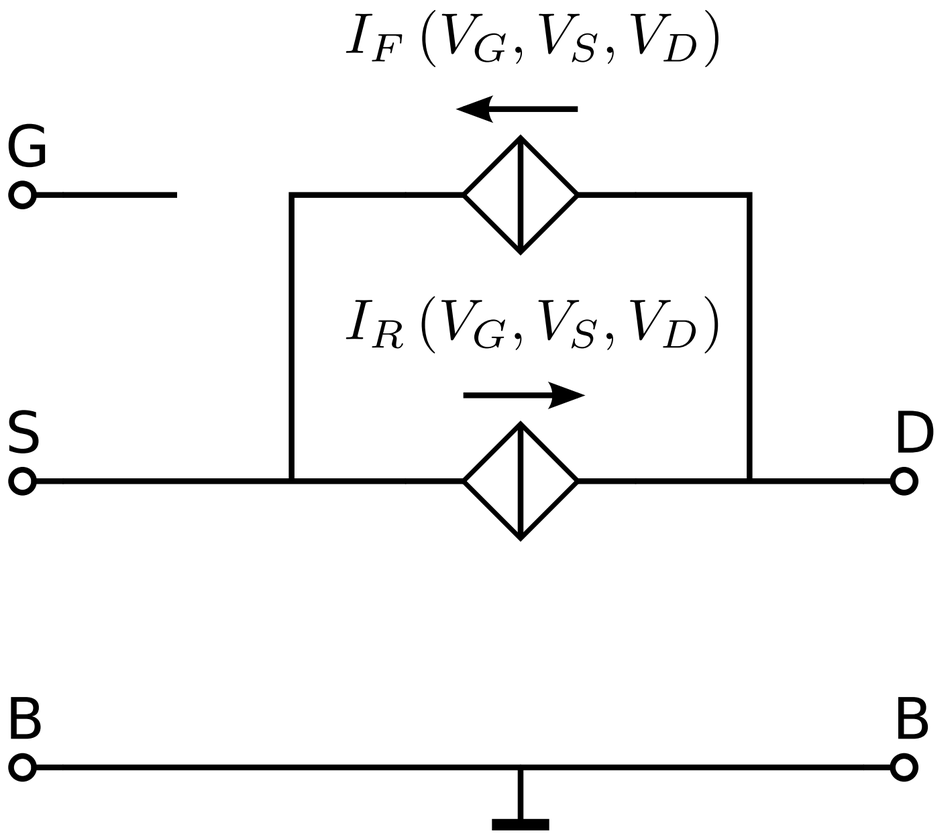

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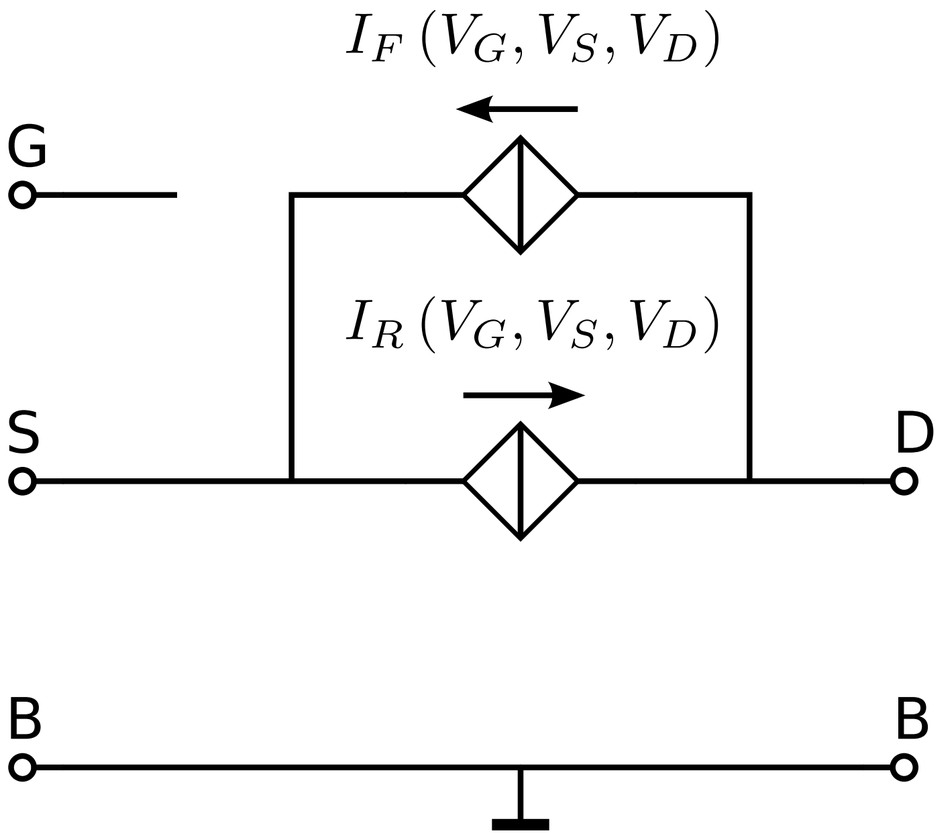

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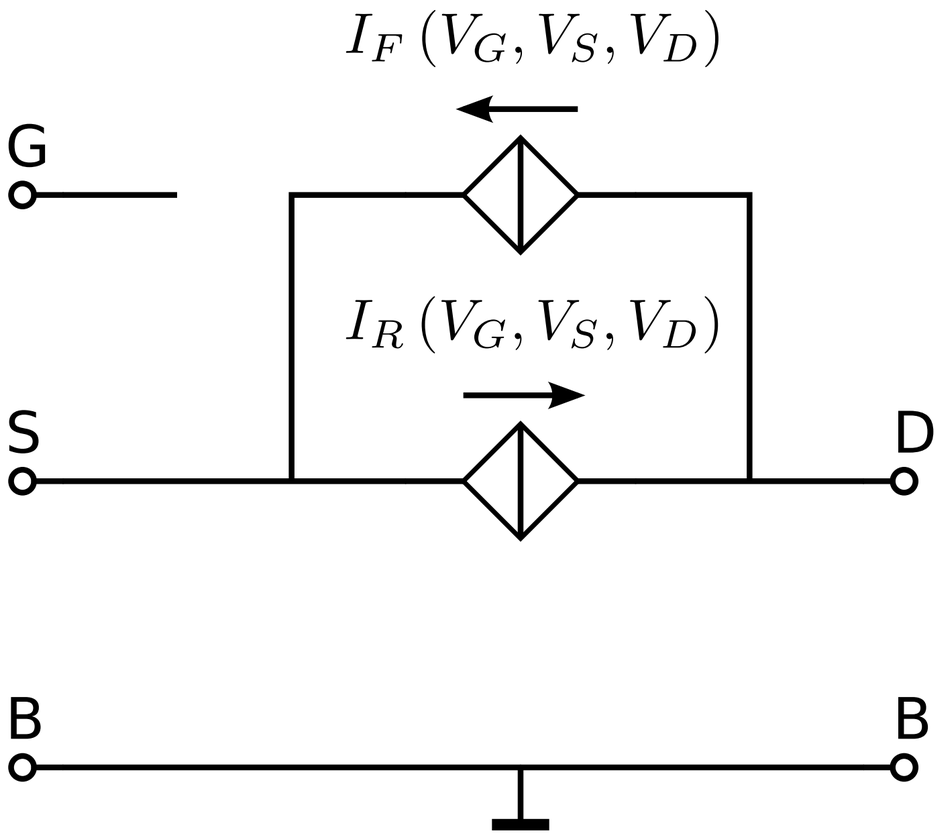

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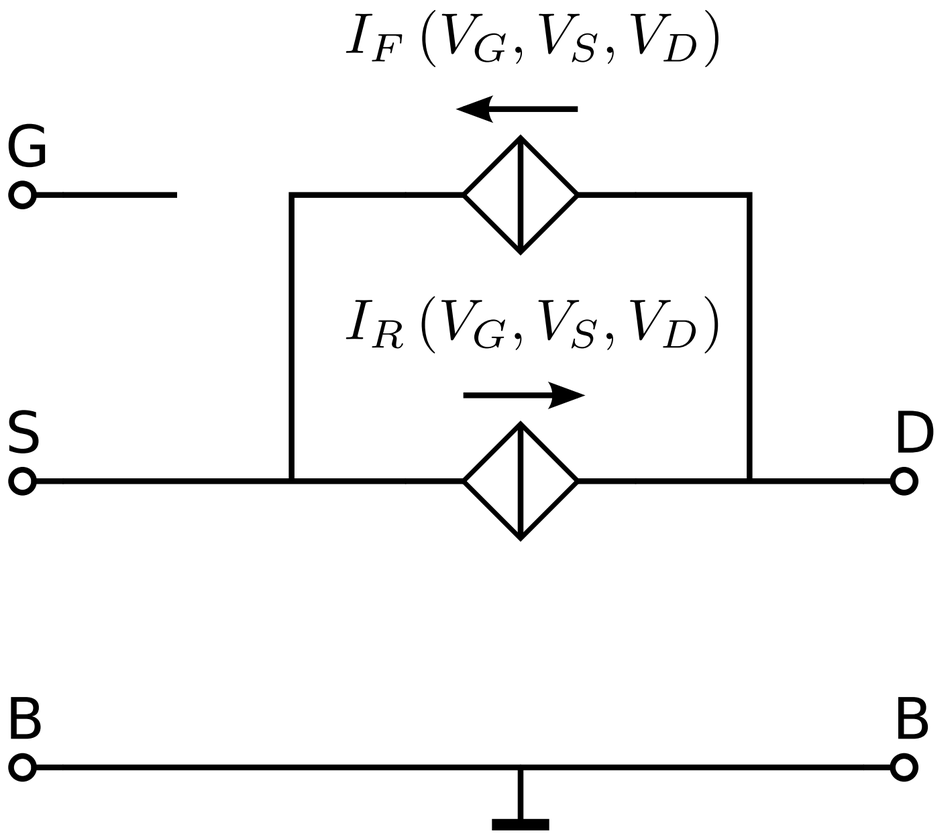

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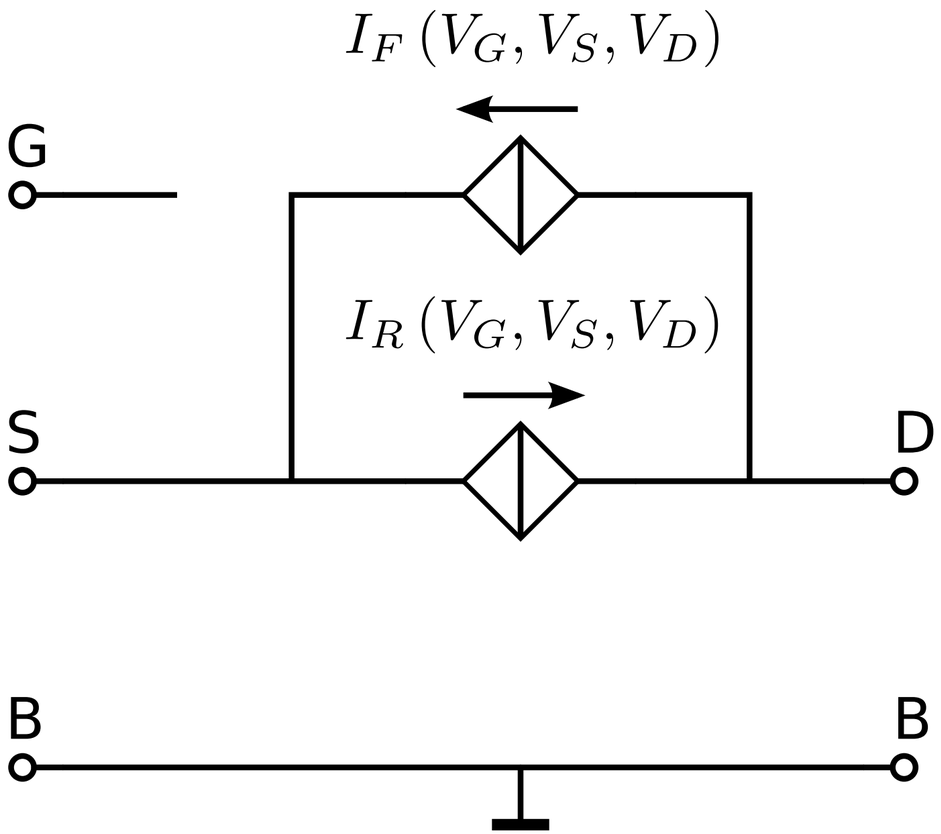

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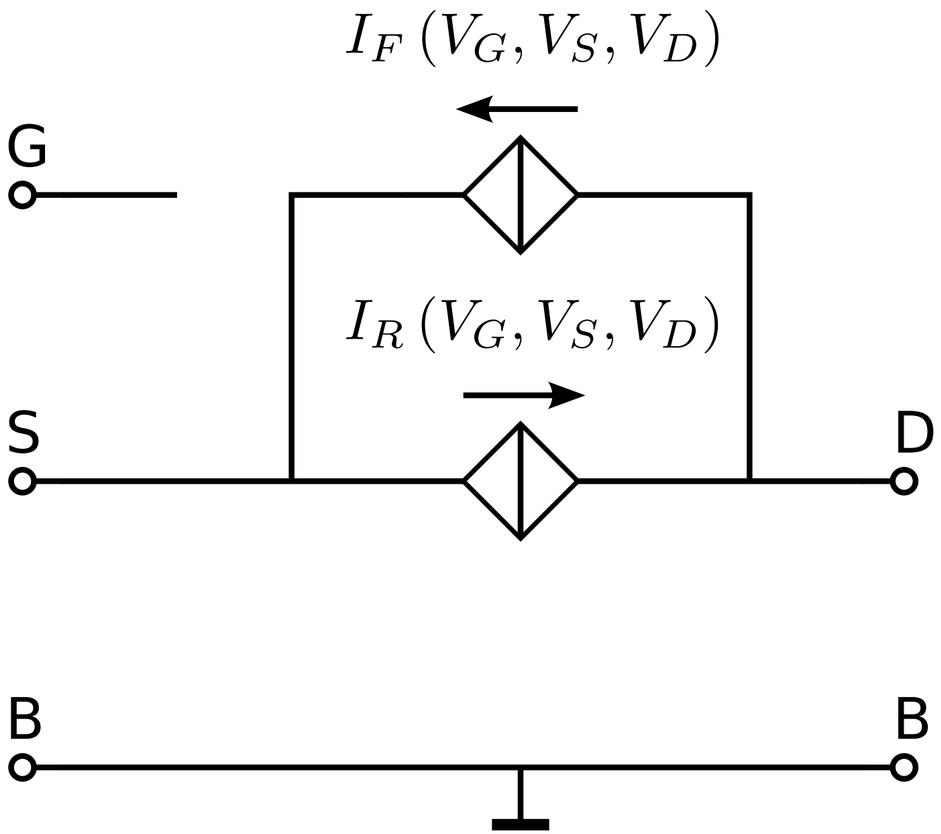

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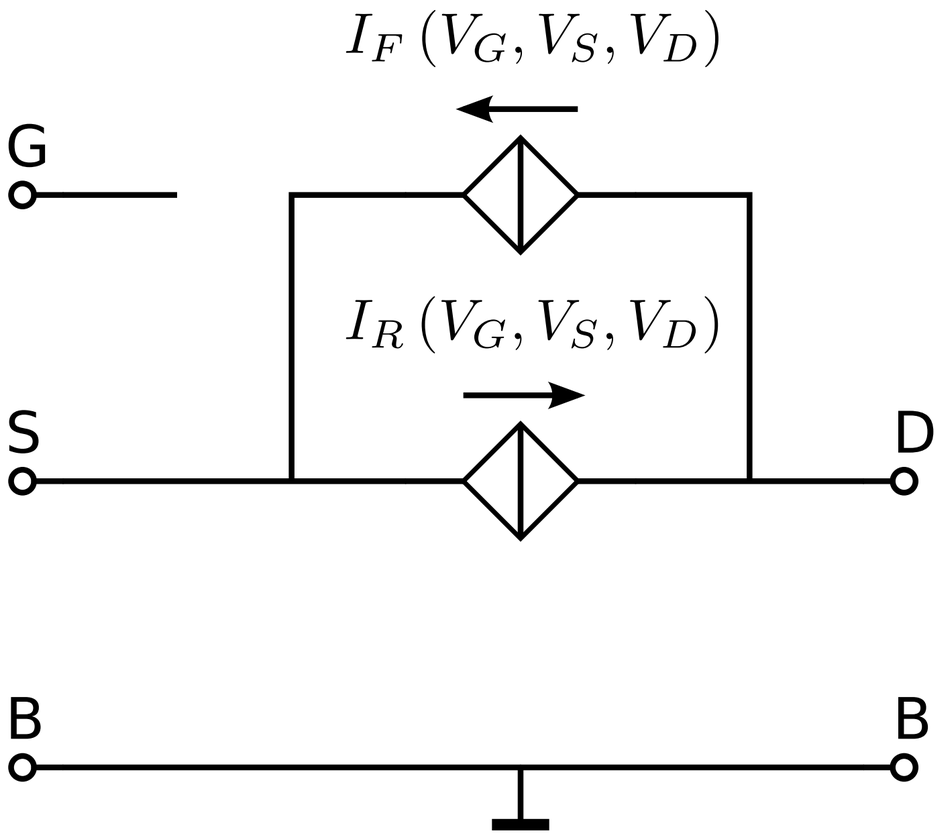

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Above critical inversion the small-signal transconductance
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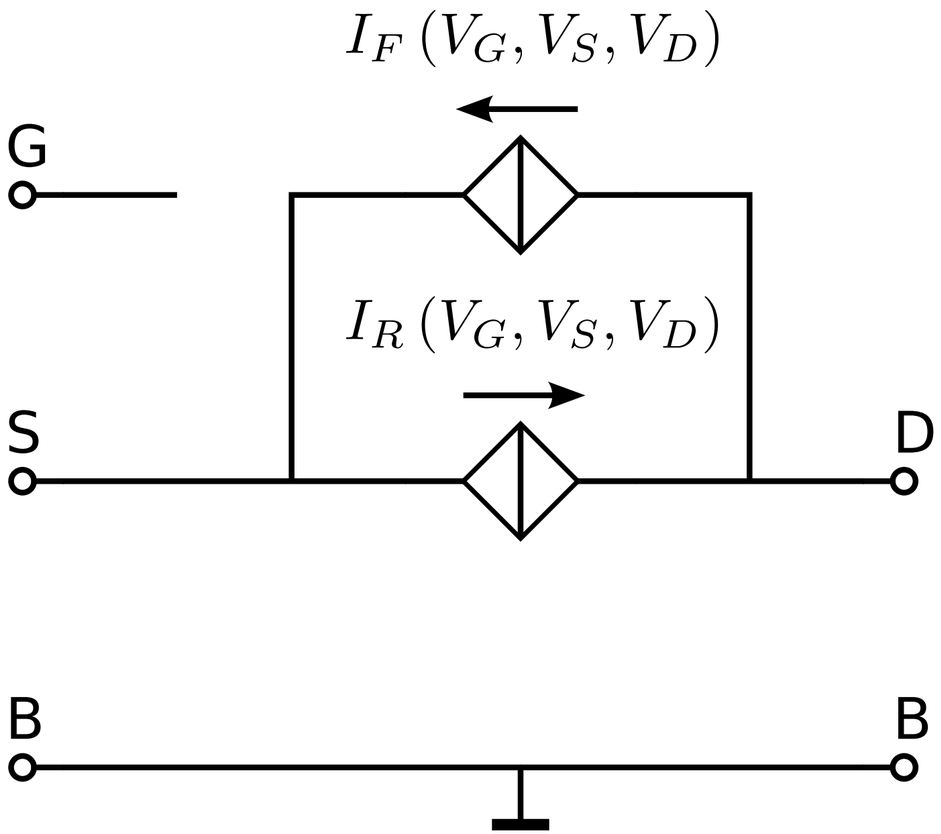

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MOS EKV model

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Small-signal model parameters can be expressed in terms of:

MOS EKV model

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- Technology parameters

MOS EKV model

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Binkley:
Tradeoffs and Optimization
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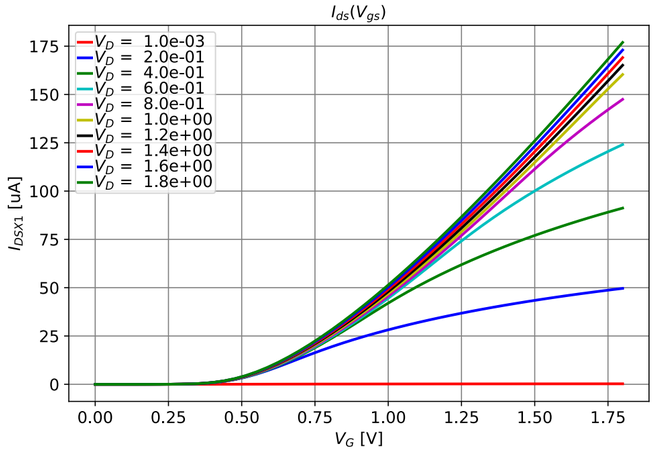
Tradeoffs and Optimization in Analog CMOS Design



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MOS EKV model

Small-signal model parameters can be expressed in terms of:

- Technology parameters
- Geometry parameters
- Operating conditions

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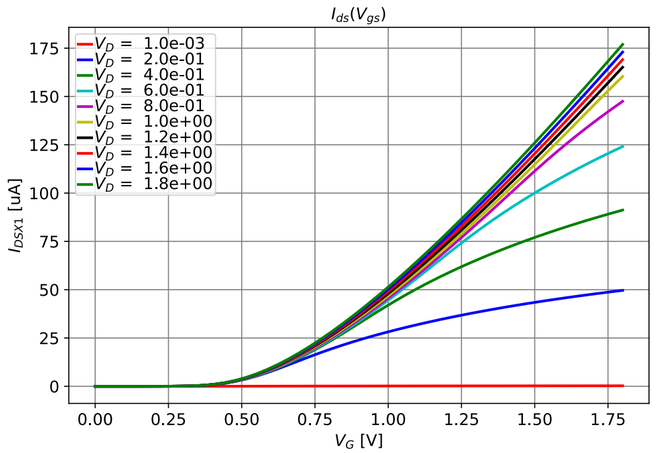

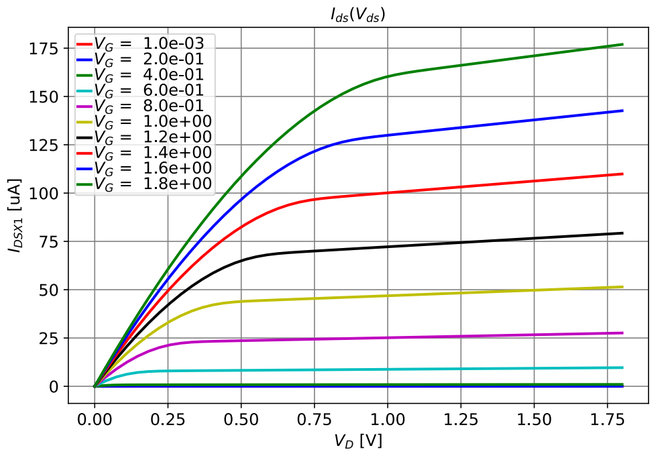

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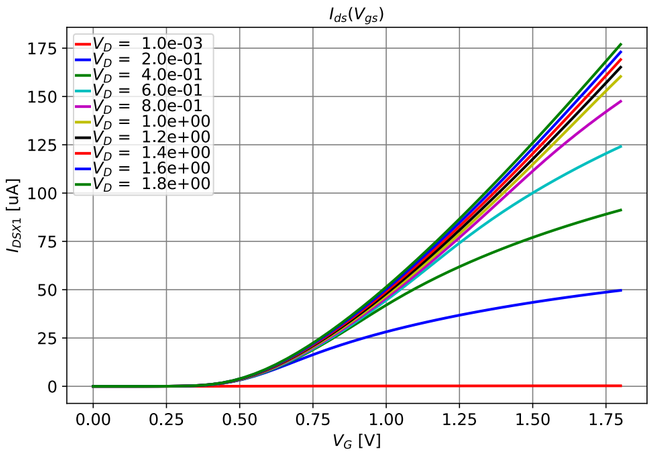

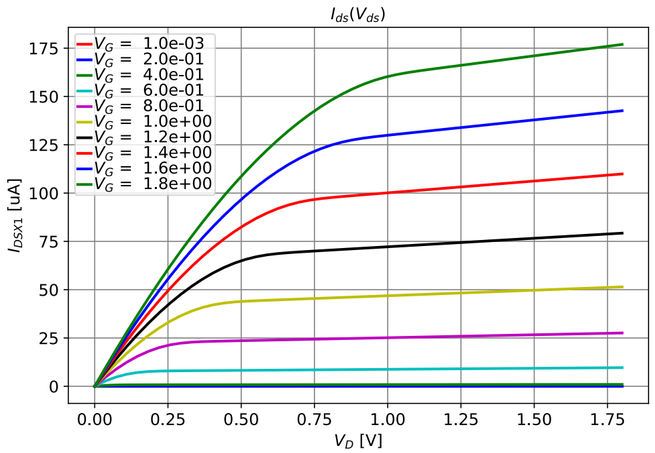

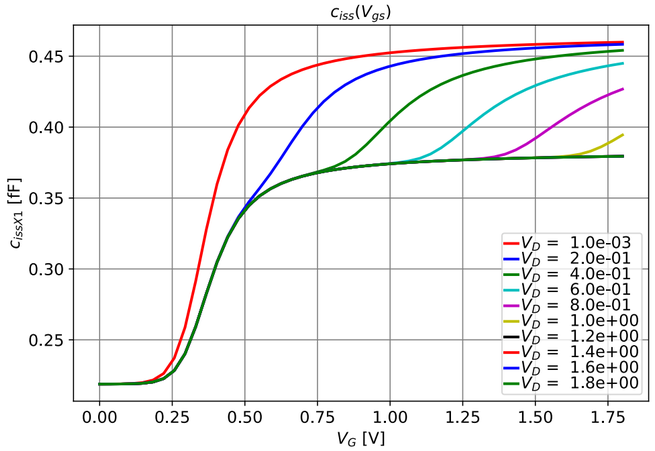

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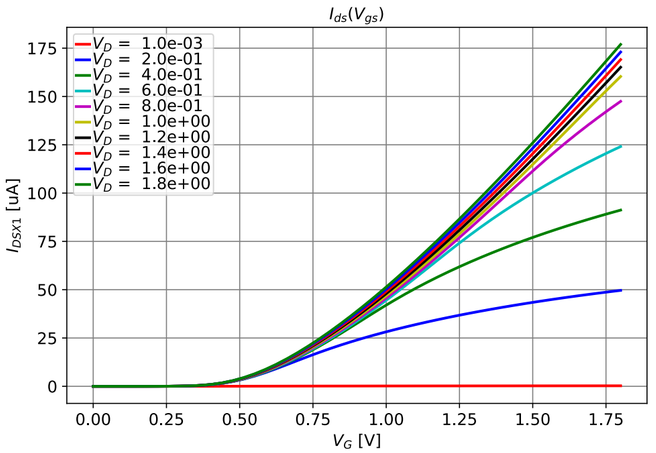

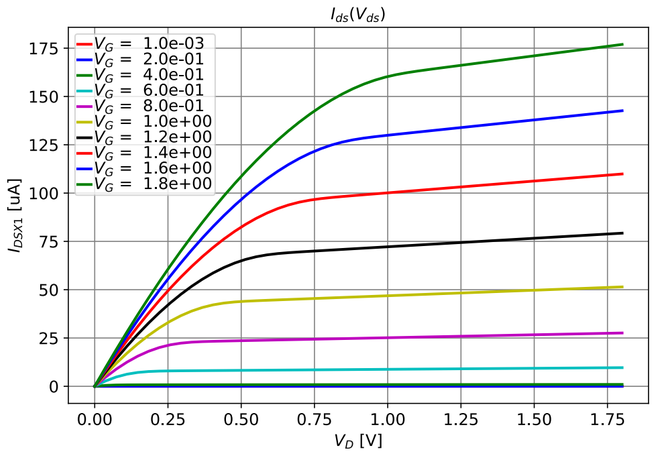

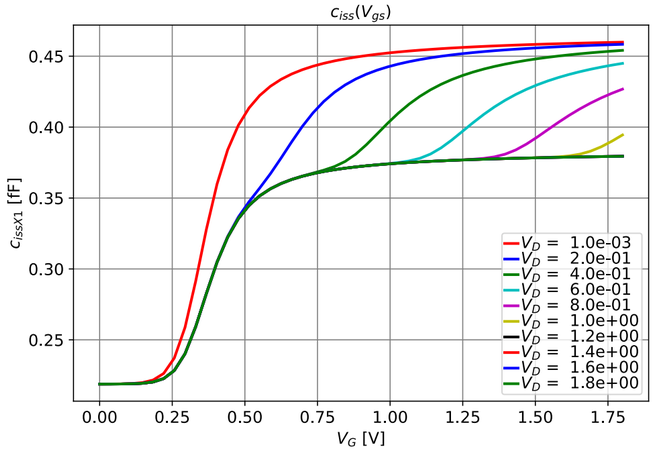

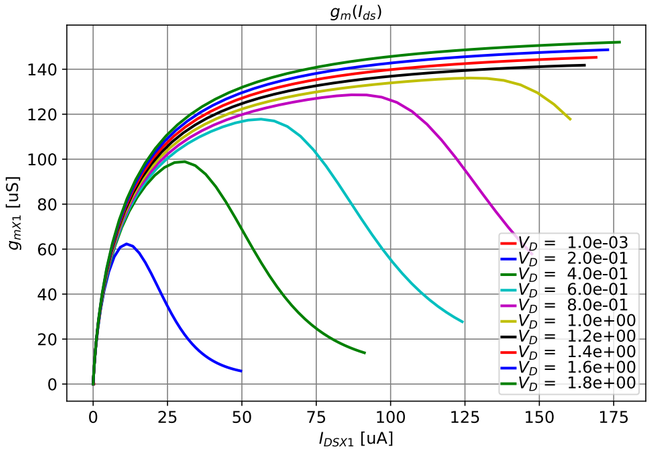

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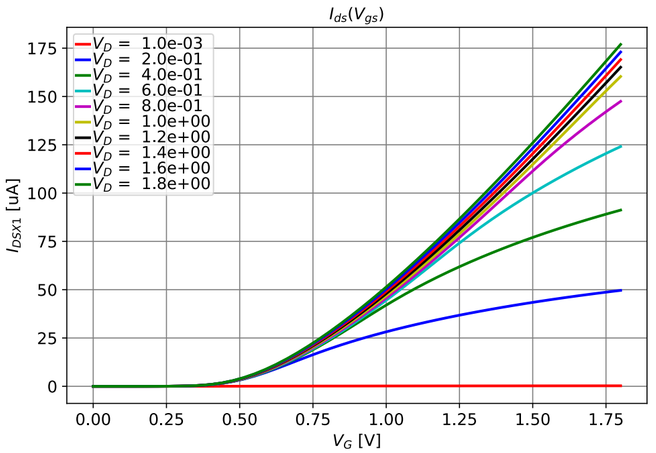

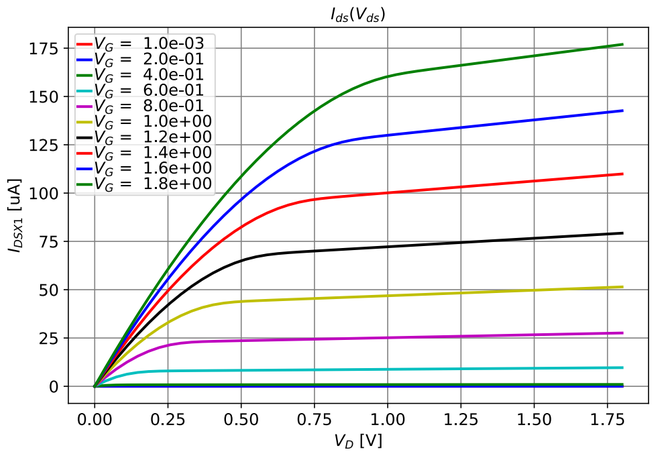

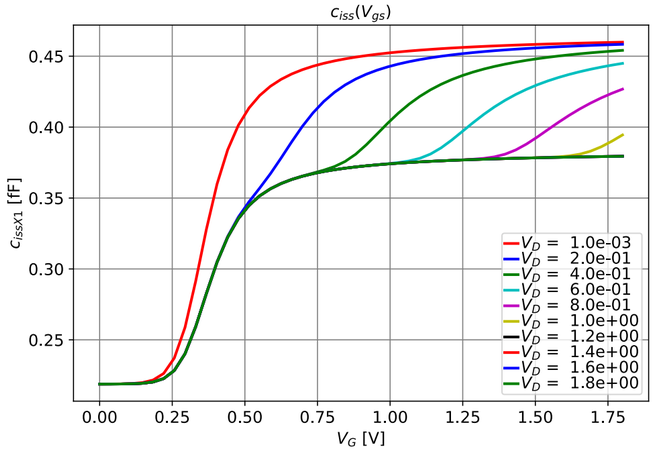

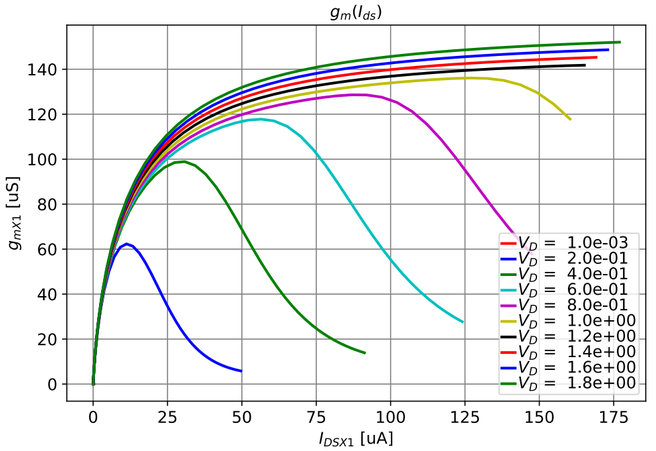

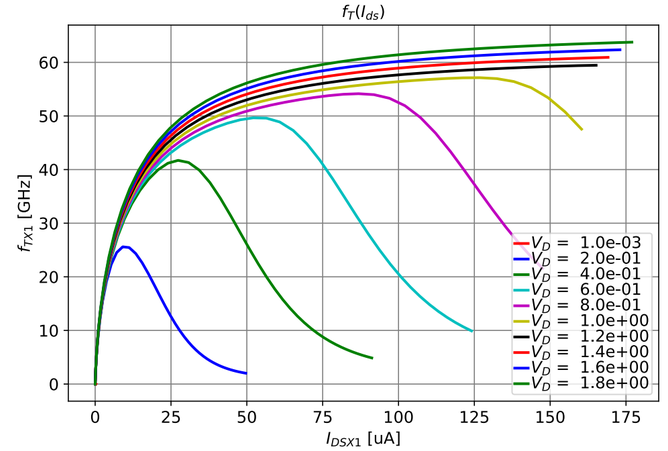

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SLiCAP MOS small-signal model

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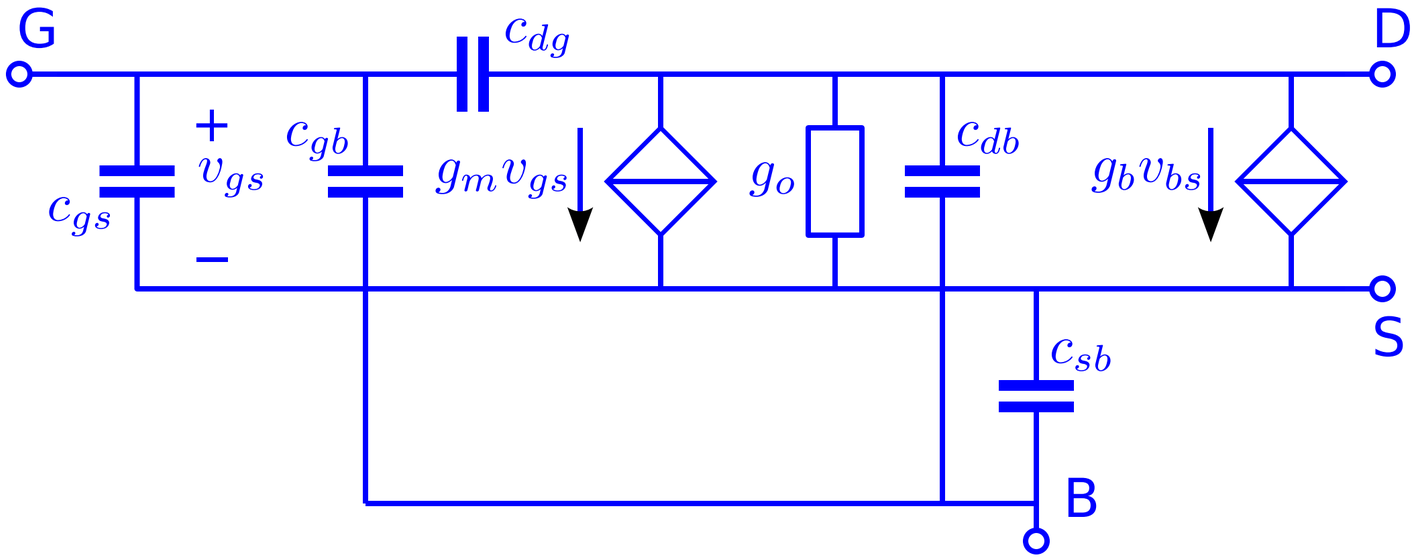
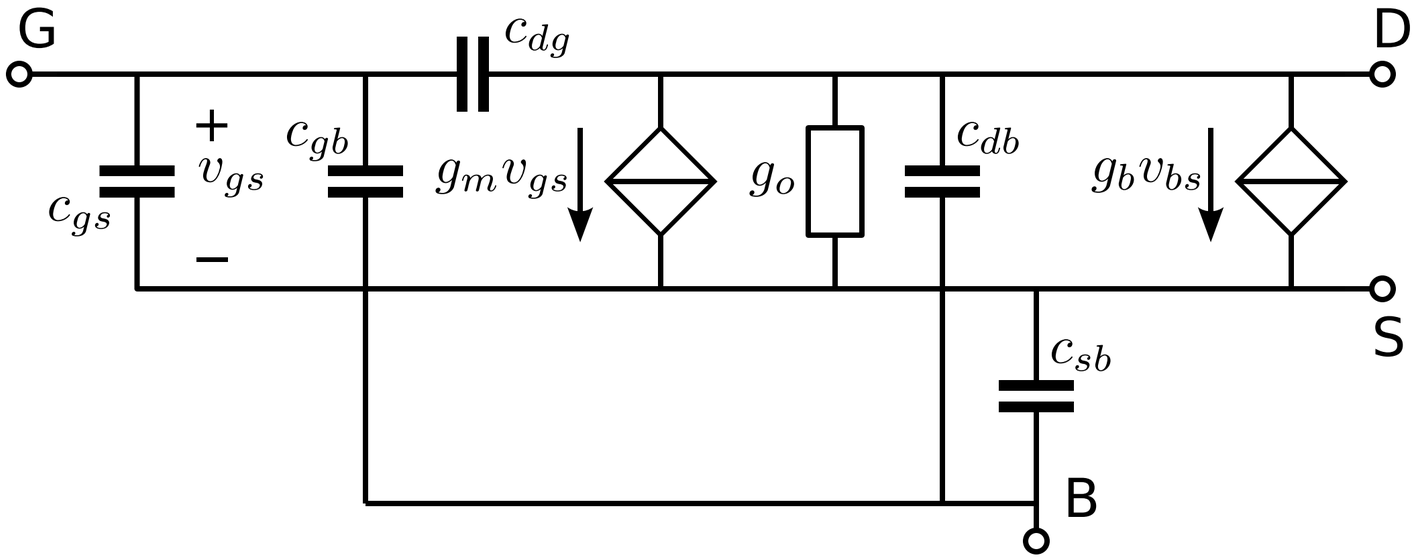
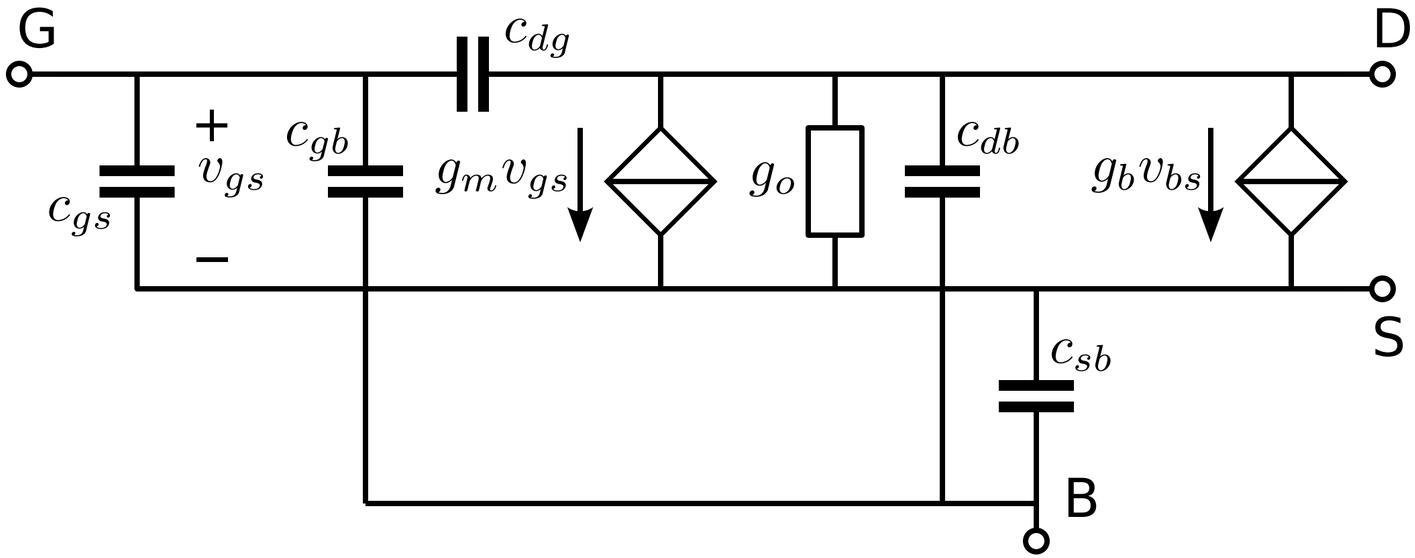


SLiCAP MOS small-signal model



Physical constants in SLiCAPmodels.lib

SLiCAP MOS small-signal model



Physical constants in SLiCAPmodels.lib

CMOS18 technology parameters in SLiCAPmodels.lib

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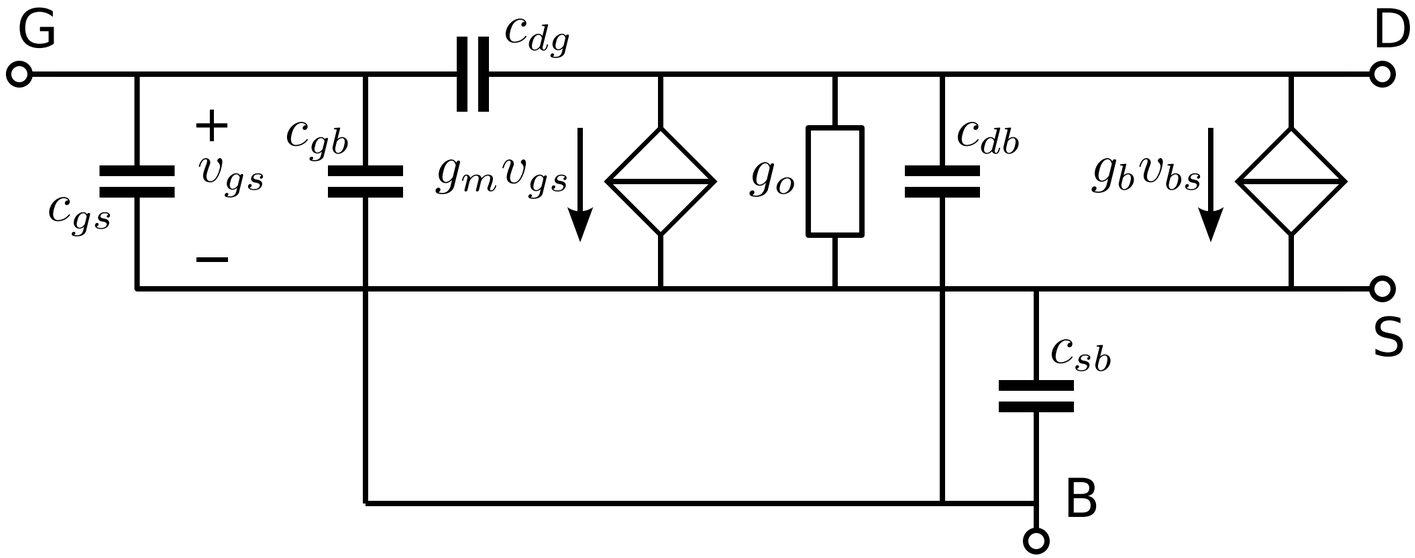

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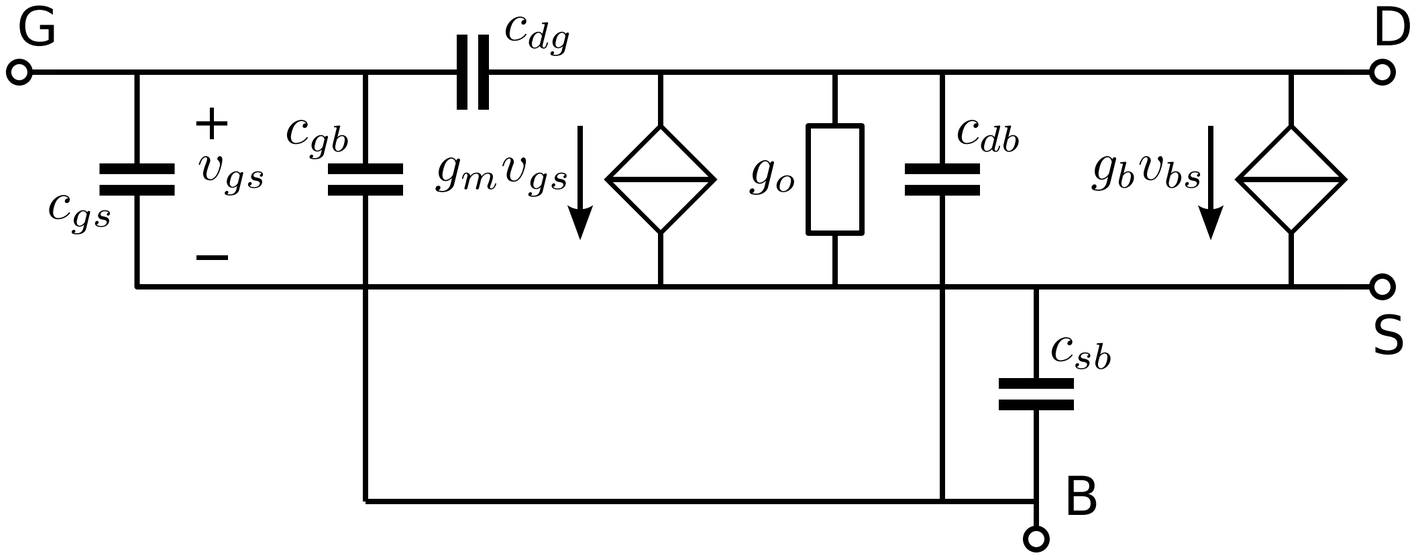
CMOS18 technology parameters in SLiCAPmodels.lib

Device equations in subcircuit definition of the small signal model in SLiCAP.lib

SLiCAP MOS small-signal model



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