Structured Electronic Design

Common Drain Stage

Anton J.M. Montagne

CD stage introduction

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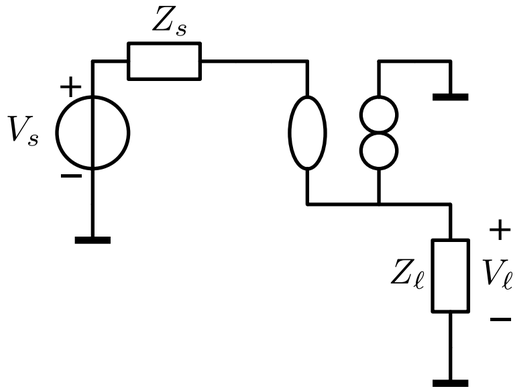

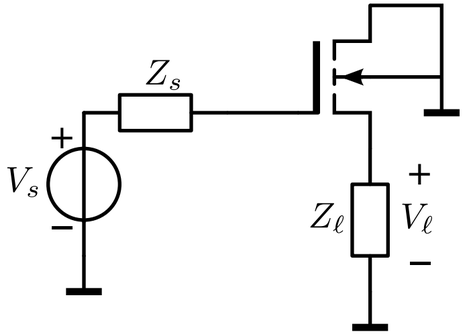

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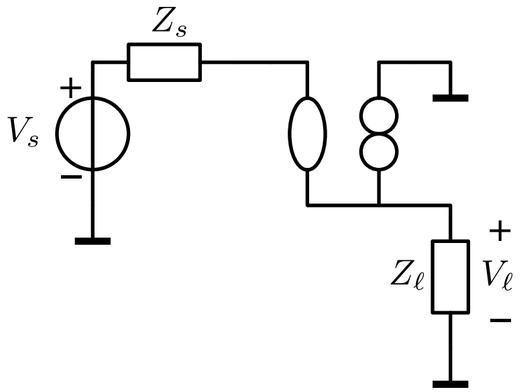

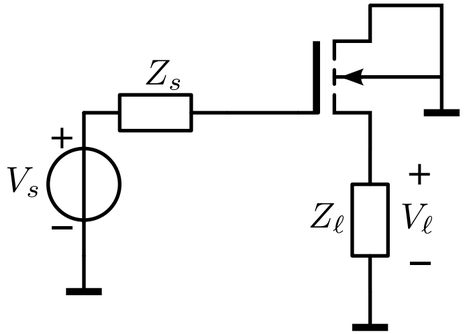

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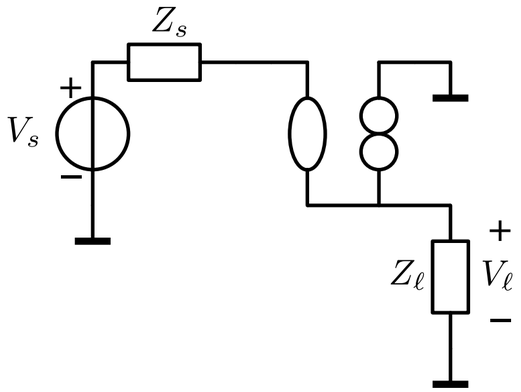

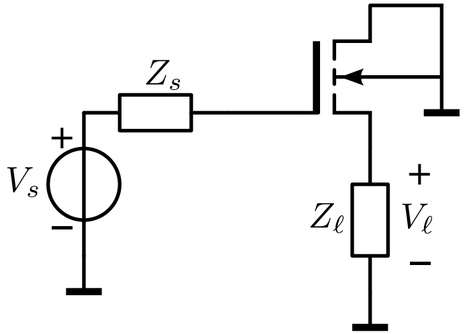

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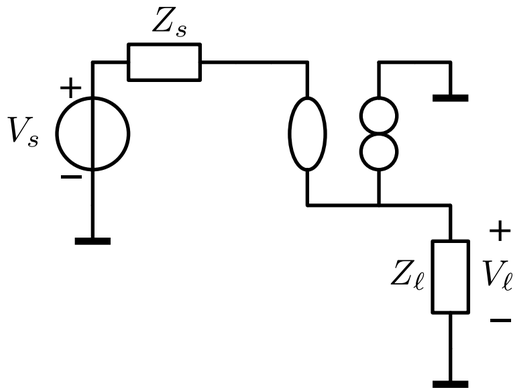

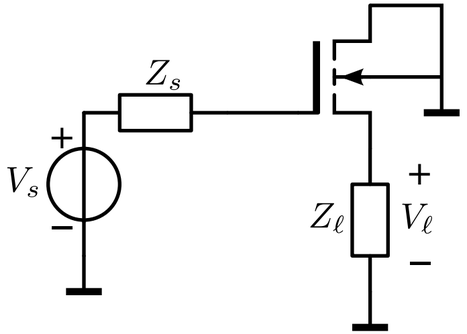

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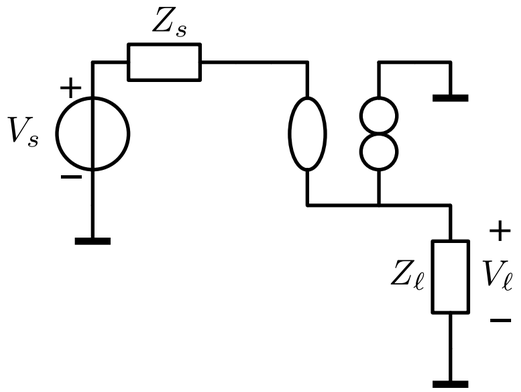

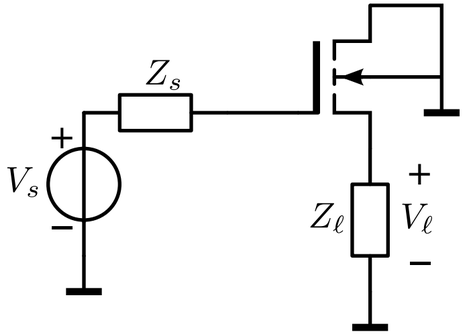

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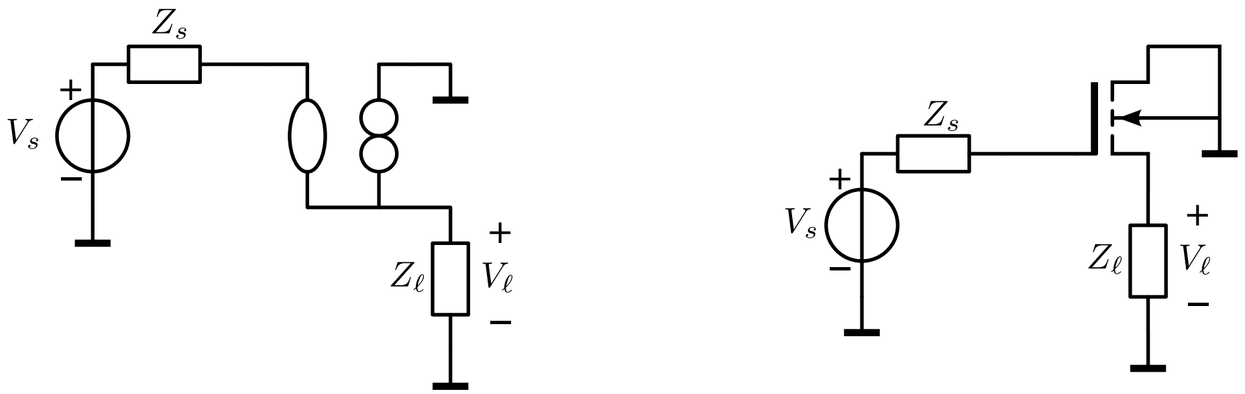

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2: False

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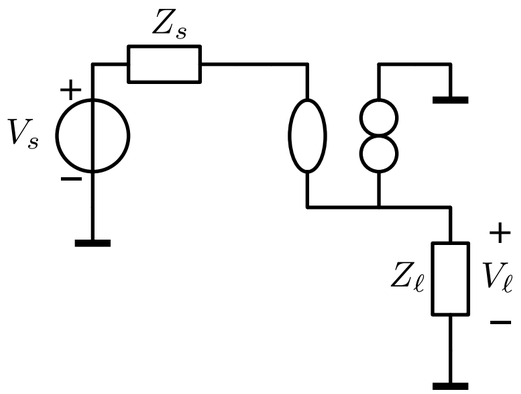

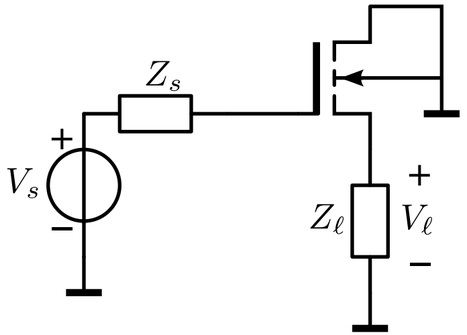

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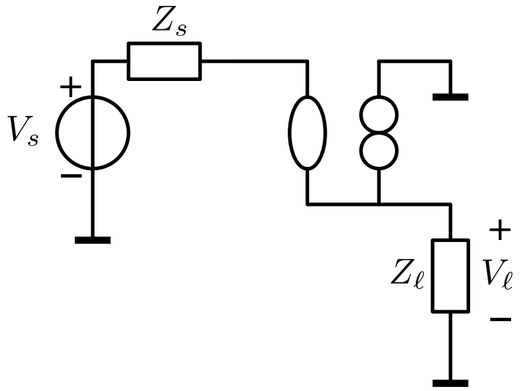

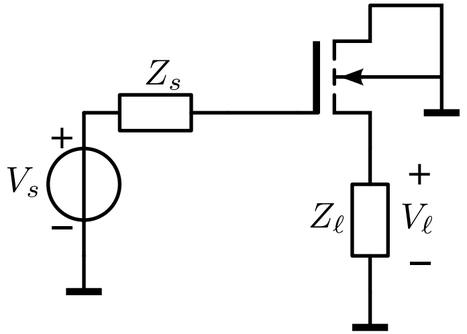

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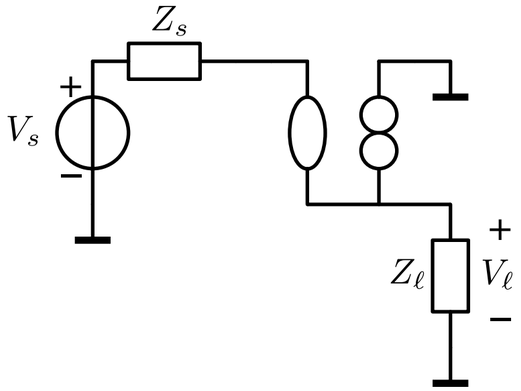

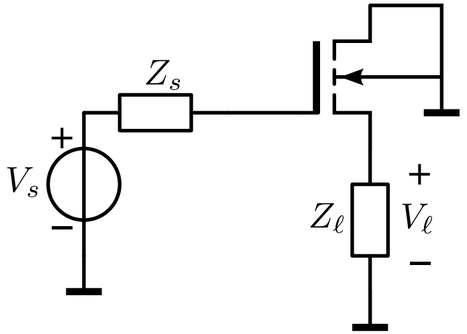

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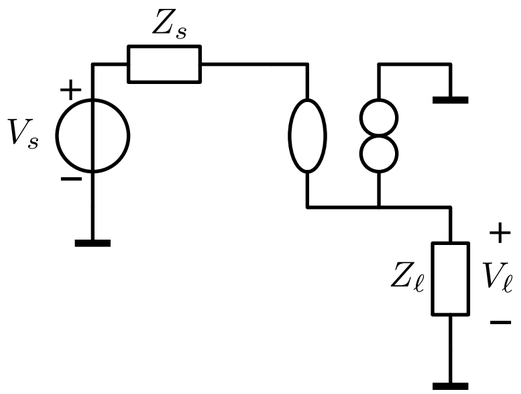

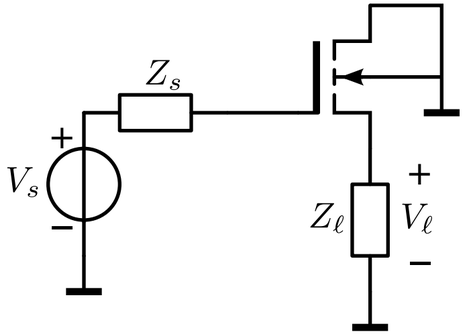

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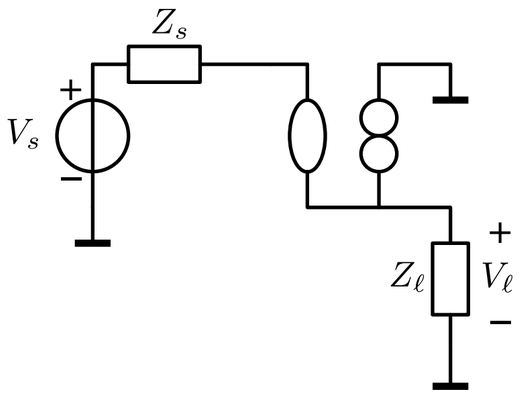

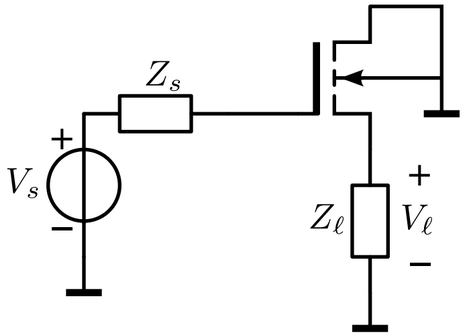

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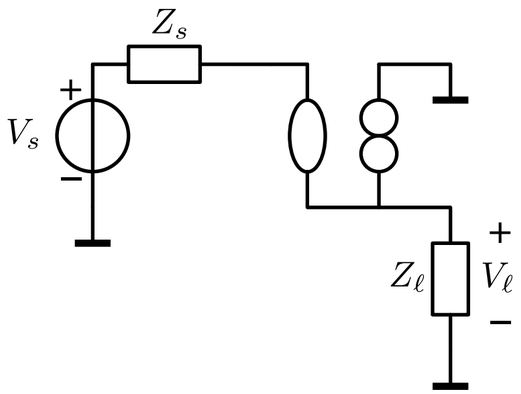

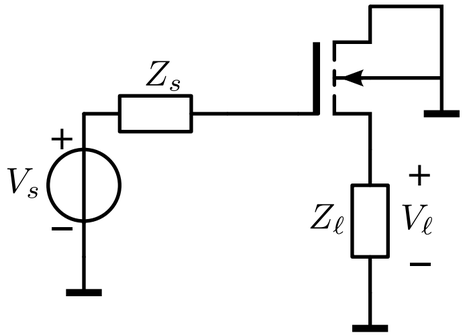

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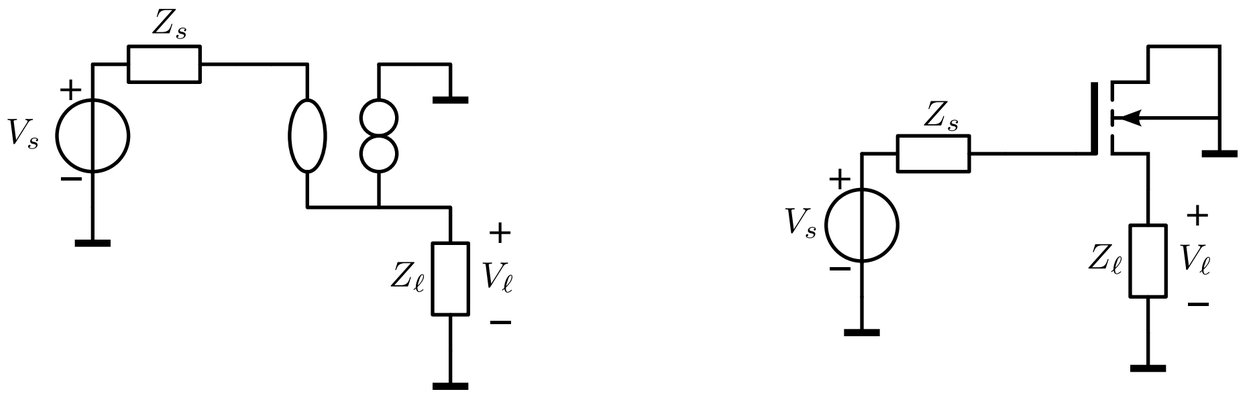

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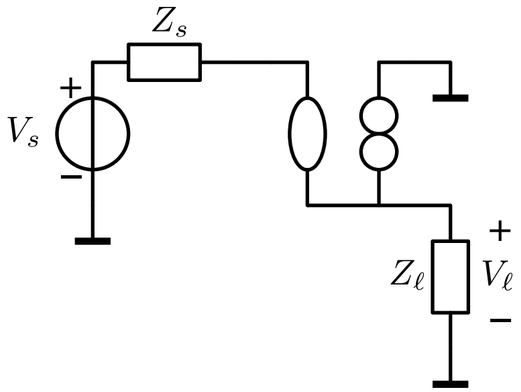

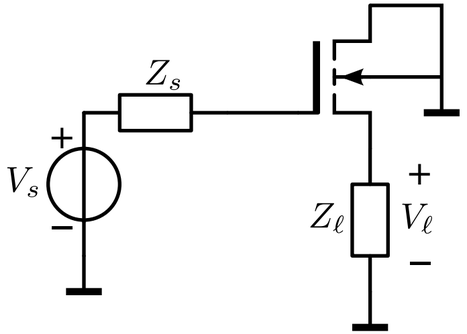

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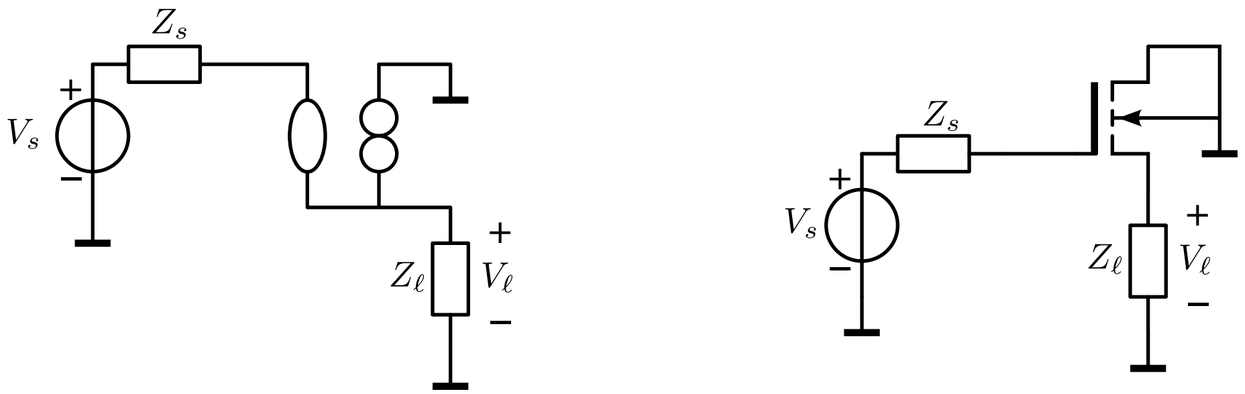

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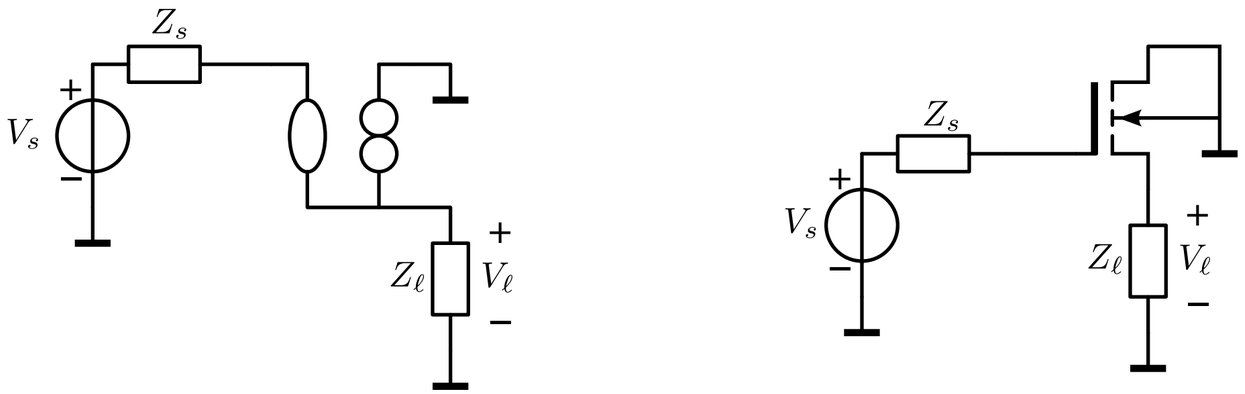

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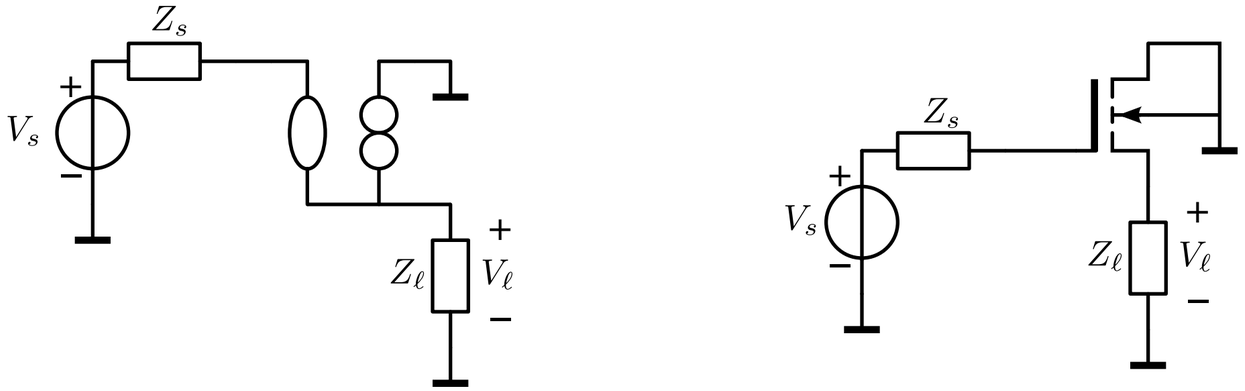

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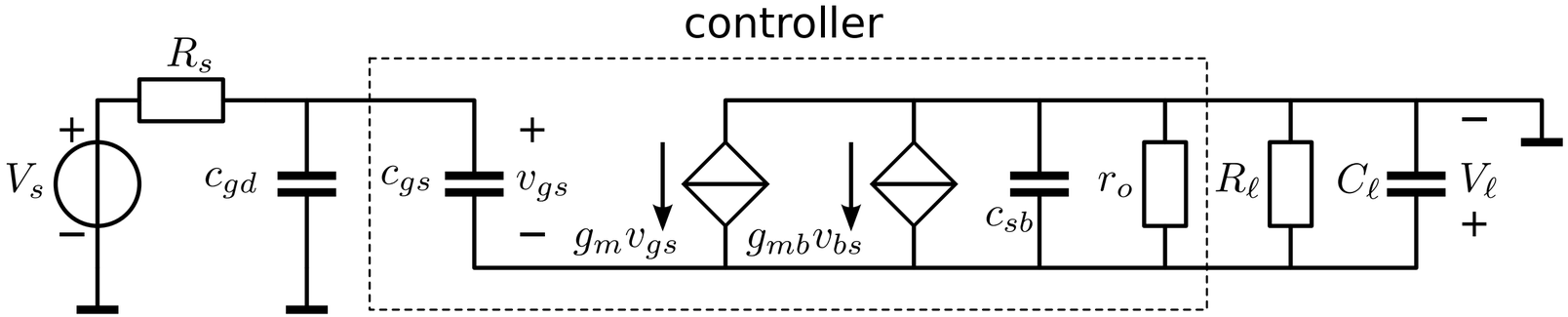

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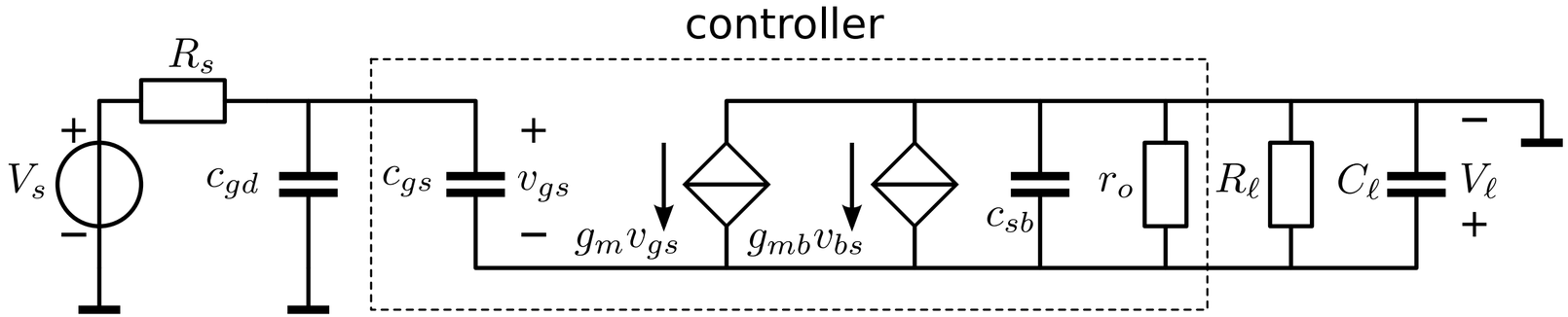

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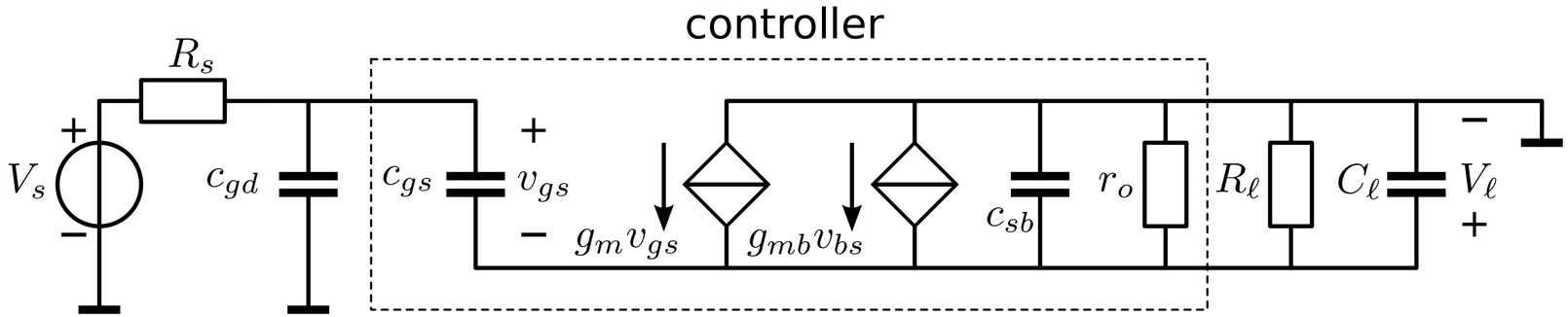

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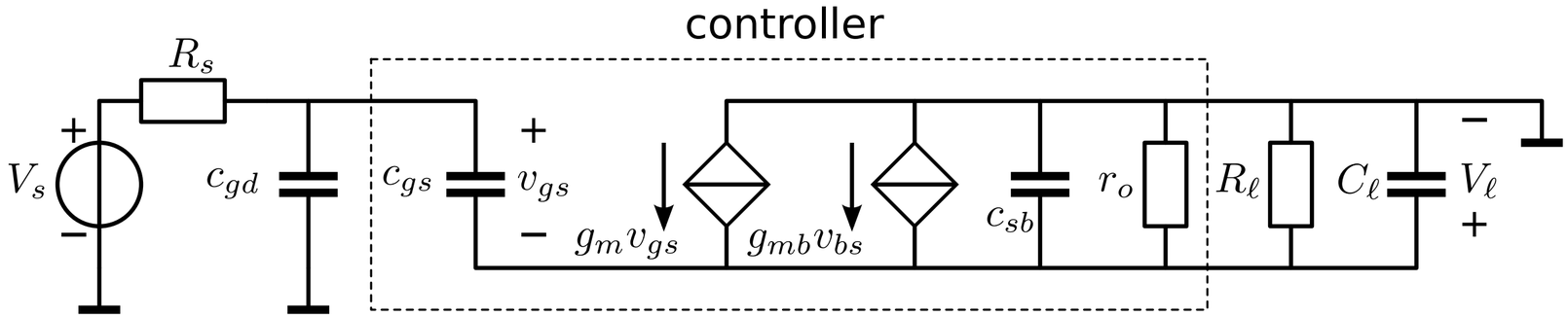

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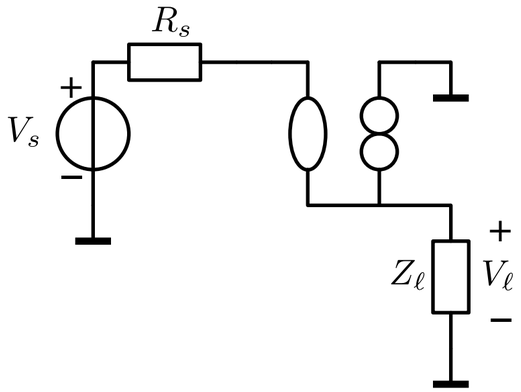

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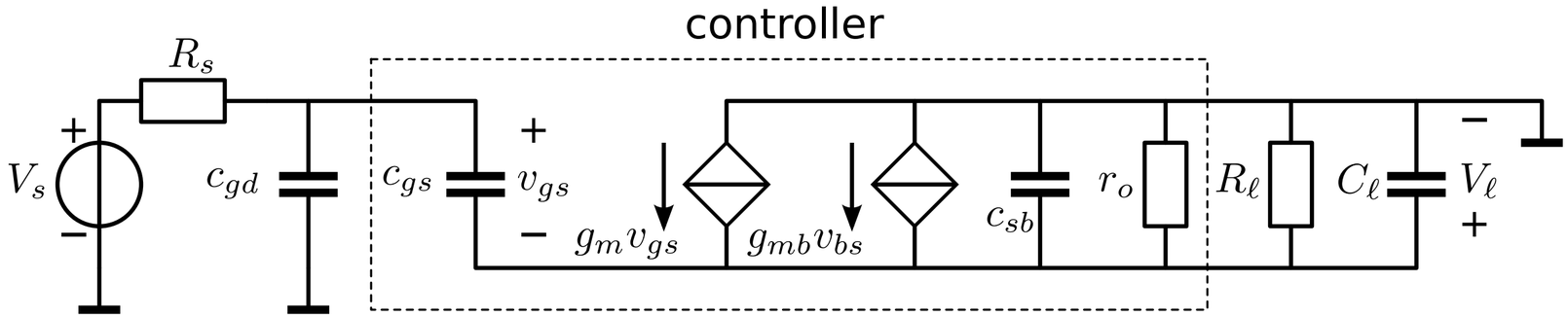

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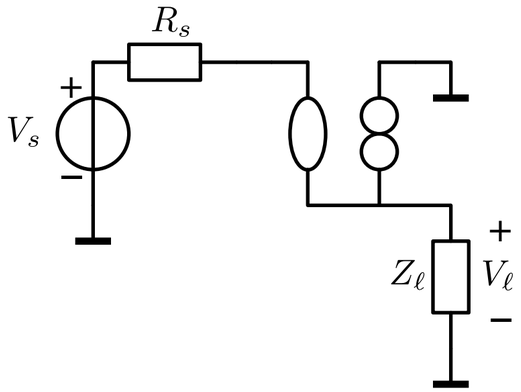

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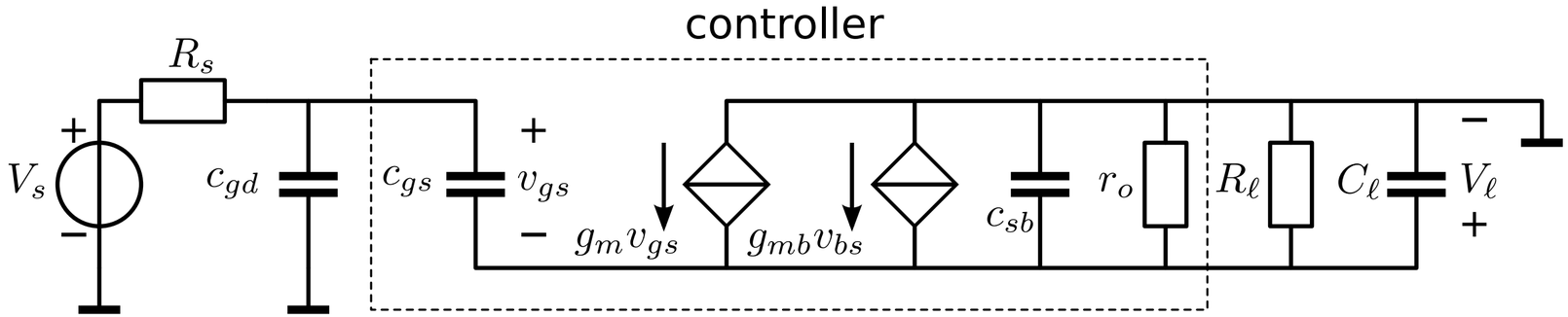

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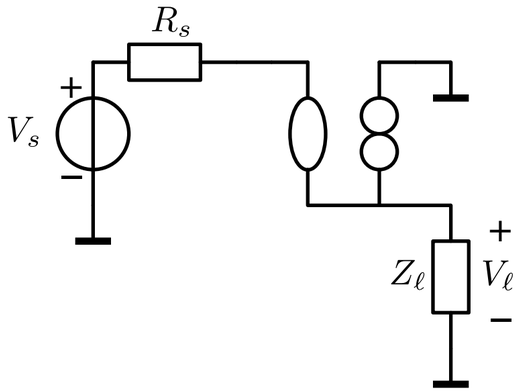

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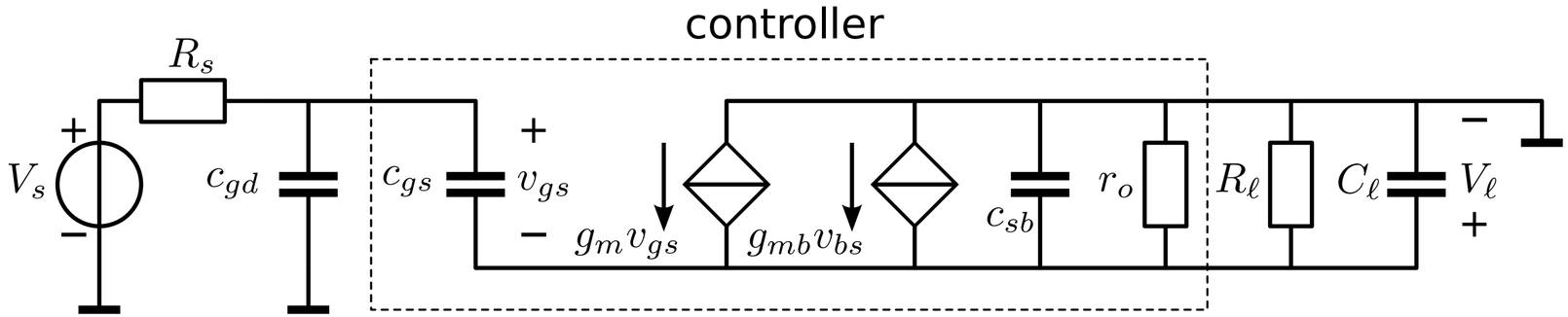

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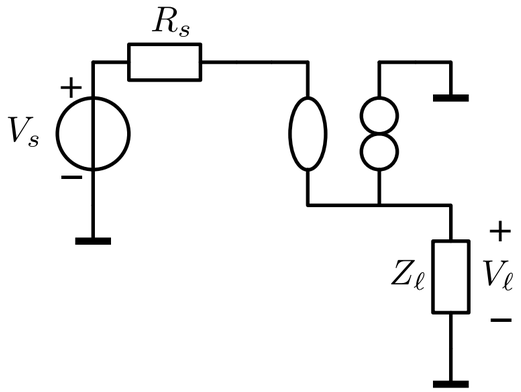

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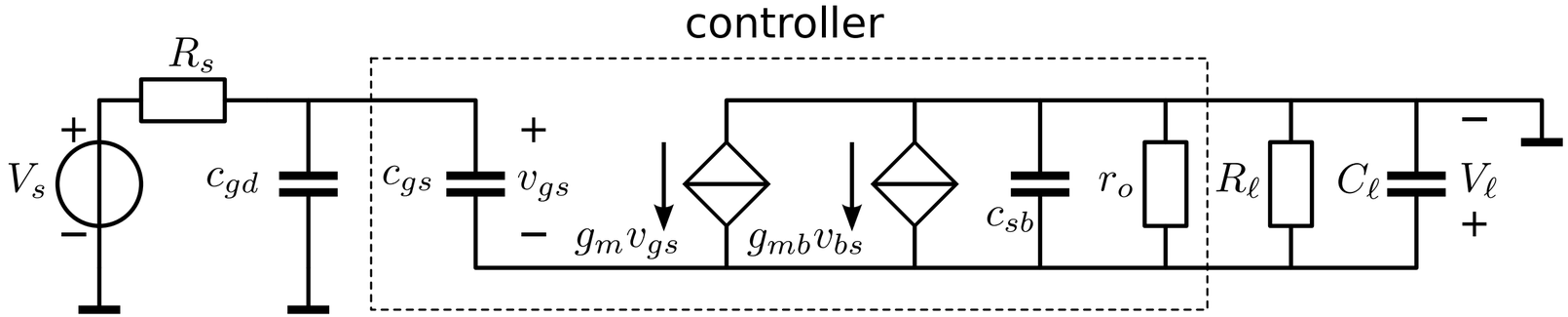

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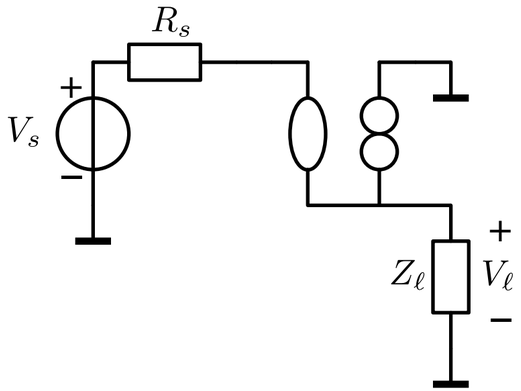

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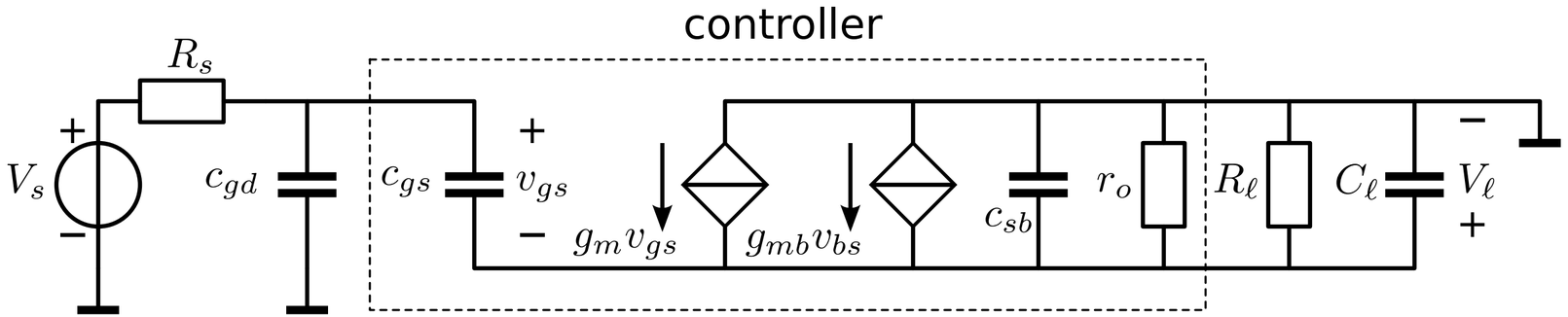

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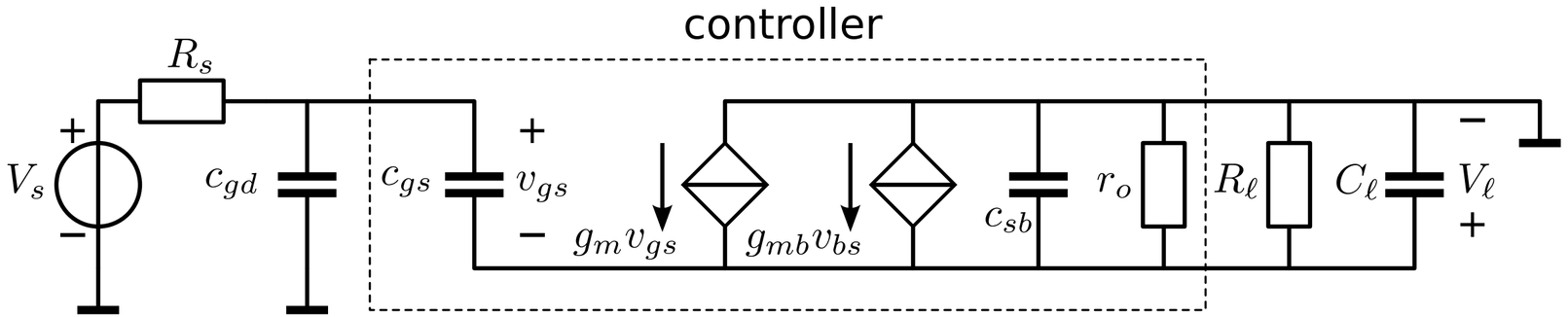

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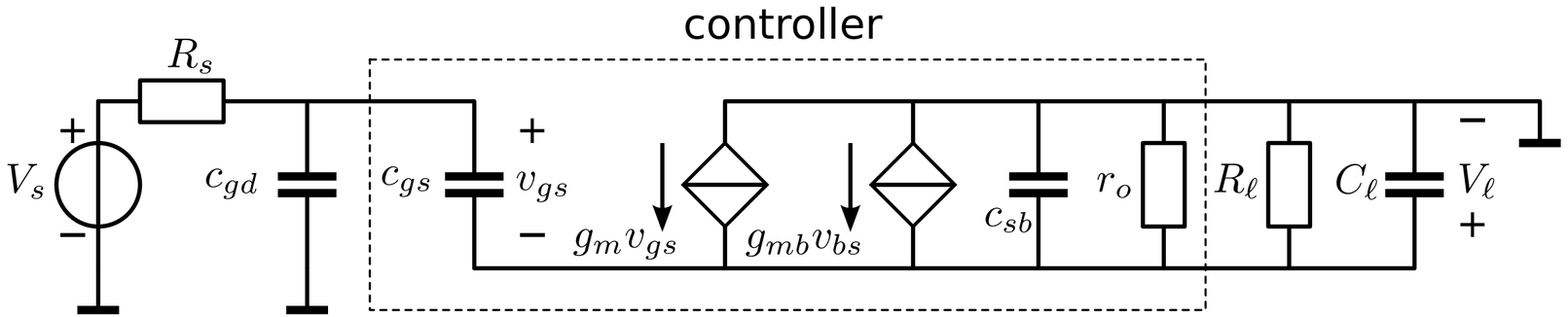

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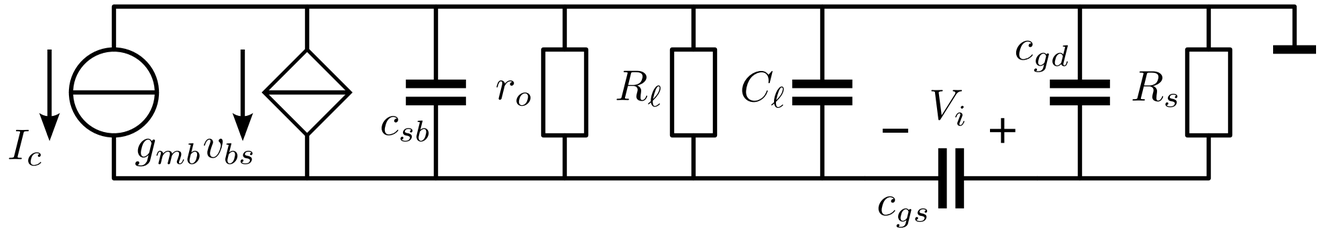

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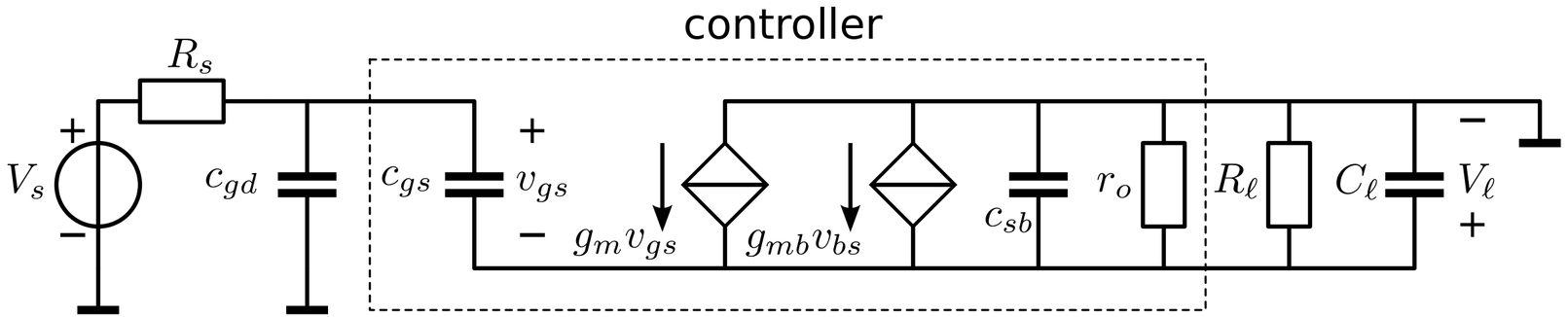

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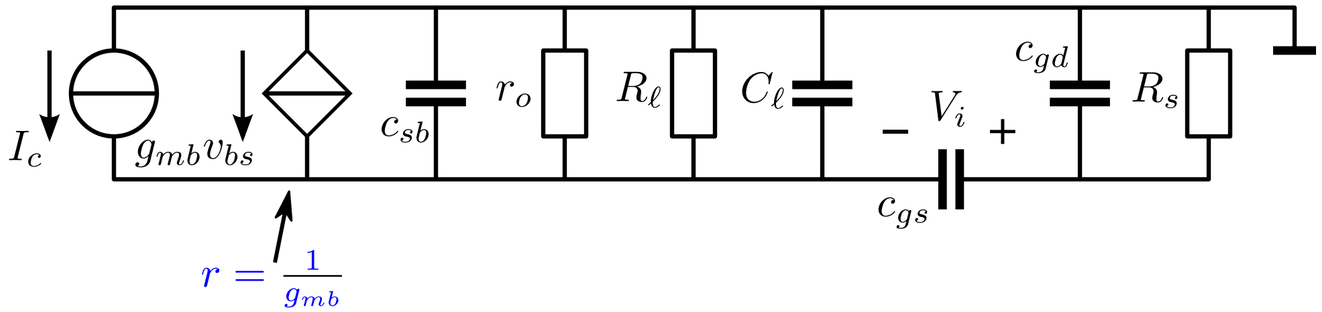

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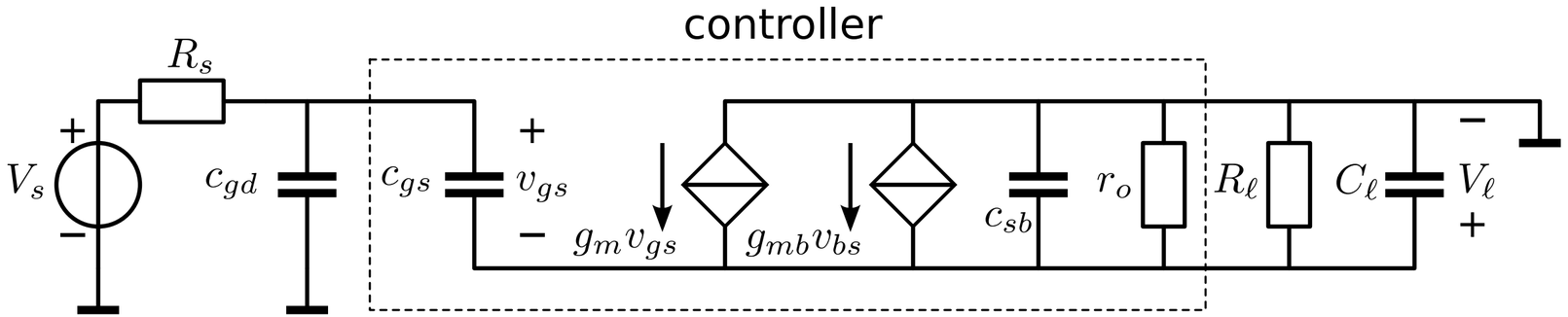

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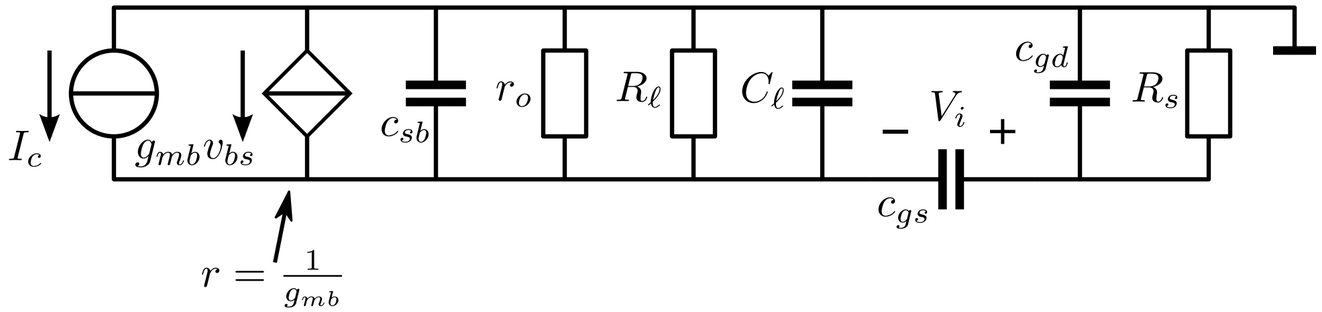
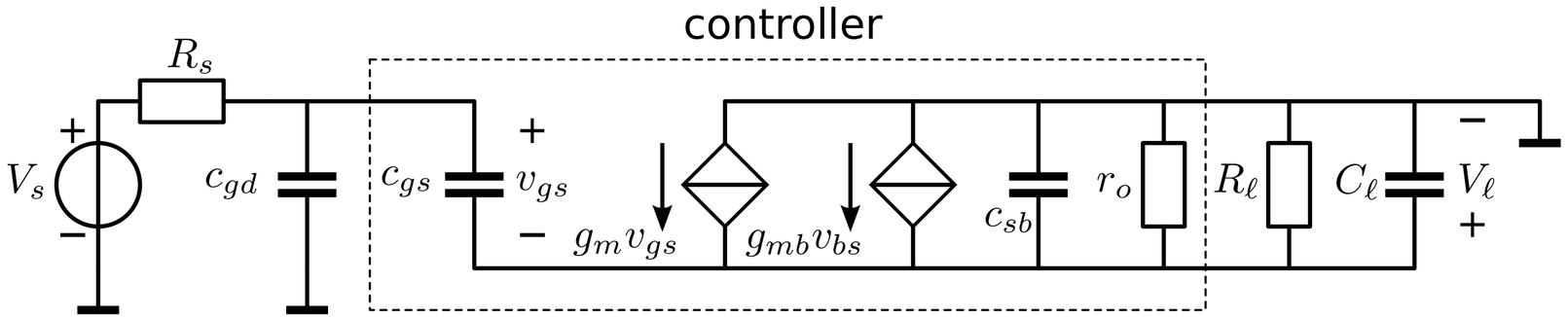


Simplified diagram:

CD stage: loop gain



Loop gain:

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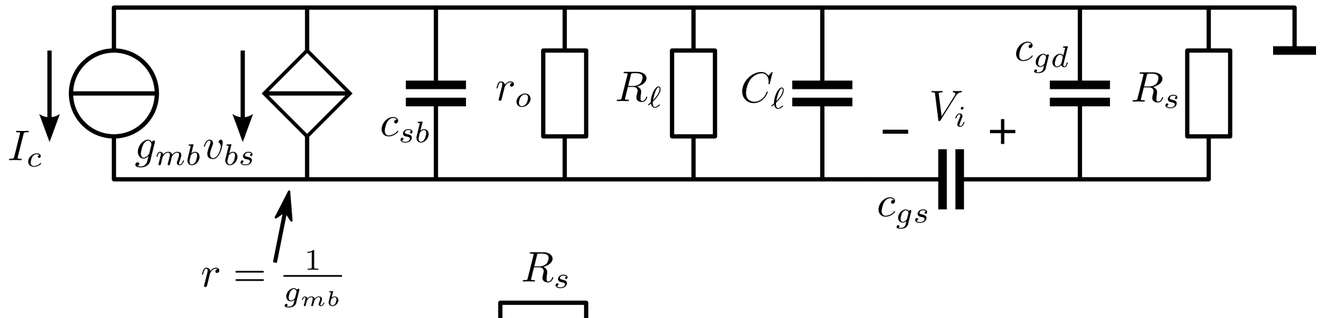
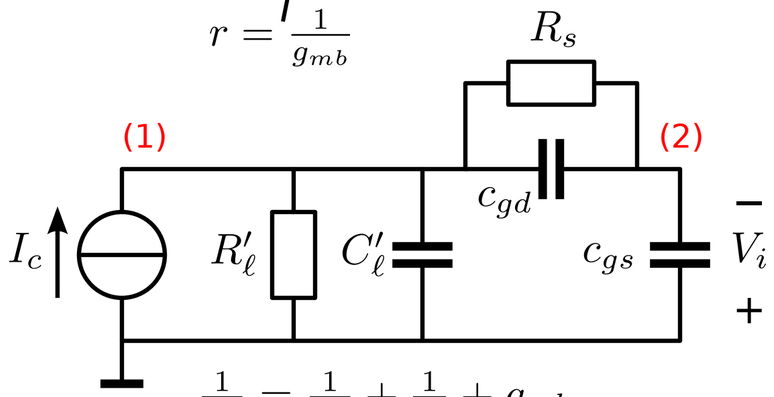


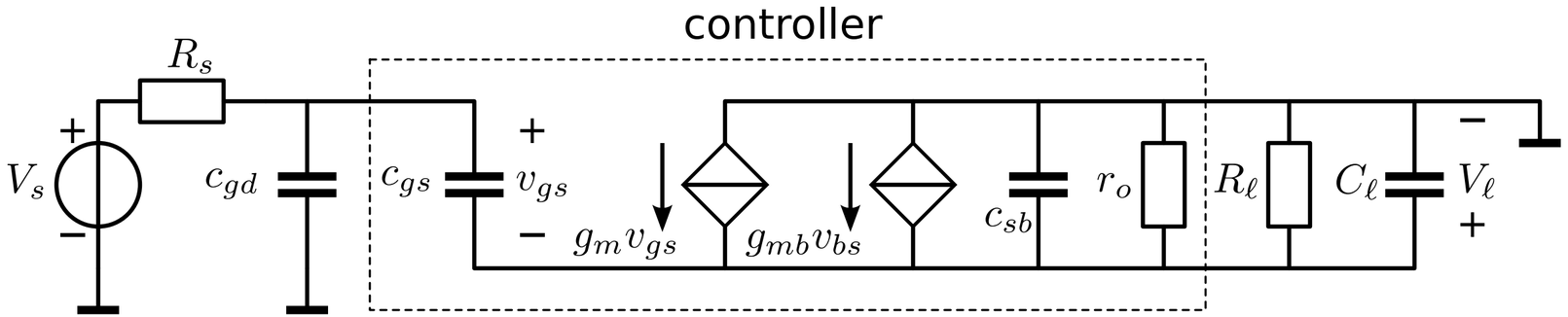
Simplified diagram:



$$\frac{1}{R'_\ell} = \frac{1}{R_\ell} + \frac{1}{r_o} + g_{mb}$$

$$C'_\ell = C_\ell + c_{sb}$$

CD stage: loop gain



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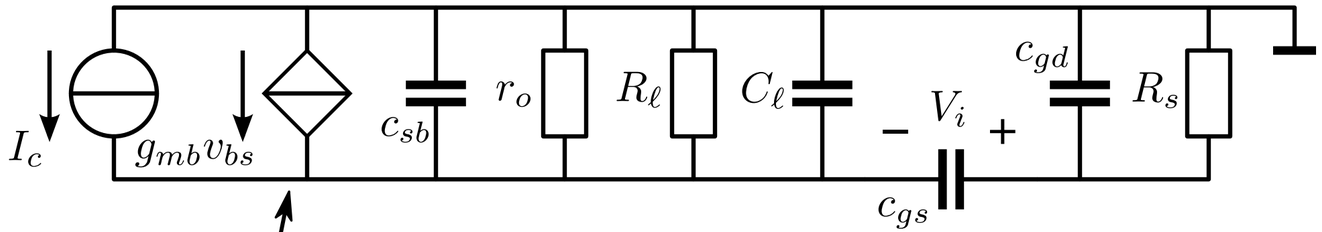
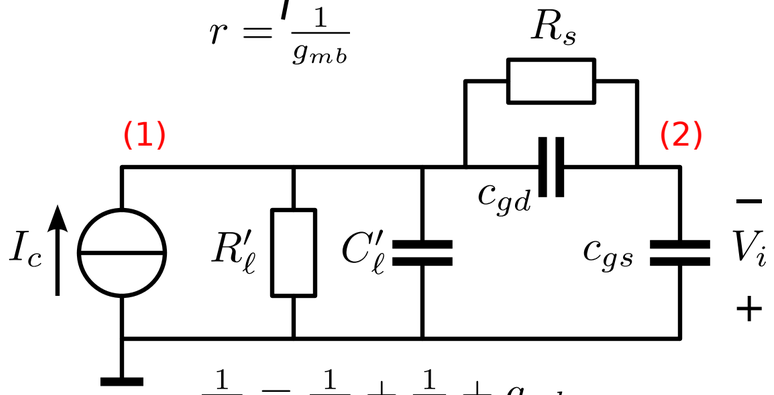


$$r = \frac{1}{g_{mb}}$$

Simplified diagram:

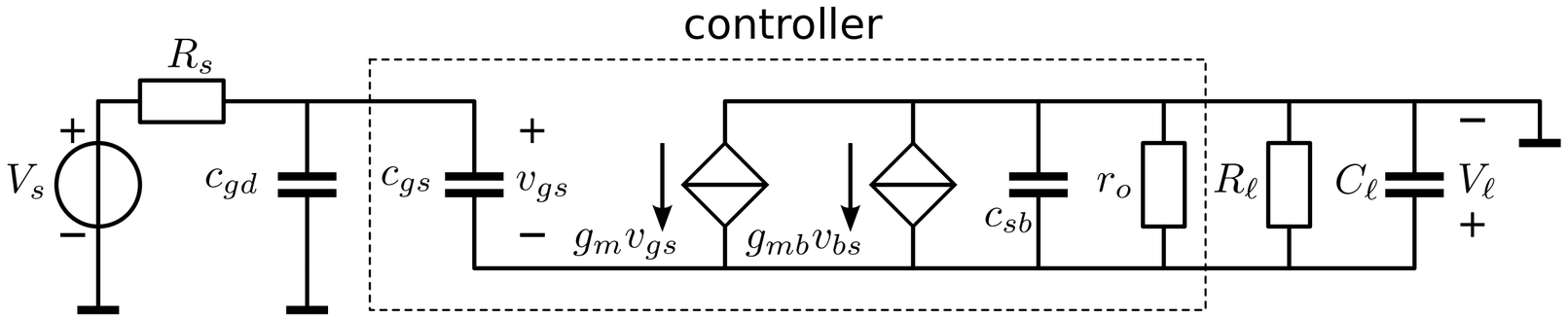


Loop gain drops if:

$$\frac{1}{R'_\ell} = \frac{1}{R_\ell} + \frac{1}{r_o} + g_{mb}$$

$$C'_\ell = C_\ell + c_{sb}$$

CD stage: loop gain



Loop gain:

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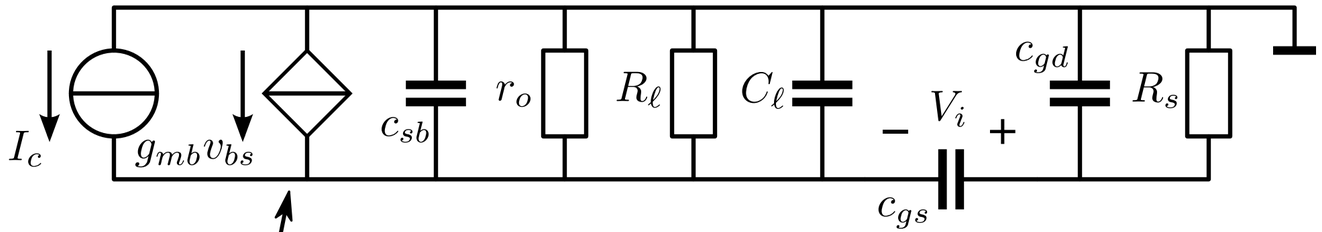
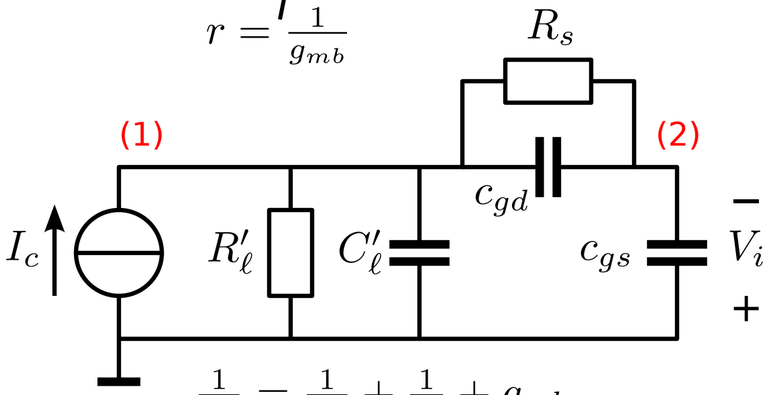


$$r = \frac{1}{g_{mb}}$$

Simplified diagram:

Loop gain drops if:

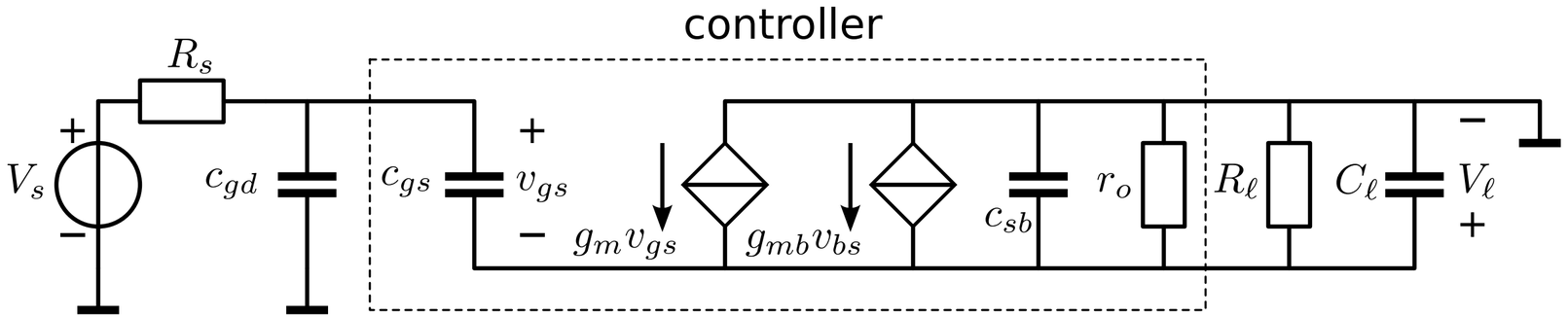
Load resistance decreases



$$\frac{1}{R'_\ell} = \frac{1}{R_\ell} + \frac{1}{r_o} + g_{mb}$$

$$C'_\ell = C_\ell + c_{sb}$$

CD stage: loop gain



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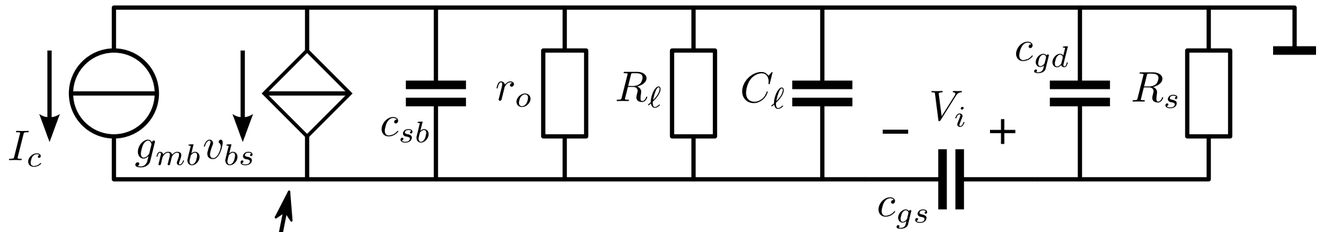
$$L = g_m \frac{V_i}{I_c}$$

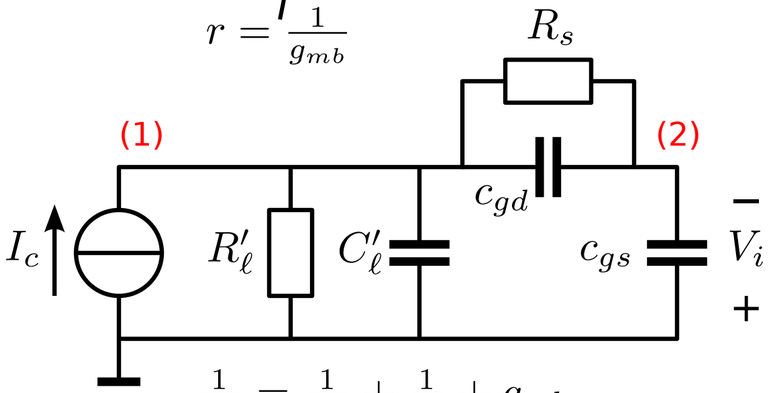


$$r = \frac{1}{g_{mb}}$$

Simplified diagram:

Loop gain drops if:

- Load resistance decreases
- Load capacitance increases



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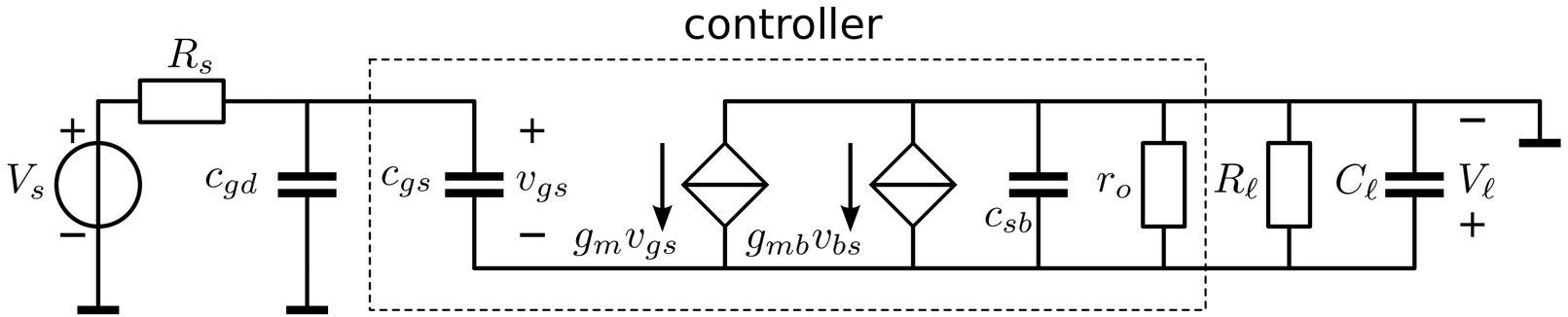
CD stage: loop gain



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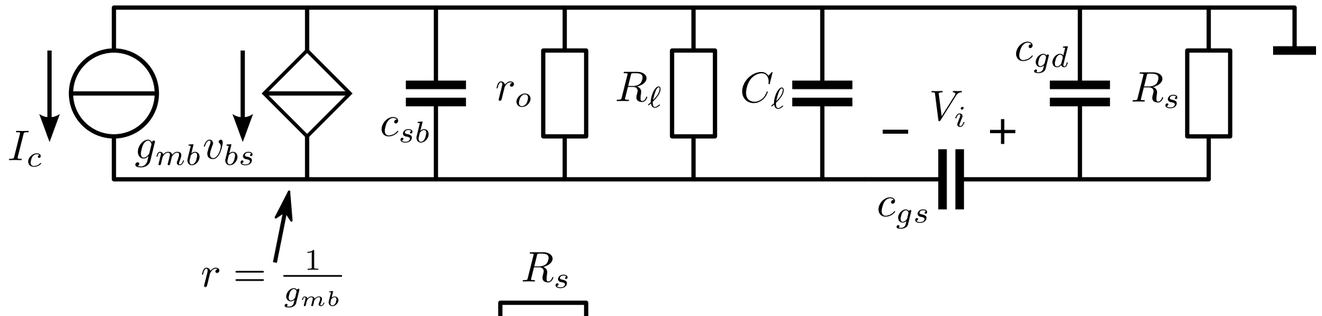
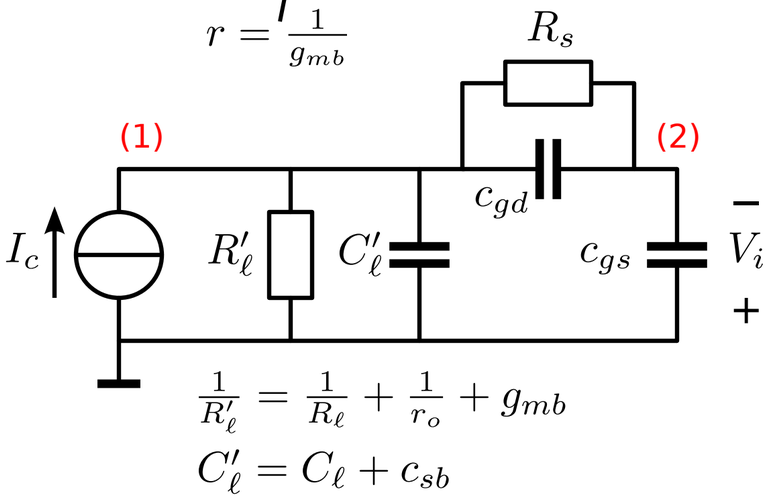


Simplified diagram:



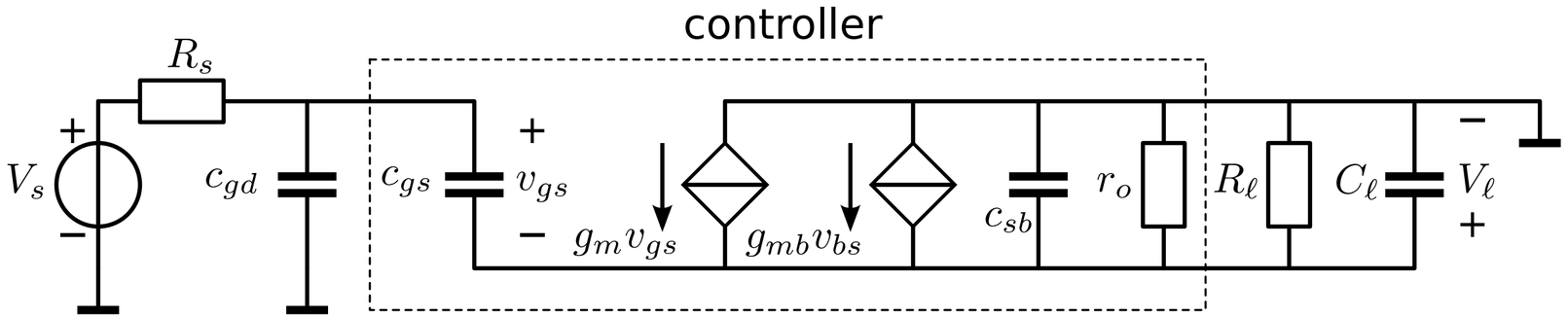
$$\frac{1}{R'_\ell} = \frac{1}{R_\ell} + \frac{1}{r_o} + g_{mb}$$

$$C'_\ell = C_\ell + c_{sb}$$

Loop gain drops if:

- Load resistance decreases
- Load capacitance increases
- Source resistance increases

CD stage: loop gain



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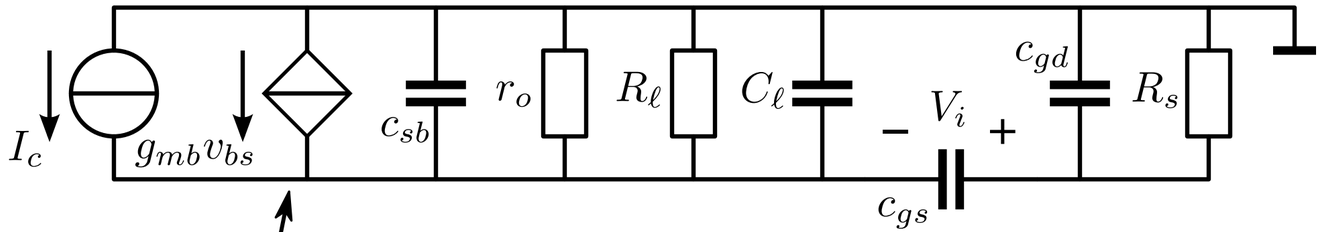
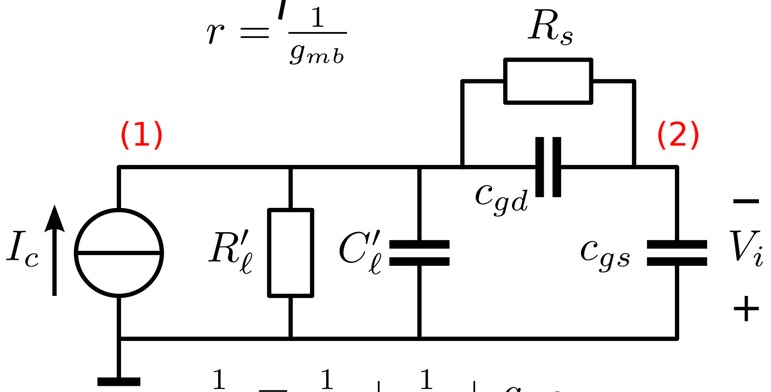


$$r = \frac{1}{g_{mb}}$$

Simplified diagram:



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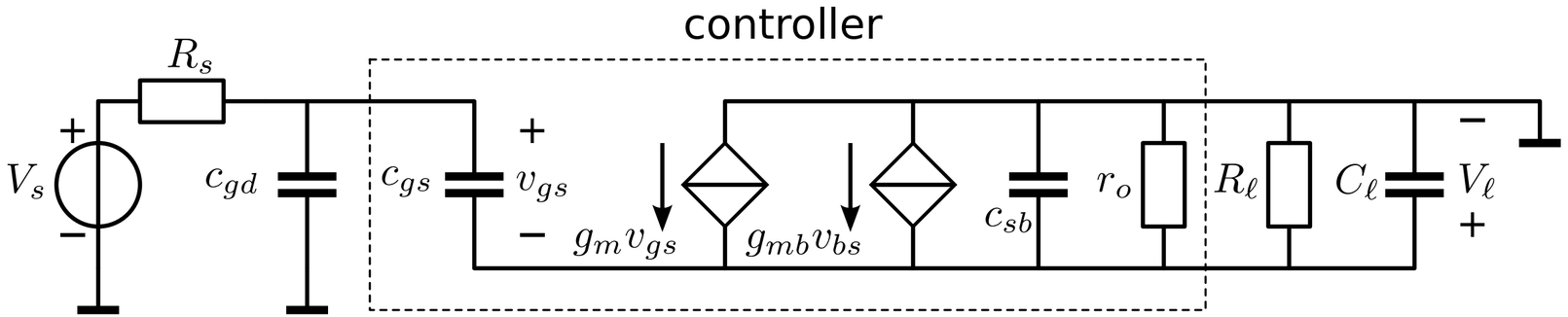
Loop gain drops if:

- Load resistance decreases
- Load capacitance increases
- Source resistance increases

Poll:
How many poles?
1: 1
2: 2
3: 3

Poll:
How many zeros?
1: 1
2: 2
3: 3

CD stage: loop gain



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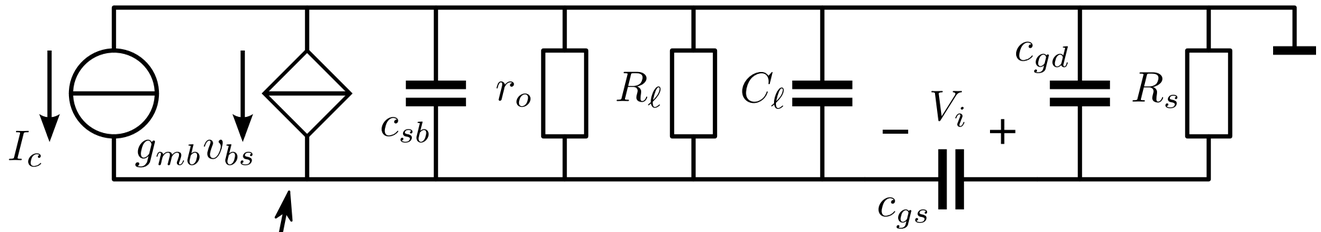

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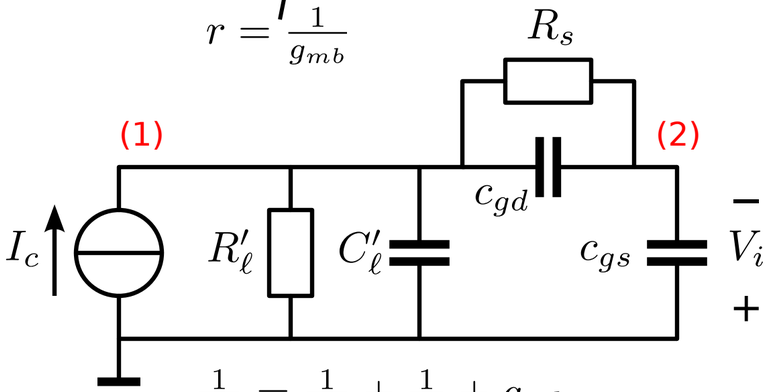

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How many zeros?
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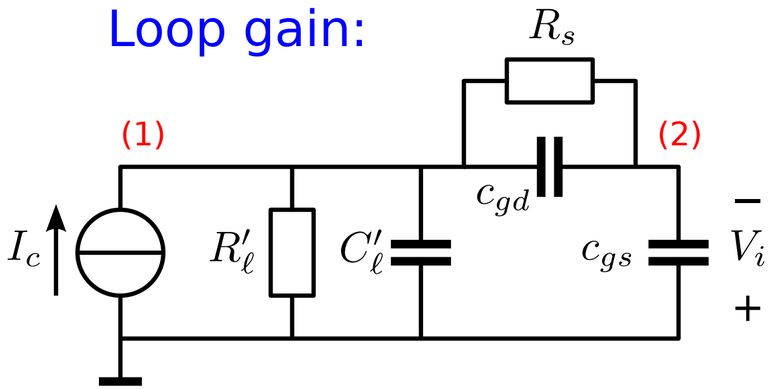
CD stage: bandwidth and stability

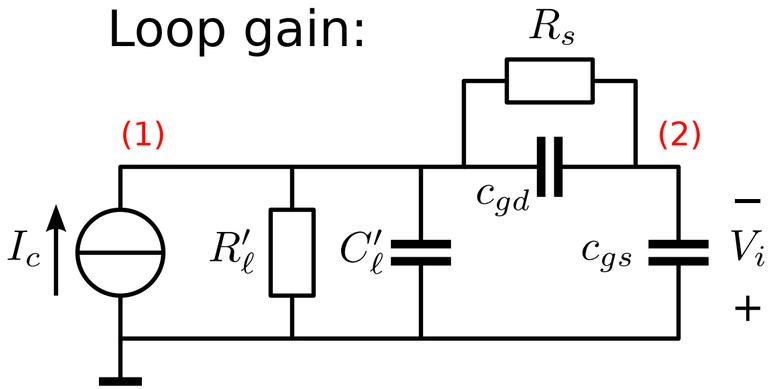
CD stage: bandwidth and stability

Loop gain:



CD stage: bandwidth and stability

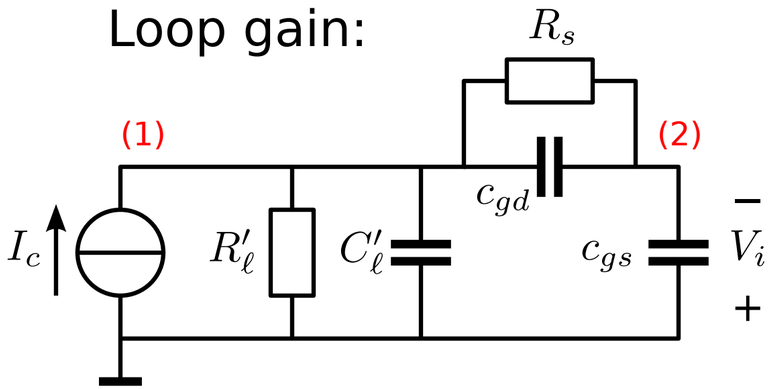
Loop gain:



$c_{gd} \ll c_{gs}$

CD stage: bandwidth and stability

Loop gain:



$c_{gd} \ll c_{gs}$

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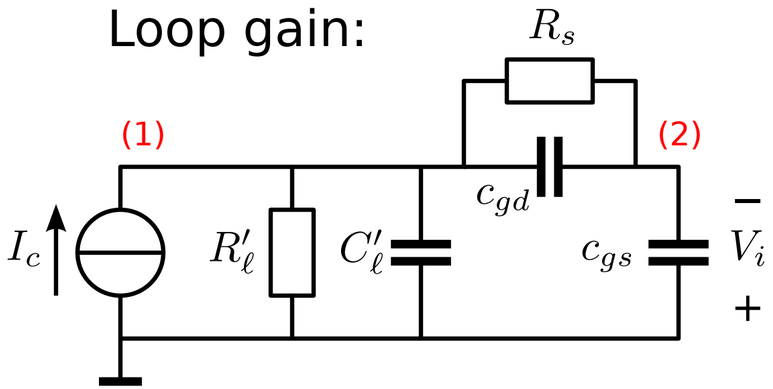
CD stage: bandwidth and stability

Loop gain:



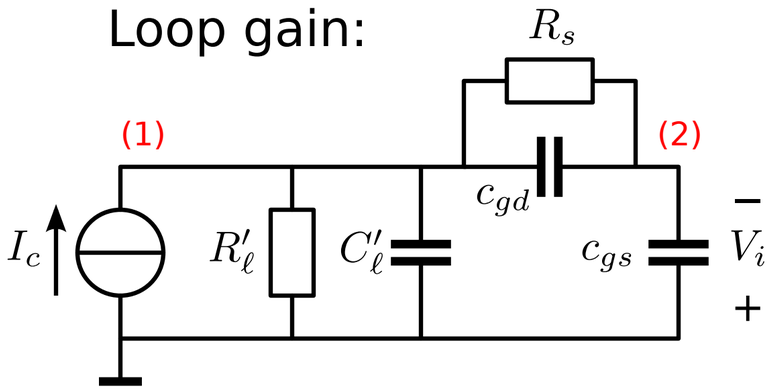
$c_{gd} \ll c_{gs}$

$c_{gd} \ll C'_\ell$

$L_{DC} = -g_m R'_\ell$

CD stage: bandwidth and stability

Loop gain:



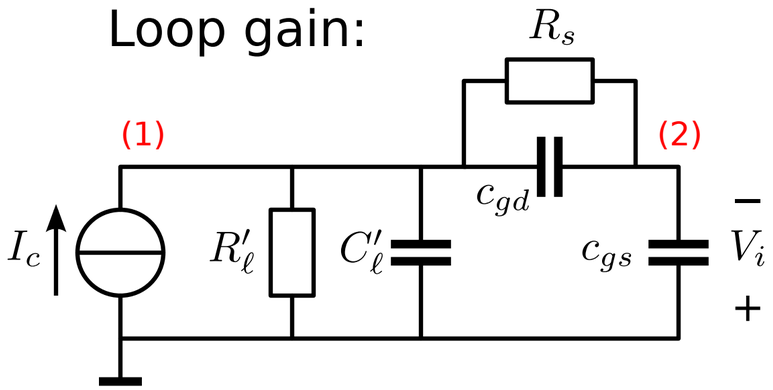
$c_{gd} \ll c_{gs}$

$c_{gd} \ll C'_\ell$

$L_{DC} = -g_m R'_\ell$ $\qquad$ $L_{DC\max} = -\frac{1}{n-1+\frac{1}{\mu}}$

CD stage: bandwidth and stability

Loop gain:



$c_{gd} \ll c_{gs}$

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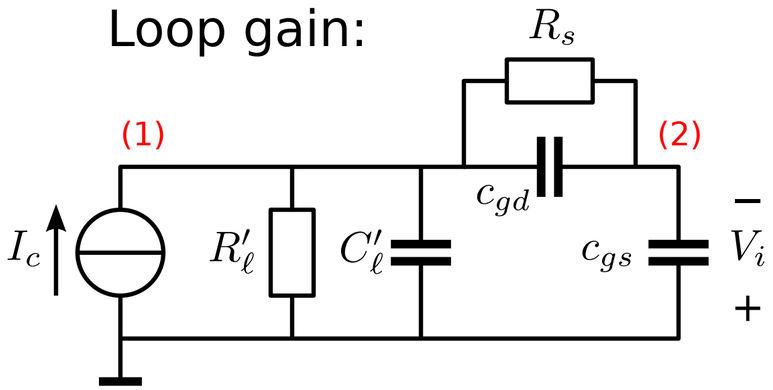
Two poles

CD stage: bandwidth and stability

Loop gain:



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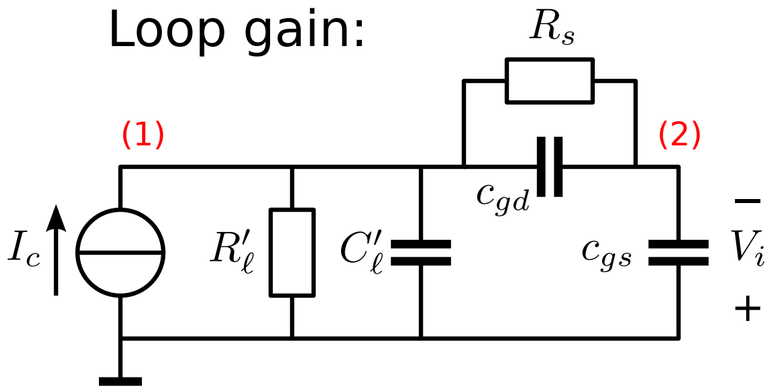
Two poles

Bandwidth follows from LP product (dominant poles only)

CD stage: bandwidth and stability

Loop gain:



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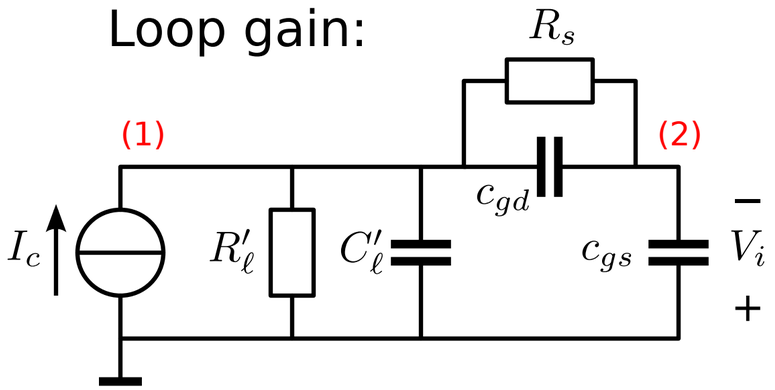
Two poles

Bandwidth follows from LP product (dominant poles only)

Two dominant poles: peaking or instability possible

CD stage: bandwidth and stability

Loop gain:



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Two poles

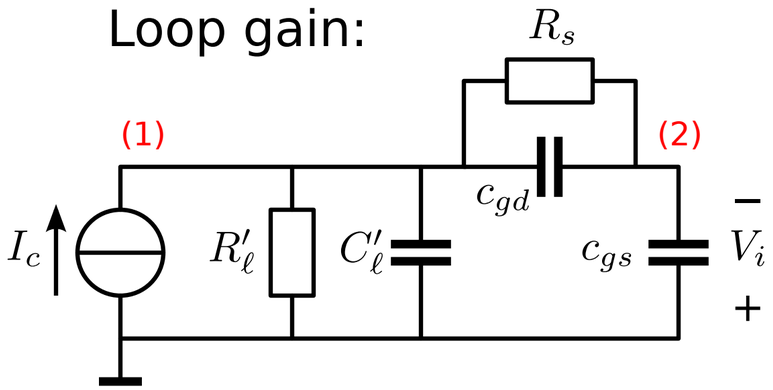
Bandwidth follows from LP product (dominant poles only)

Two dominant poles: peaking or instability possible

c_{gd} estabishes a phantom zero
frequency can be changed (reduced) with external capacitor

CD stage: bandwidth and stability

Loop gain:



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Two poles

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CD stage: SLiCAP example

Phantom zero compensation of a capacitively loaded CS stage