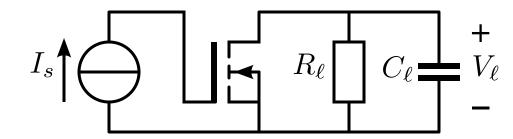
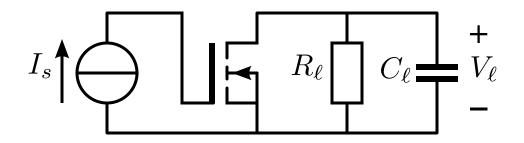
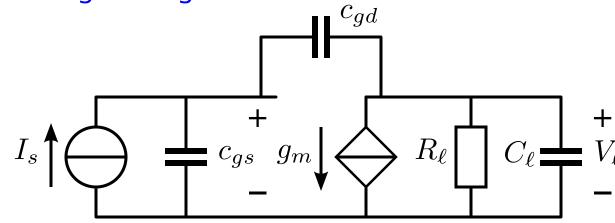
Structured Electronic Design Pole-splitting (Miller effect) and Cascode Stages

Biased, current-driven CS-stage with RC load

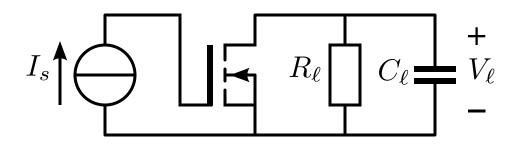


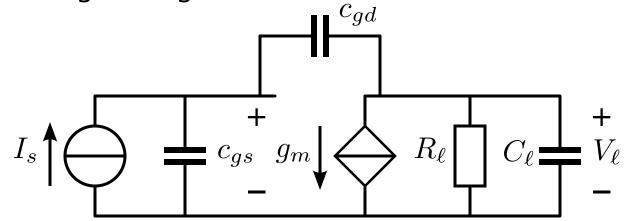
Biased, current-driven CS-stage with RC load

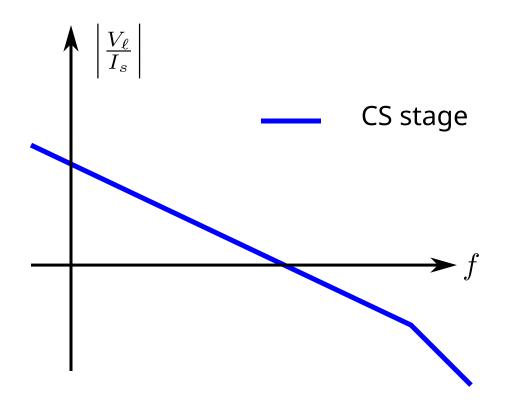




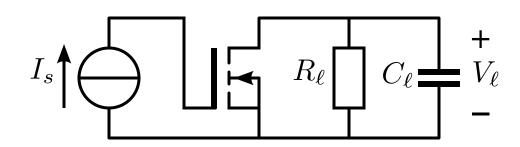
Biased, current-driven CS-stage with RC load



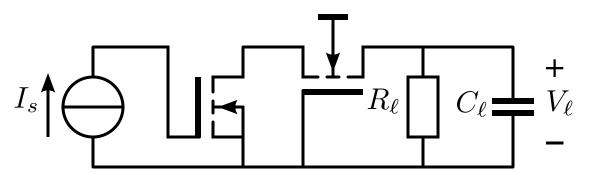


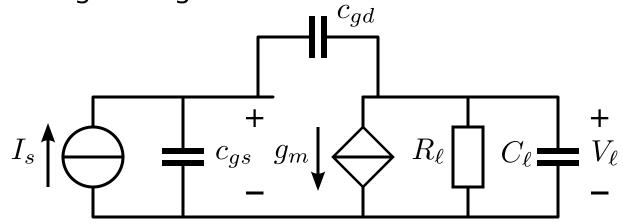


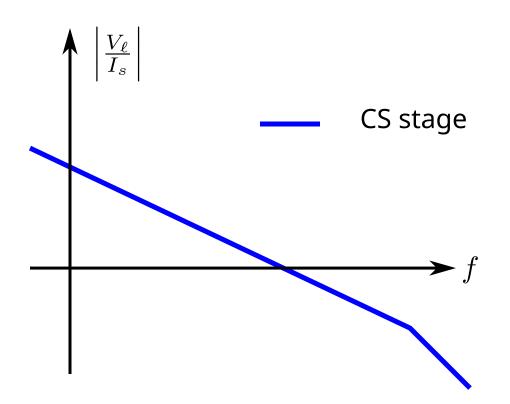
Biased, current-driven CS-stage with RC load



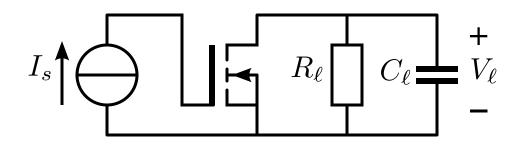
Biased, current-driven cascode stage with RC load



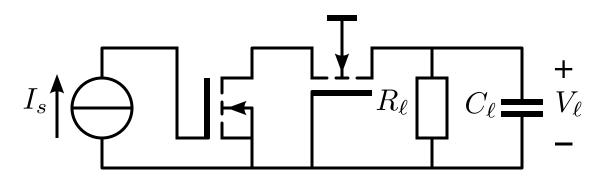




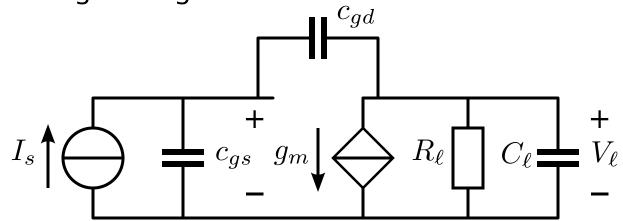
Biased, current-driven CS-stage with RC load

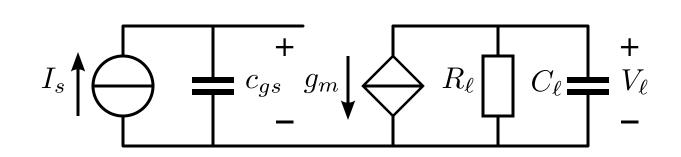


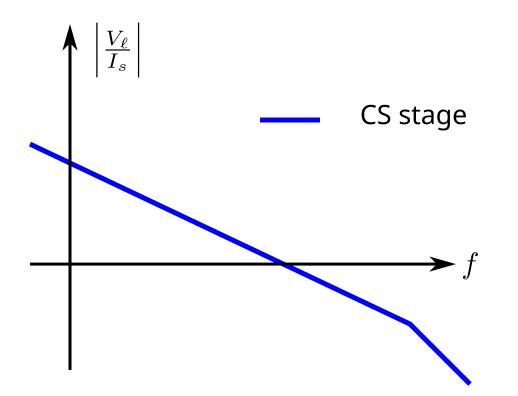
Biased, current-driven cascode stage with RC load



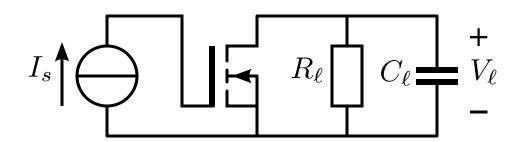
Small-signal diagram



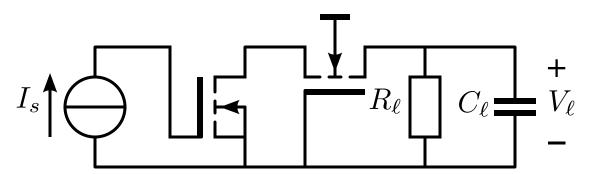




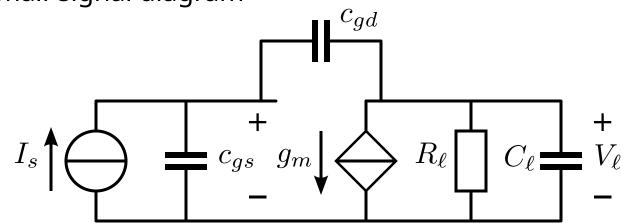
Biased, current-driven CS-stage with RC load

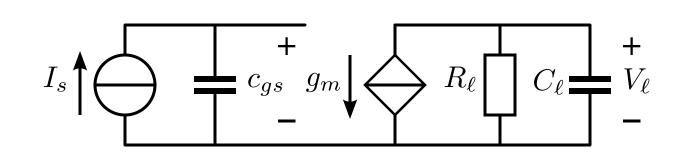


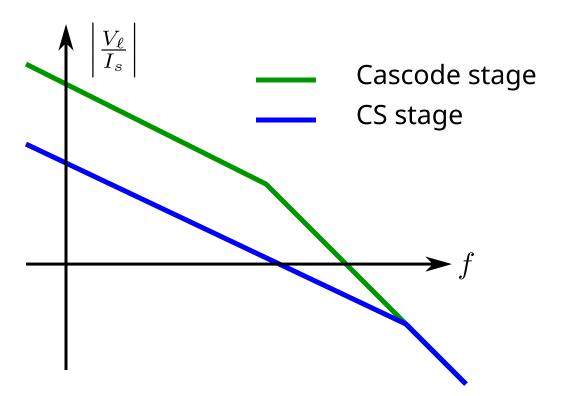
Biased, current-driven cascode stage with RC load



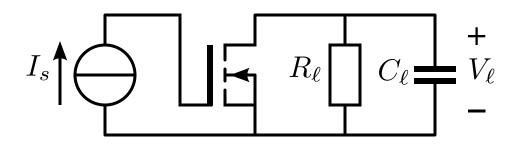
Small-signal diagram



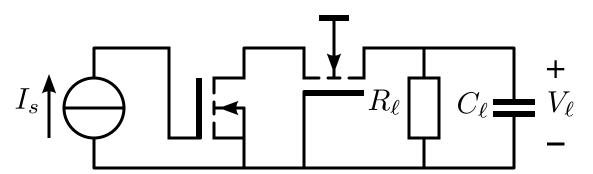




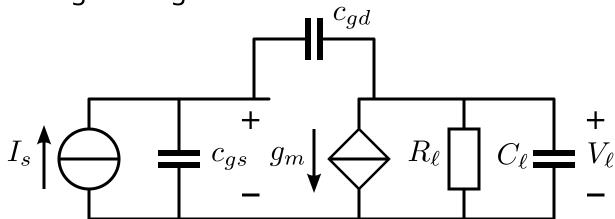
Biased, current-driven CS-stage with RC load



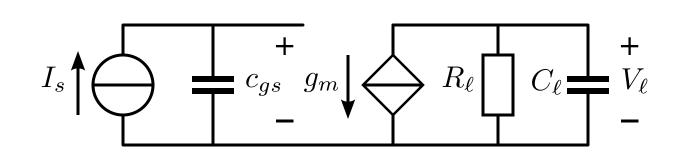
Biased, current-driven cascode stage with RC load



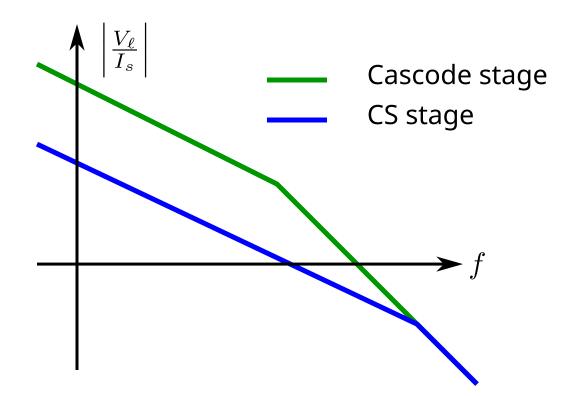
Small-signal diagram



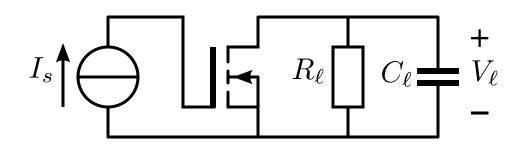
Small-signal diagram



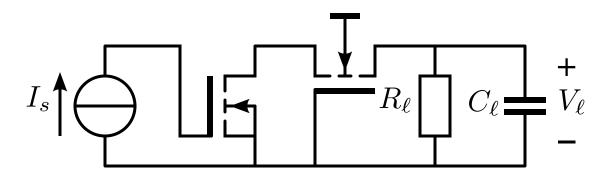
c_{qs} increases the sum of the poles: pole-splitting



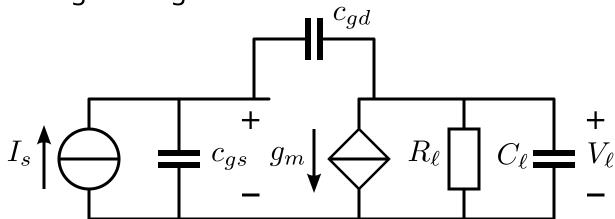
Biased, current-driven CS-stage with RC load



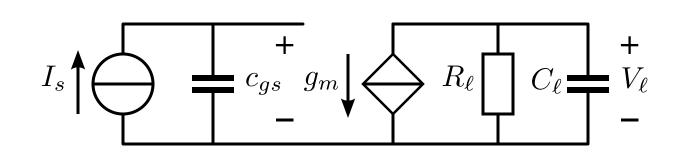
Biased, current-driven cascode stage with RC load



Small-signal diagram

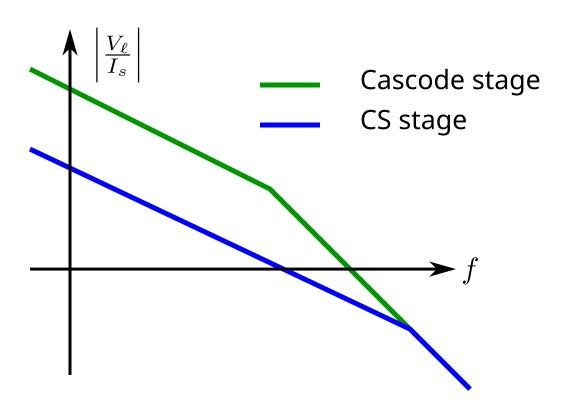


Small-signal diagram

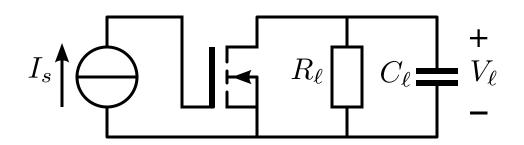


c_{gs} increases the sum of the poles: pole-splitting

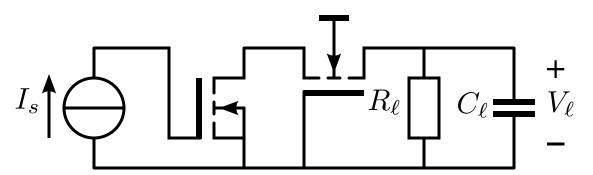
occurs if: $g_m R_\ell \gg 1$



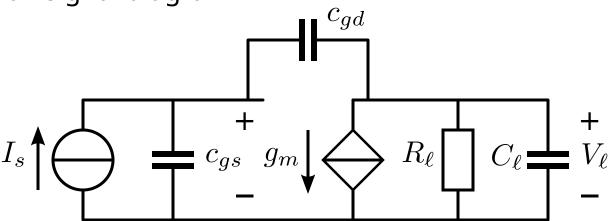
Biased, current-driven CS-stage with RC load



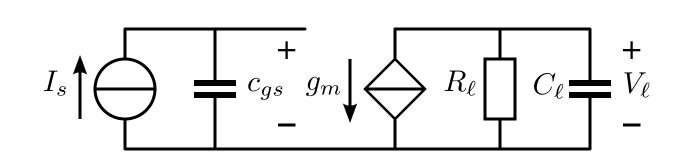
Biased, current-driven cascode stage with RC load



Small-signal diagram



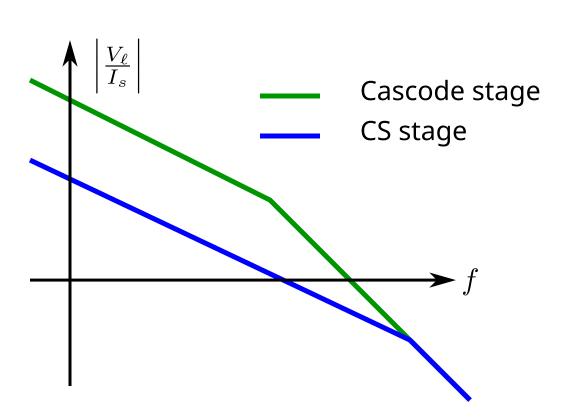
Small-signal diagram



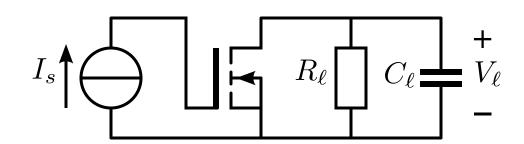
 c_{gs} increases the sum of the poles: pole-splitting

occurs if: $g_m R_\ell \gg 1$

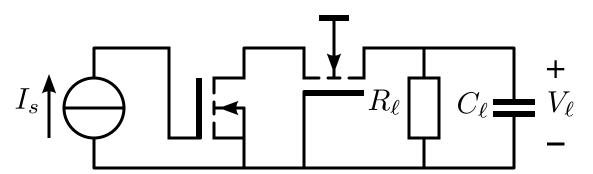
product of the poles not affected by c_{gd} if $c_{gd} \ll c_{gs}$ and $c_{gd} \ll C_{\ell}$



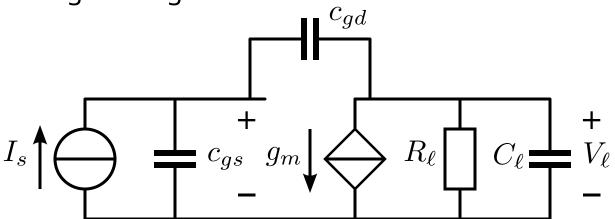
Biased, current-driven CS-stage with RC load



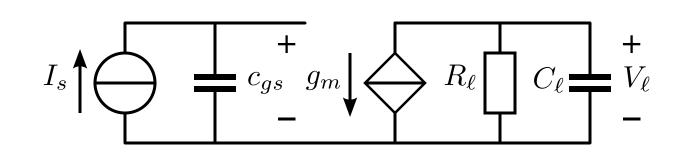
Biased, current-driven cascode stage with RC load



Small-signal diagram



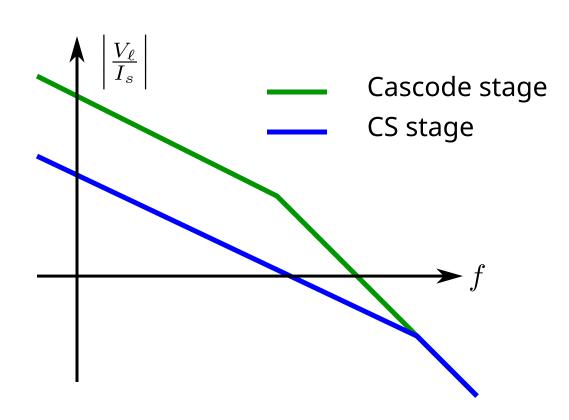
Small-signal diagram



 c_{gs} increases the sum of the poles: pole-splitting

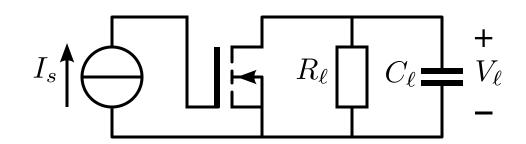
occurs if:
$$g_m R_\ell \gg 1$$

product of the poles not affected by ${\it c}_{\rm gd}$ if $c_{gd}\ll c_{gs}$ and $c_{gd}\ll C_{\ell}$

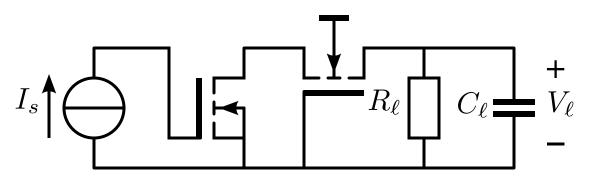


Cascode stage is considered a single stage

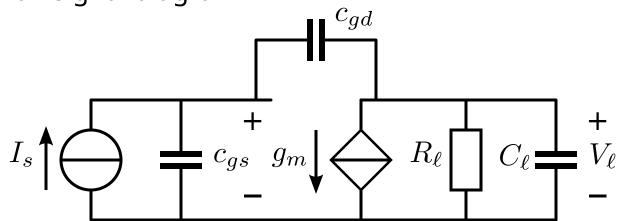
Biased, current-driven CS-stage with RC load



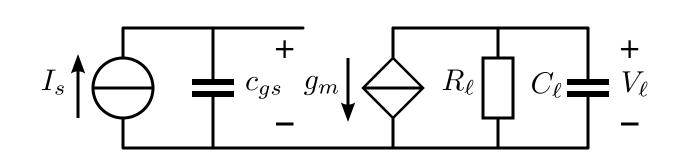
Biased, current-driven cascode stage with RC load



Small-signal diagram



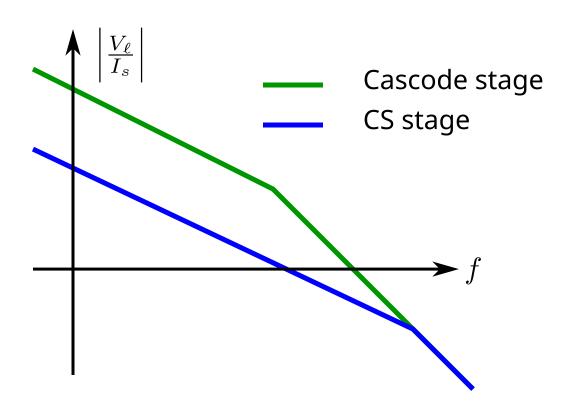
Small-signal diagram



 c_{gs} increases the sum of the poles: pole-splitting

occurs if: $g_m R_\ell \gg 1$

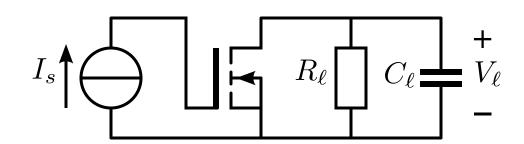
product of the poles not affected by ${\it c}_{\rm gd}$ if $c_{gd}\ll c_{gs}$ and $c_{gd}\ll C_{\ell}$



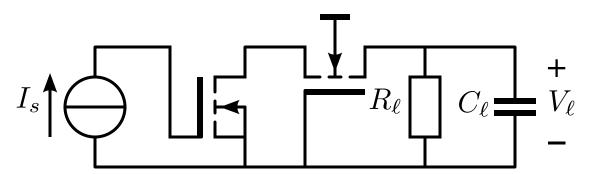
Cascode stage is considered a single stage

CG stage contributes a (non dominant) pole at f_T and unity current gain

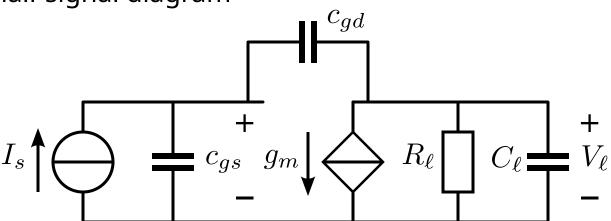
Biased, current-driven CS-stage with RC load



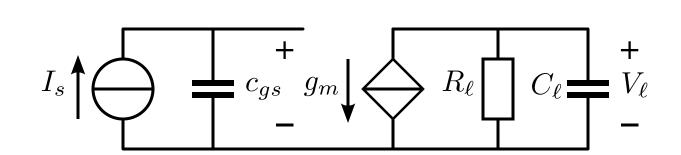
Biased, current-driven cascode stage with RC load



Small-signal diagram



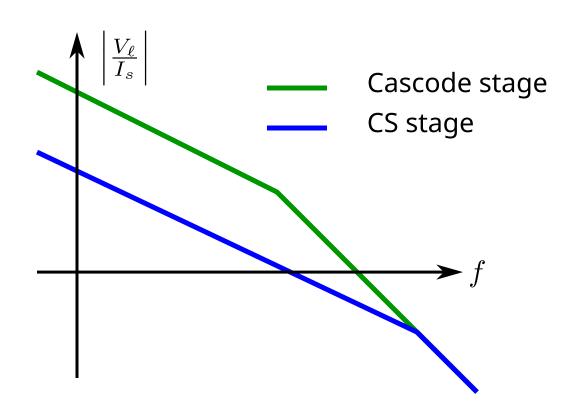
Small-signal diagram



 c_{gs} increases the sum of the poles: pole-splitting

occurs if: $g_m R_\ell \gg 1$

product of the poles not affected by c_{gd} if $c_{gd} \ll c_{gs}$ and $c_{gd} \ll C_{\ell}$

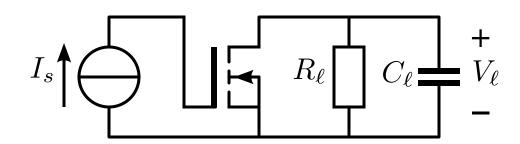


Cascode stage is considered a single stage

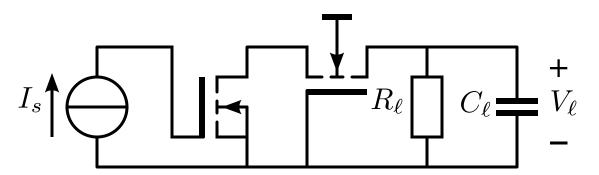
CG stage contributes a (non dominant) pole at f_T and unity current gain

Uni-lateral stage

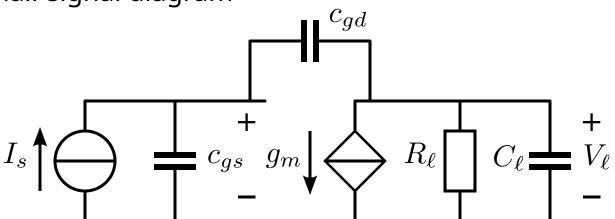
Biased, current-driven CS-stage with RC load



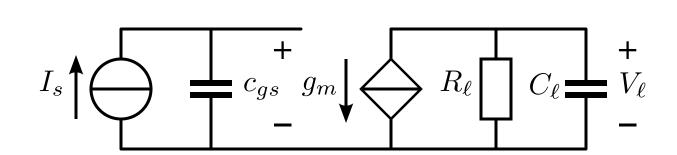
Biased, current-driven cascode stage with RC load



Small-signal diagram



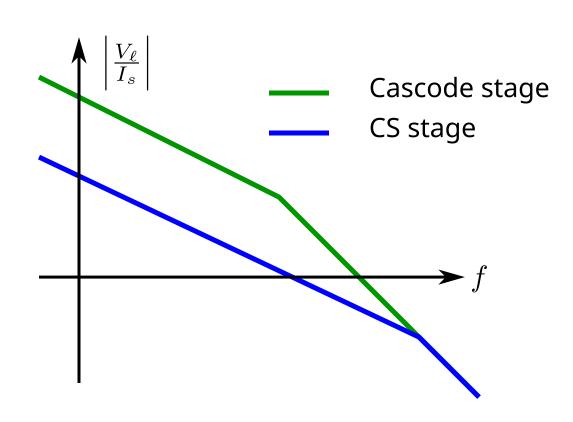
Small-signal diagram



c_{gs} increases the sum of the poles: pole-splitting

occurs if: $g_m R_\ell \gg 1$

product of the poles not affected by ${\it c}_{\rm gd}$ if $c_{gd}\ll c_{gs}$ and $c_{gd}\ll C_{\ell}$



Cascode stage is considered a single stage

CG stage contributes a (non dominant) pole at f_T and unity current gain

Uni-lateral stage

Structured Electronic Design Pole-splitting (Miller effect) and Cascode Stages