Structured Electronic Design

EE4109
Poll: Principle of Amplification and Biasing

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The figure above shows a biased transistor stage with a signal source \((V_s\) and \(R_s\)) and a load resistor with a resistance \(R_l\).

The values \(I_{GS}\) and \(V_{GS}\) of the input bias sources have been assigned such that the zero-signal drain-source current equals \(I_{DS}\) equals 100\(\mu\)A and the zero-signal drain-source voltage \(V_{DS}\) equals 0.9V.
The figure above shows a biased transistor stage with a signal source ($V_s$ and $R_s$) and a load resistor with a resistance $R_\ell$.

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