Structured Electronic Design

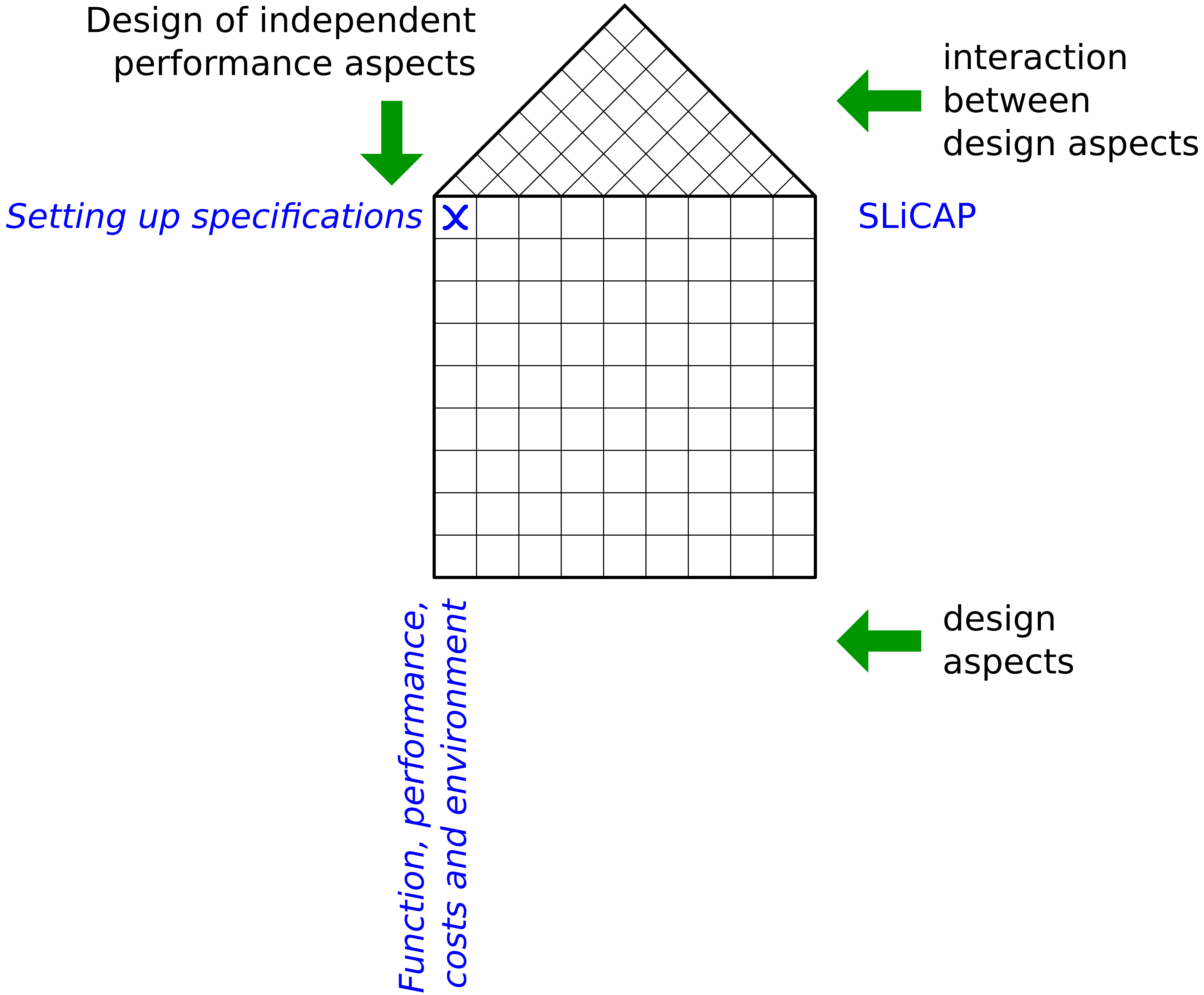
Design of application-specific
negative feedback amplifiers
in CMOS technology
(recap)

Anton J.M. Montagne

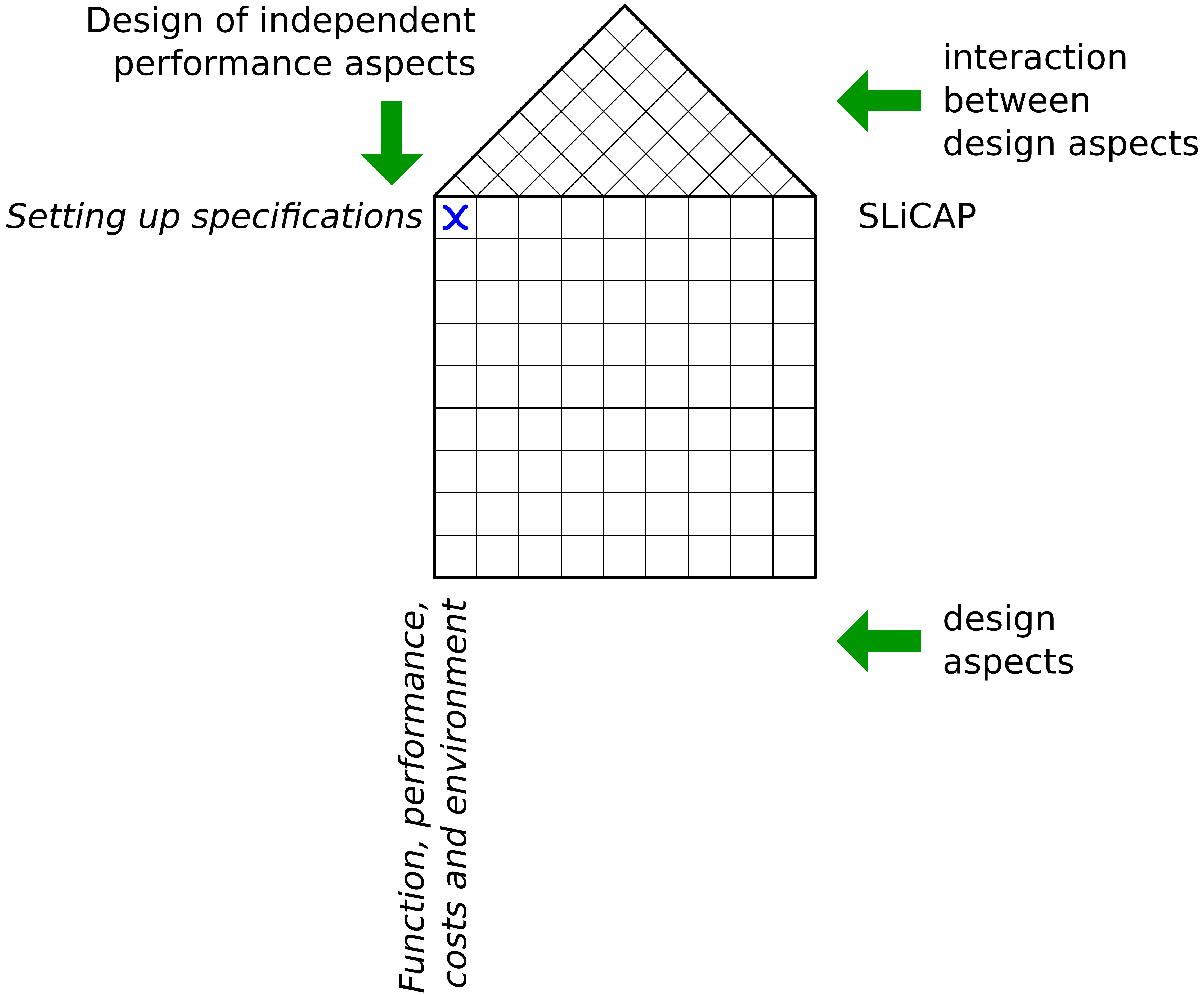
Structured Electronic Design

Step 1
Setting up the specification

Anton J.M. Montagne

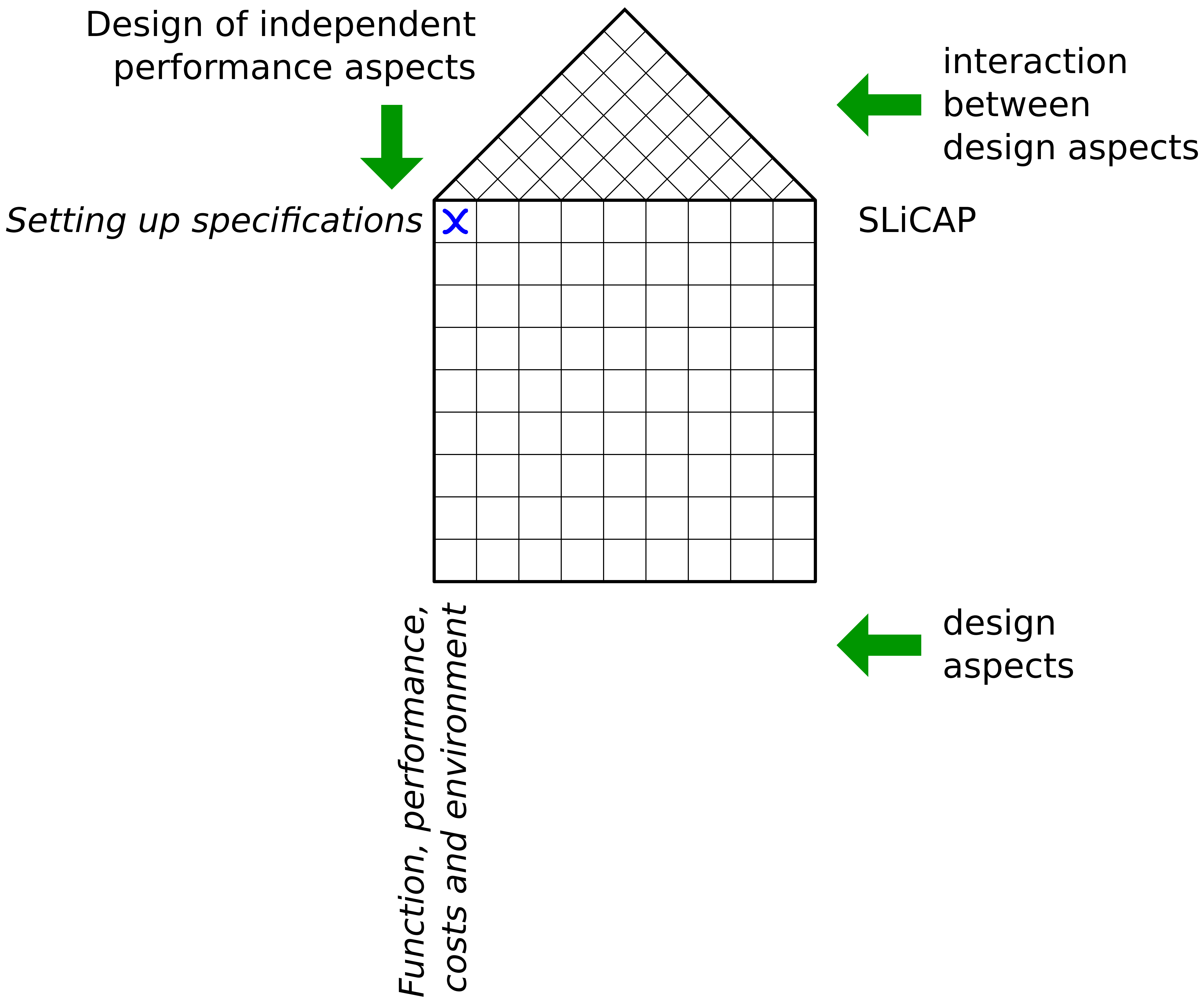

Design of independent
performance aspects
interaction
between
design aspects
Setting up specifications
X
SLiCAP
design
aspects
Function, performance,
costs and environment

Design of the active antenna:



Design of the active antenna:

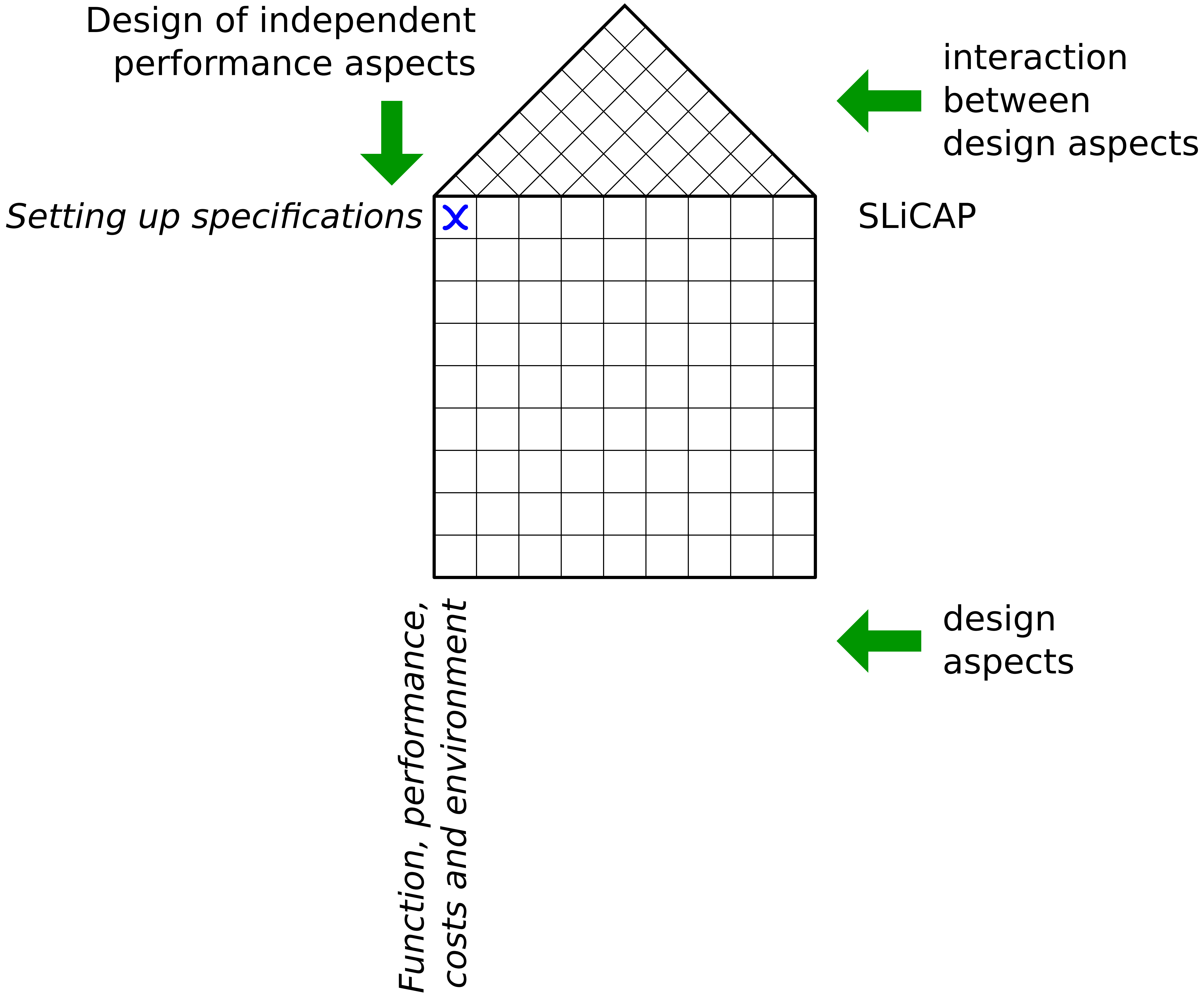
From the application description derive:



Design of the active antenna:

From the application description derive:

Functional requirements

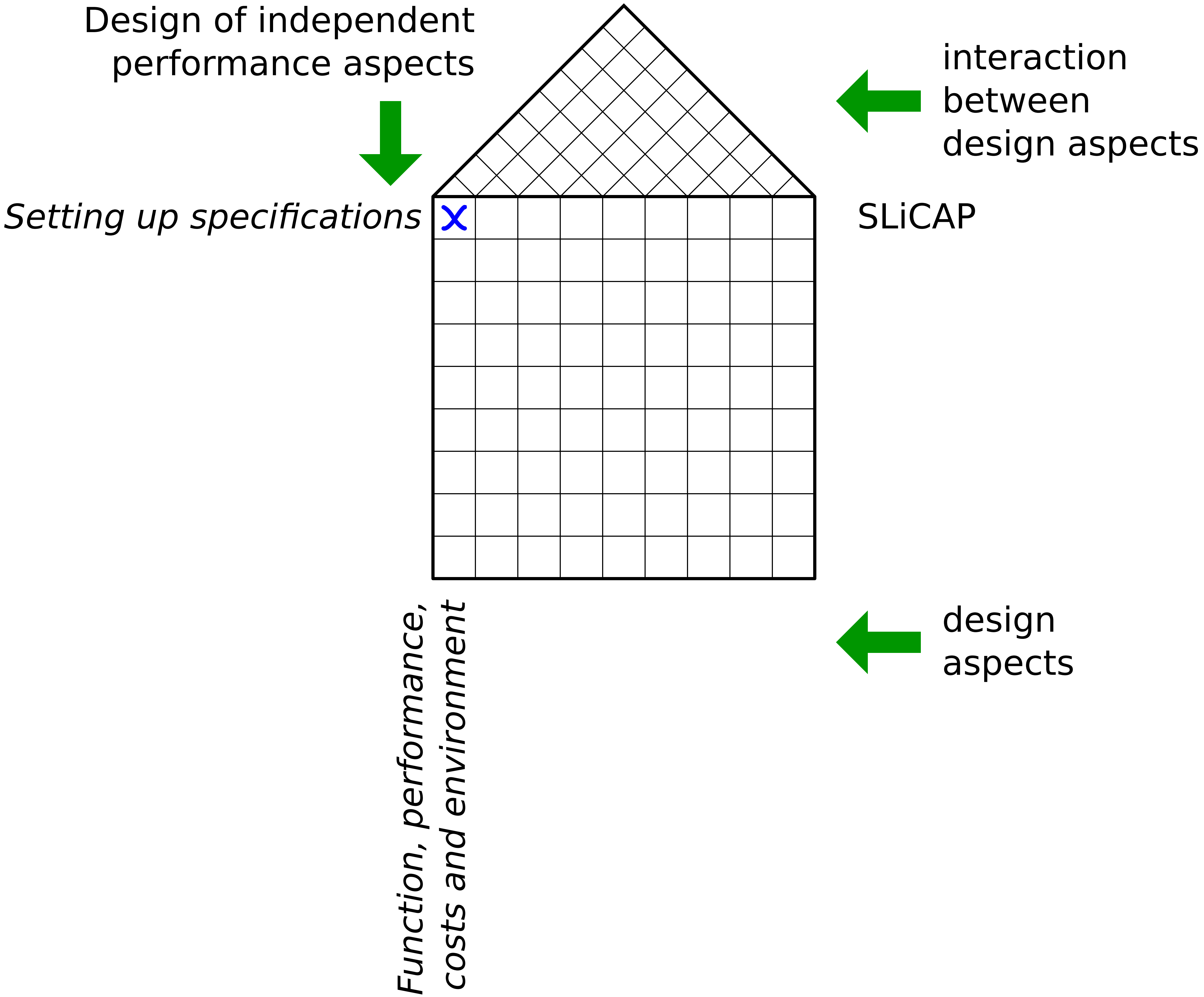


Design of the active antenna:

From the application description derive:

Functional requirements

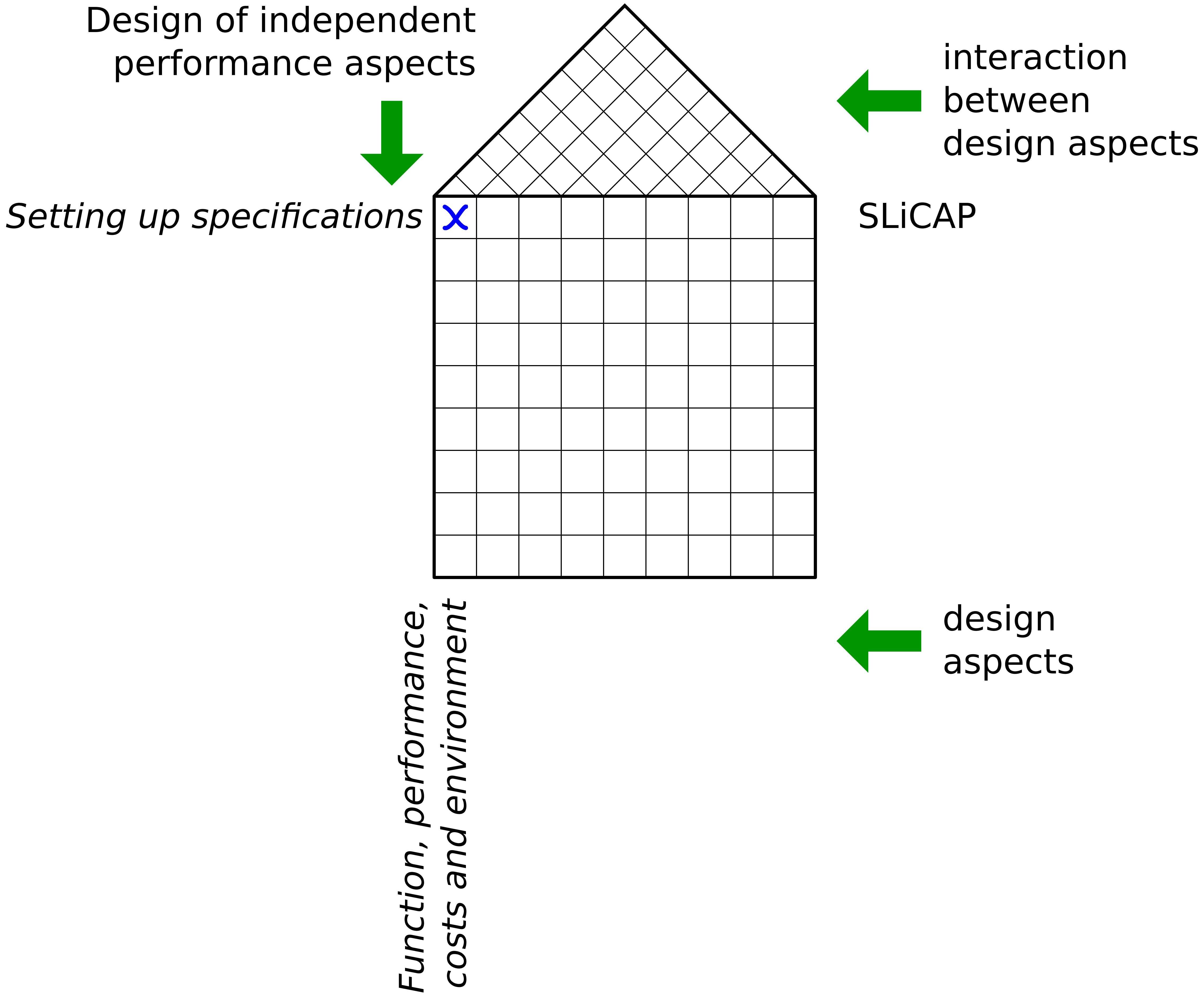
Port impedances



Design of the active antenna:

From the application description derive:

- Functional requirements
  - Port impedances
  - Source-to-load transfer



Design of the active antenna:

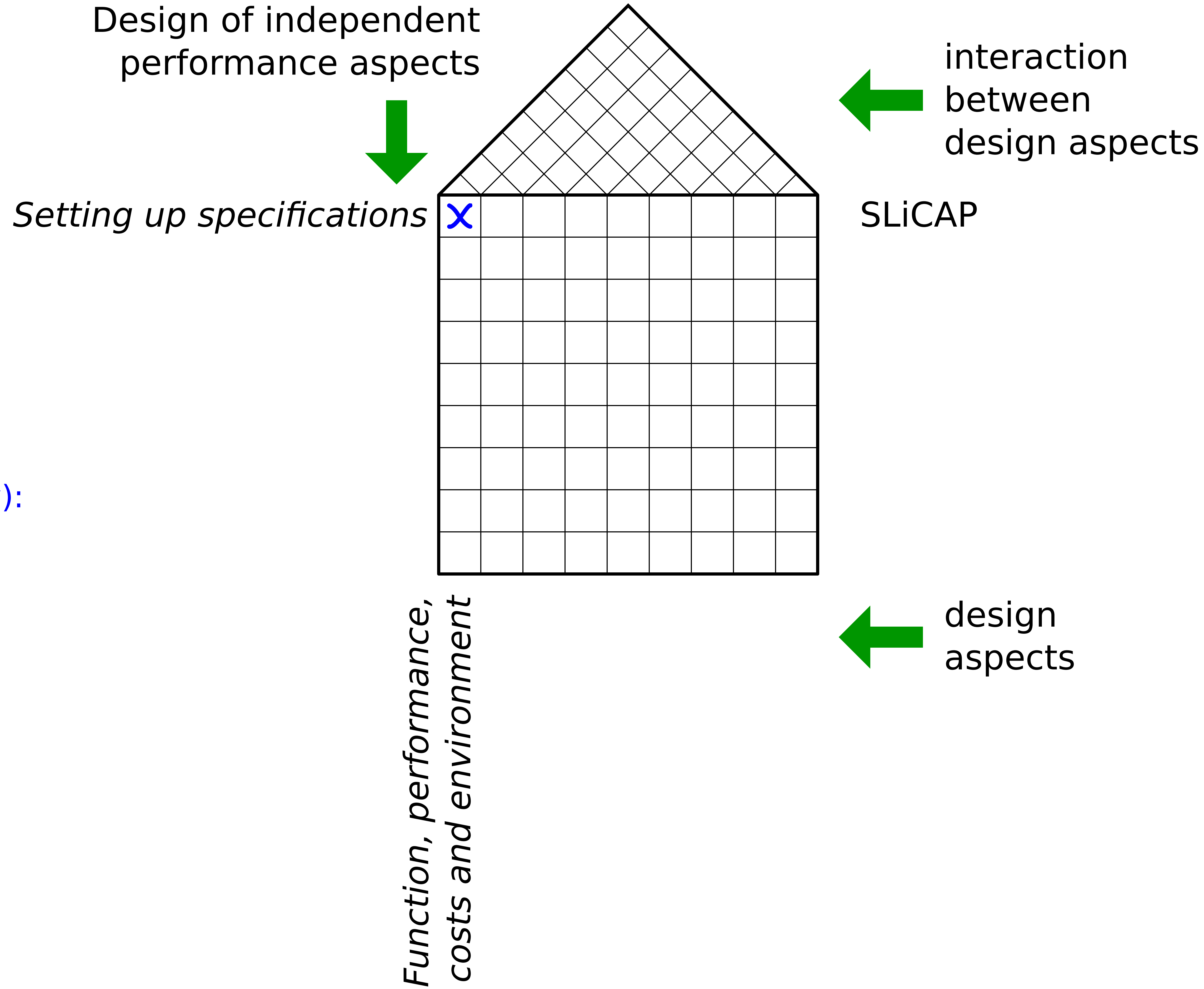
From the application description derive:

Functional requirements

Port impedances

Source-to-load transfer

Performance requirements
(information processing capacity and quality):



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From the application description derive:

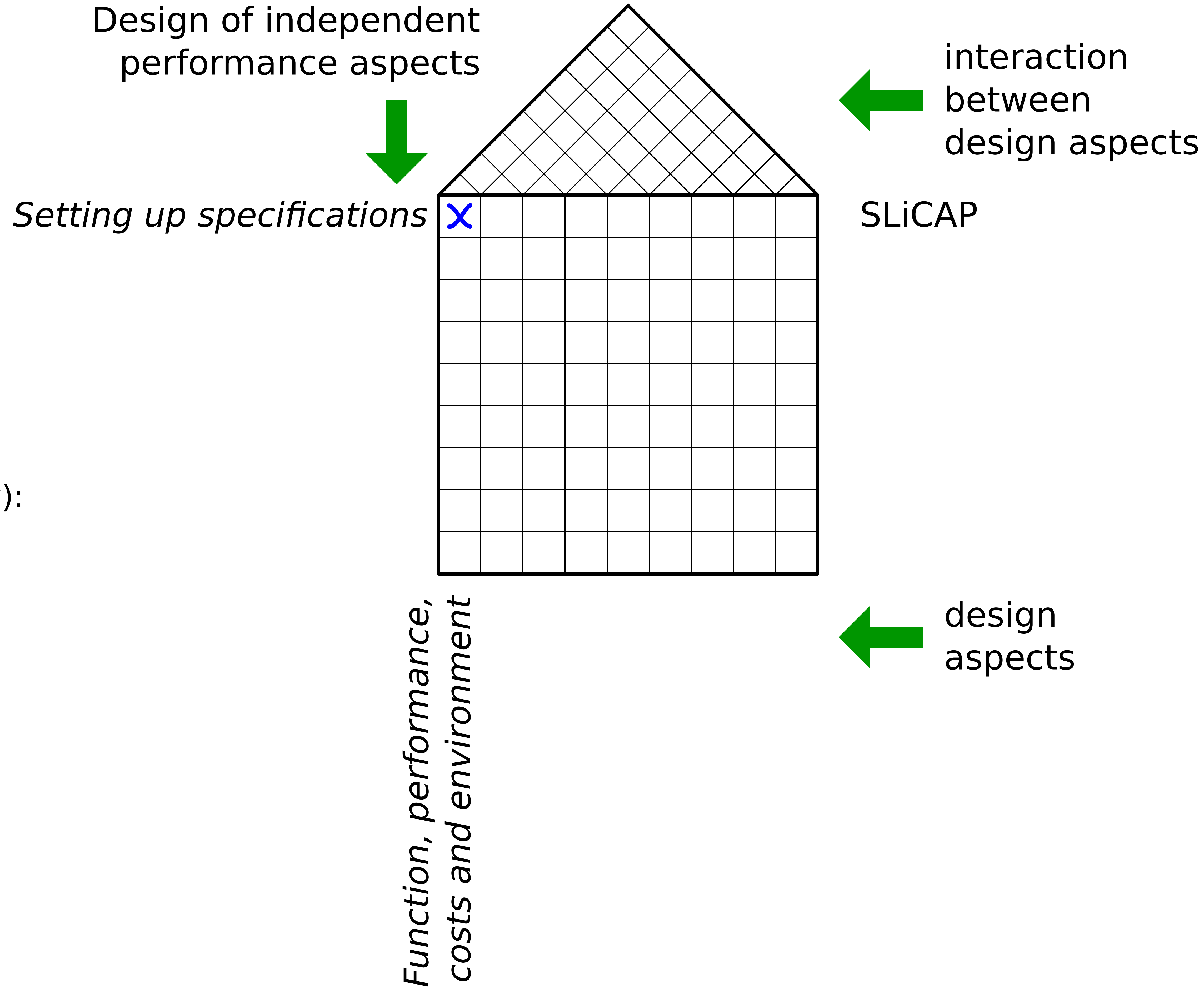
Functional requirements

Port impedances

Source-to-load transfer

Performance requirements
(information processing capacity and quality):

Noise addition (temperature ofset drift)



Design of the active antenna:

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Source-to-load transfer

Performance requirements
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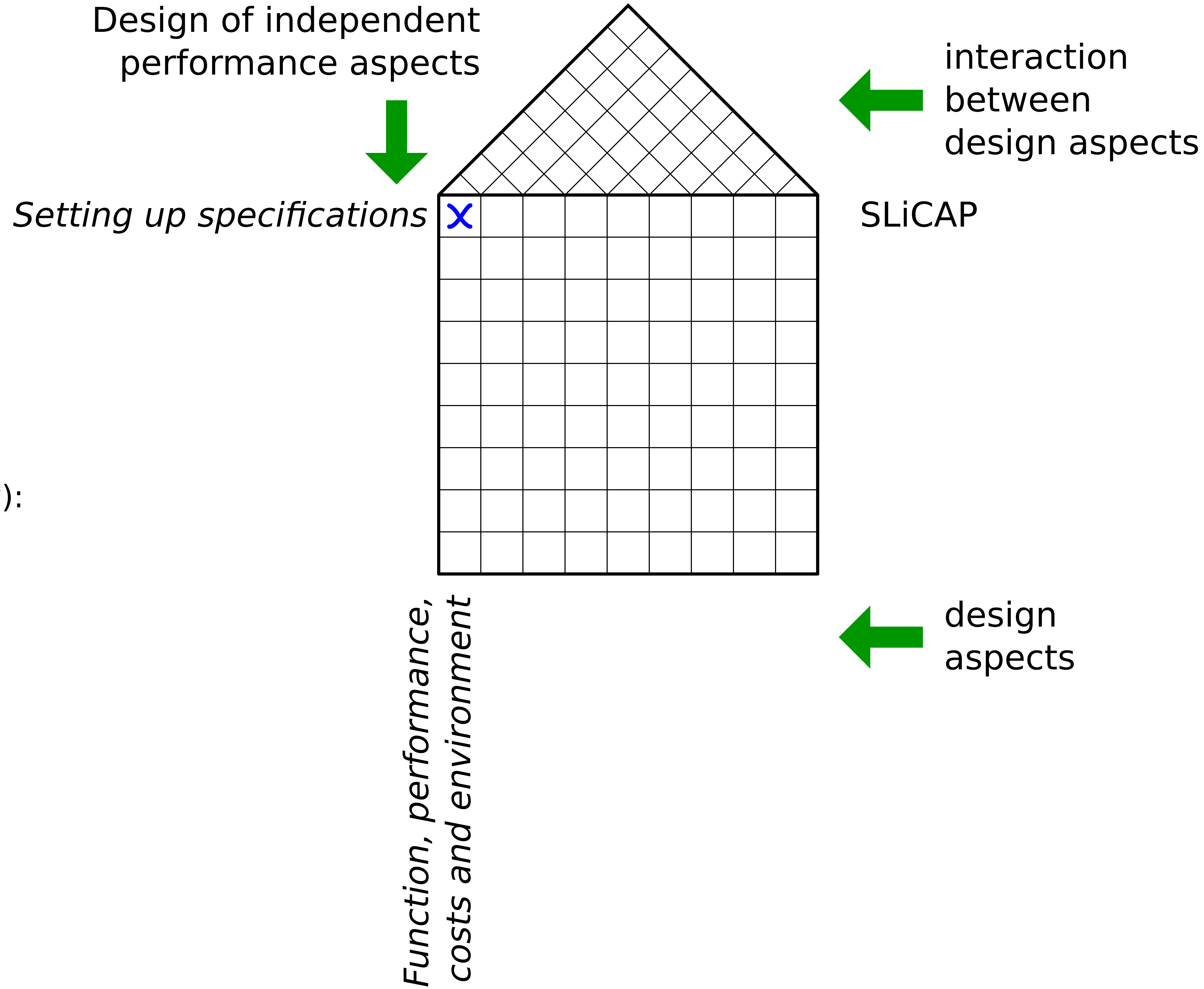
Noise addition (temperature ofset drift)

Static and dynamic signal handling capability



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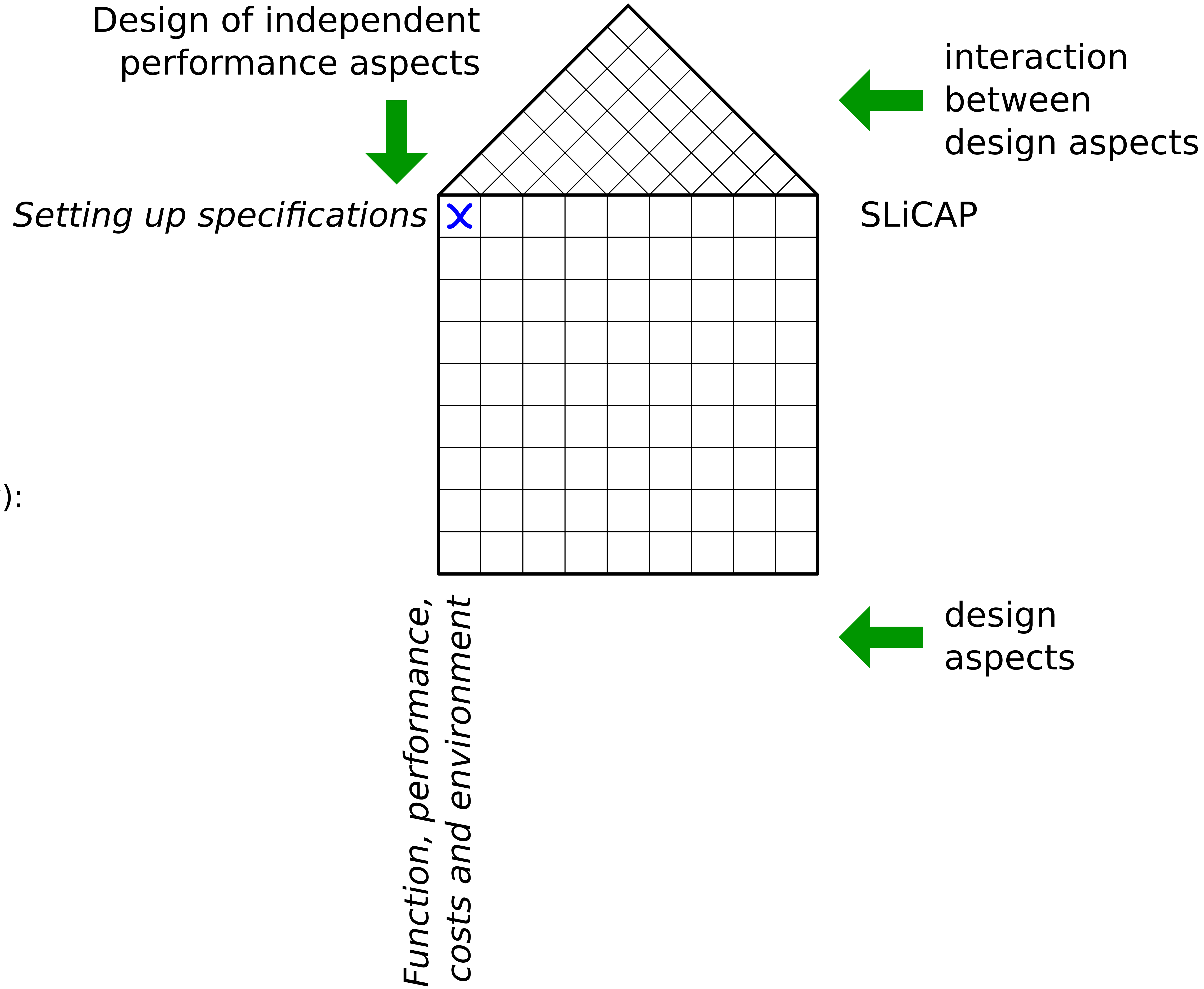
Static and dynamic signal handling capability

Inaccuracy (temperature gain drift)



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Performance requirements (information processing capacity and quality):

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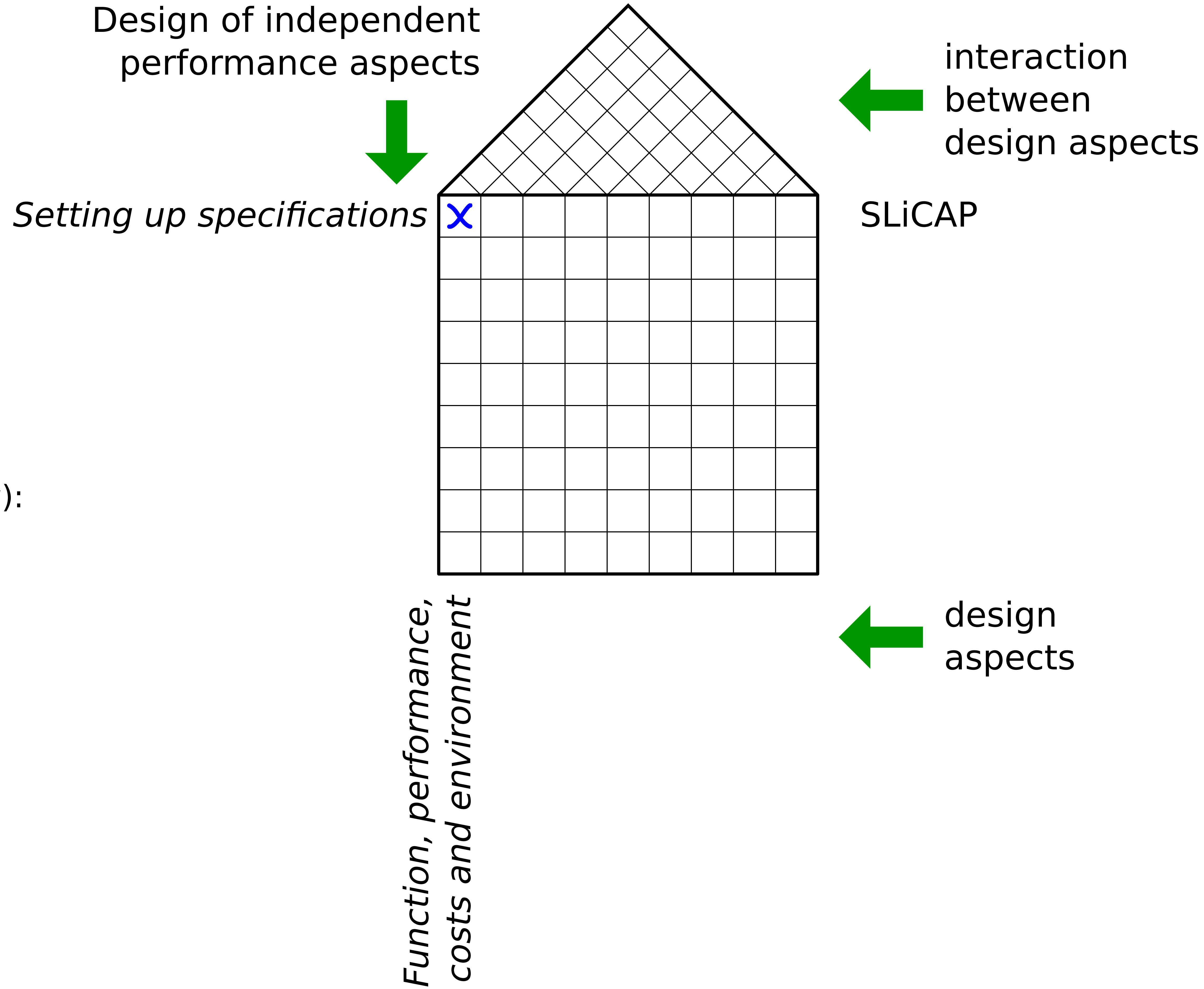

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Performance requirements
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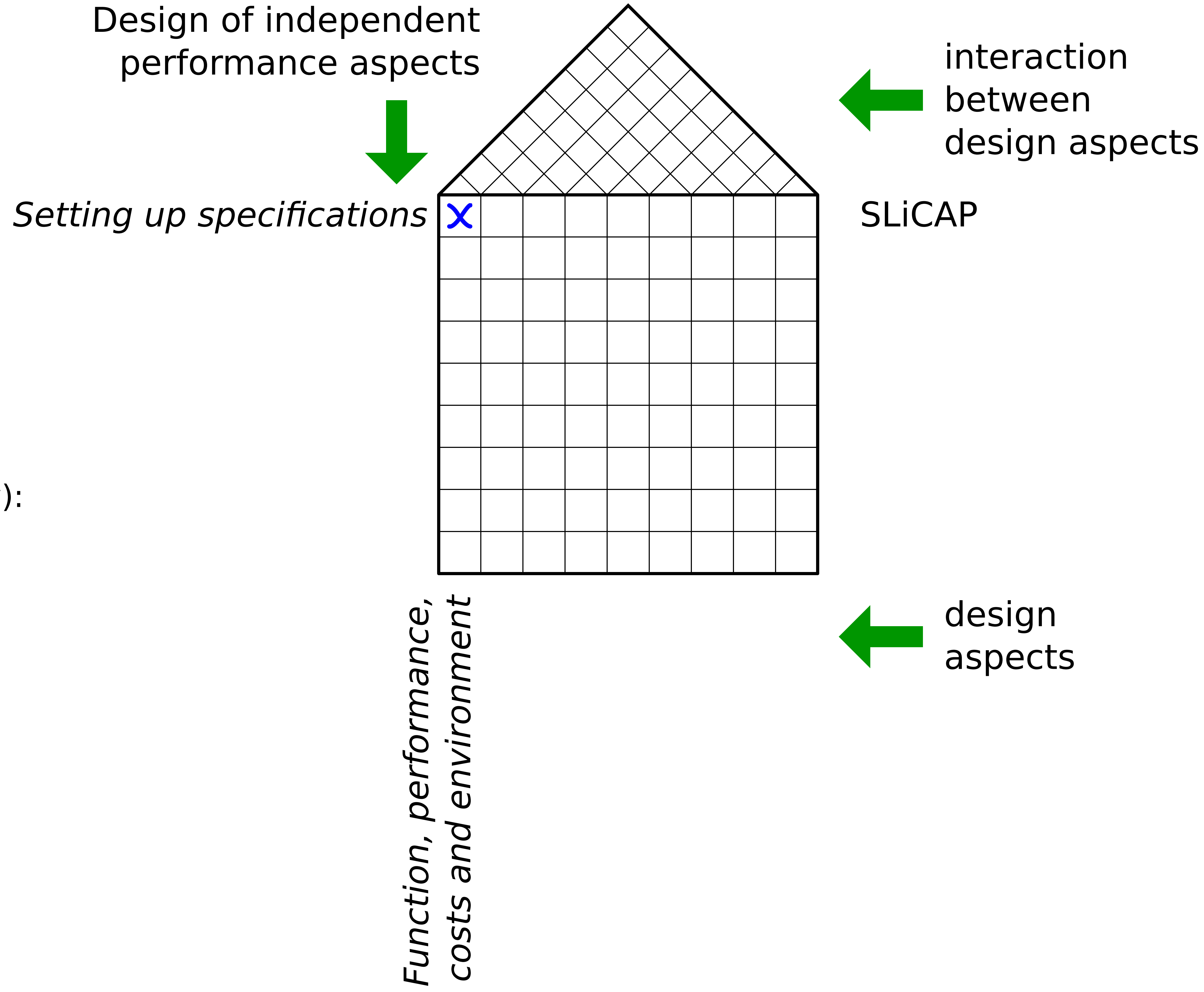
- Inaccuracy (temperature gain drift)
- Frequency or time domain response
- Weak nonlinearity



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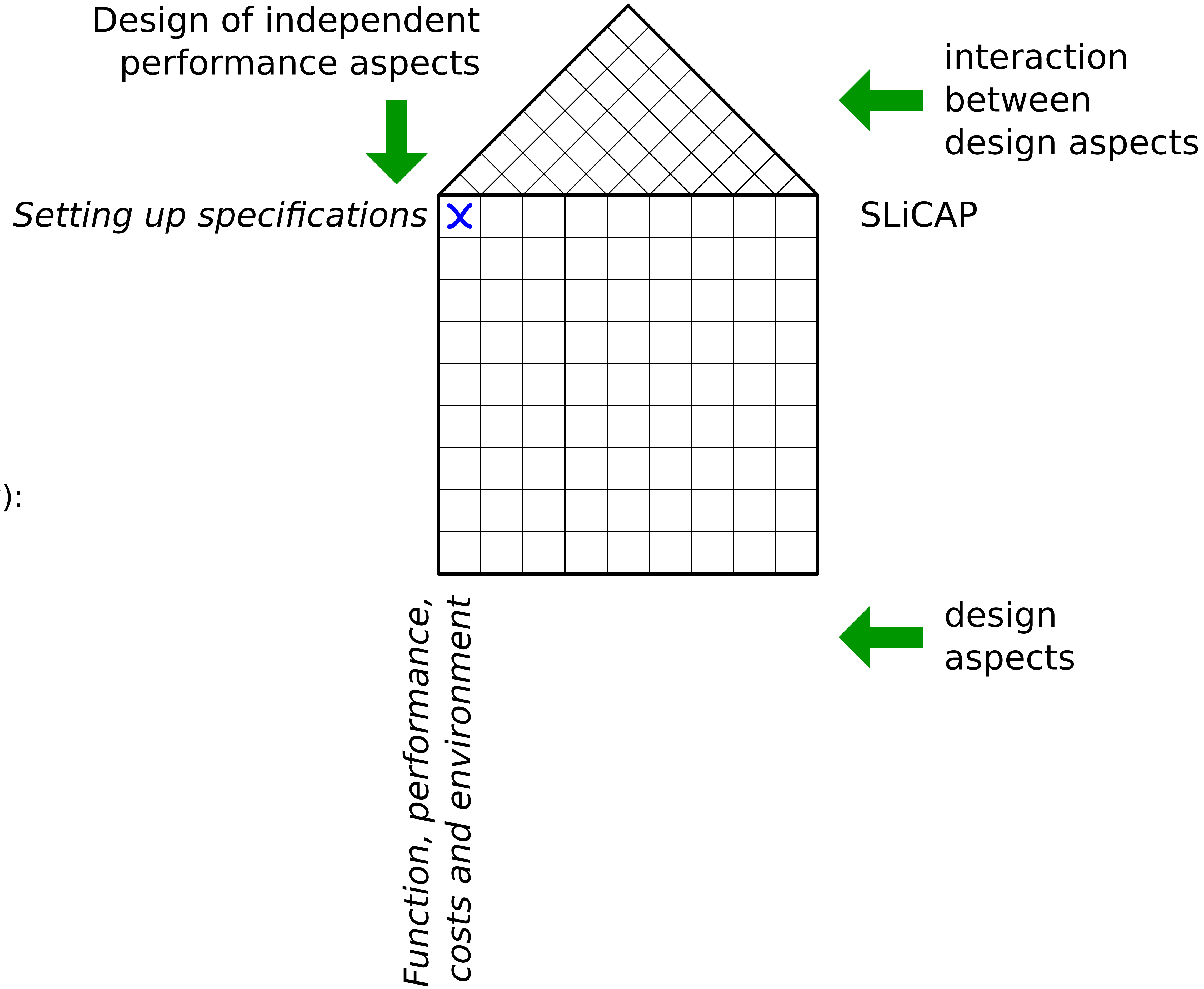
Cost factors:



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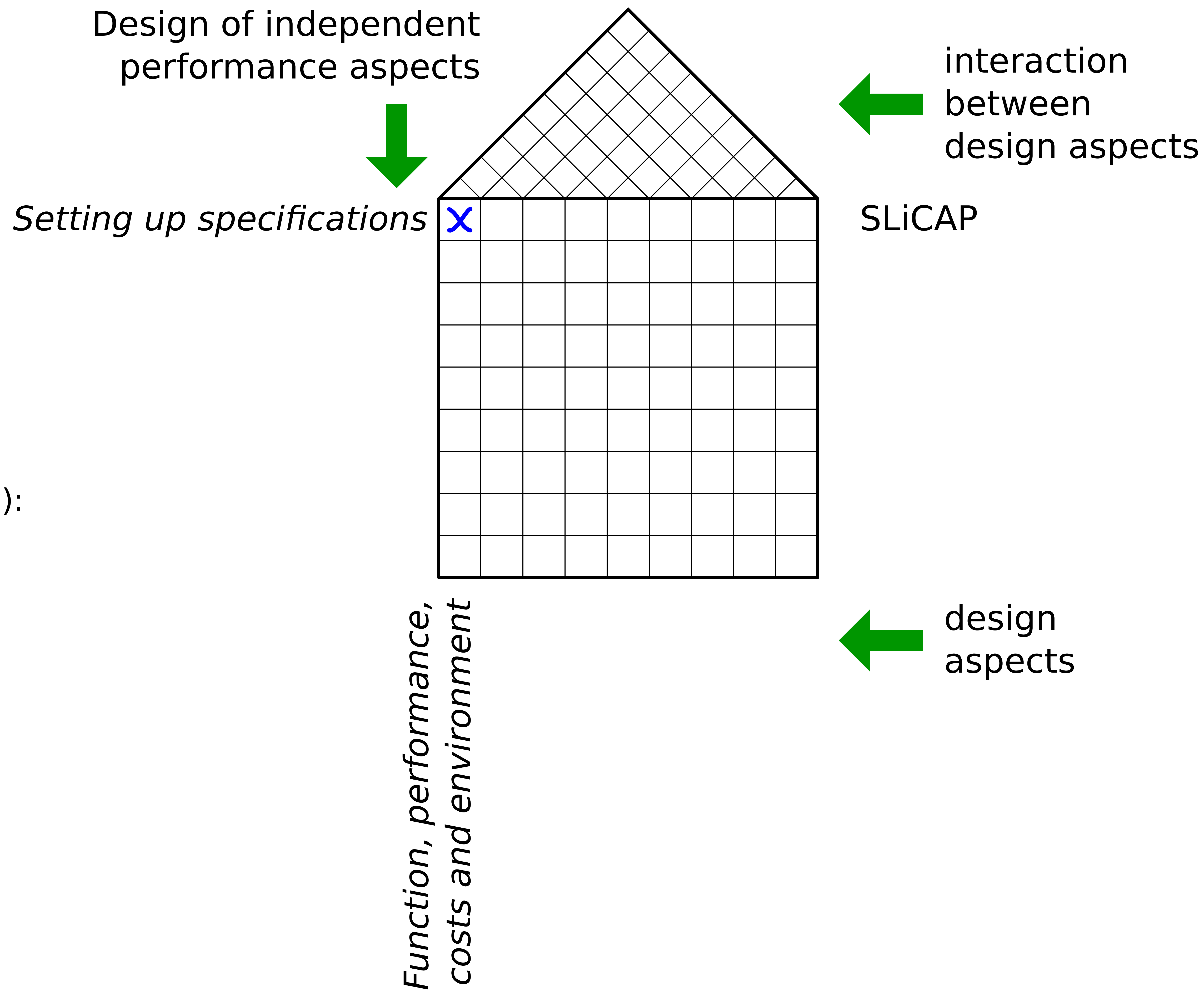

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Cost factors:

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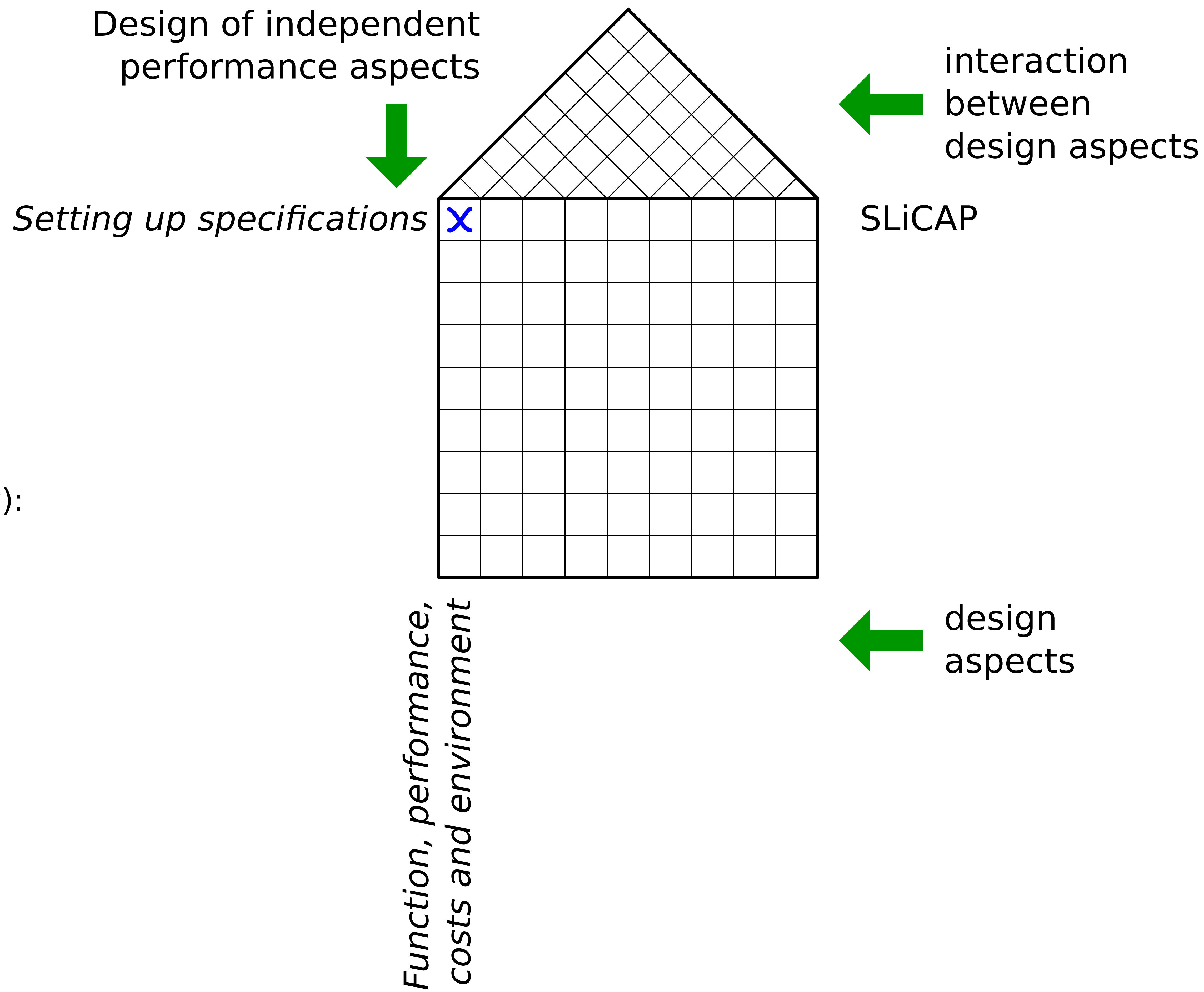

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Cost factors:

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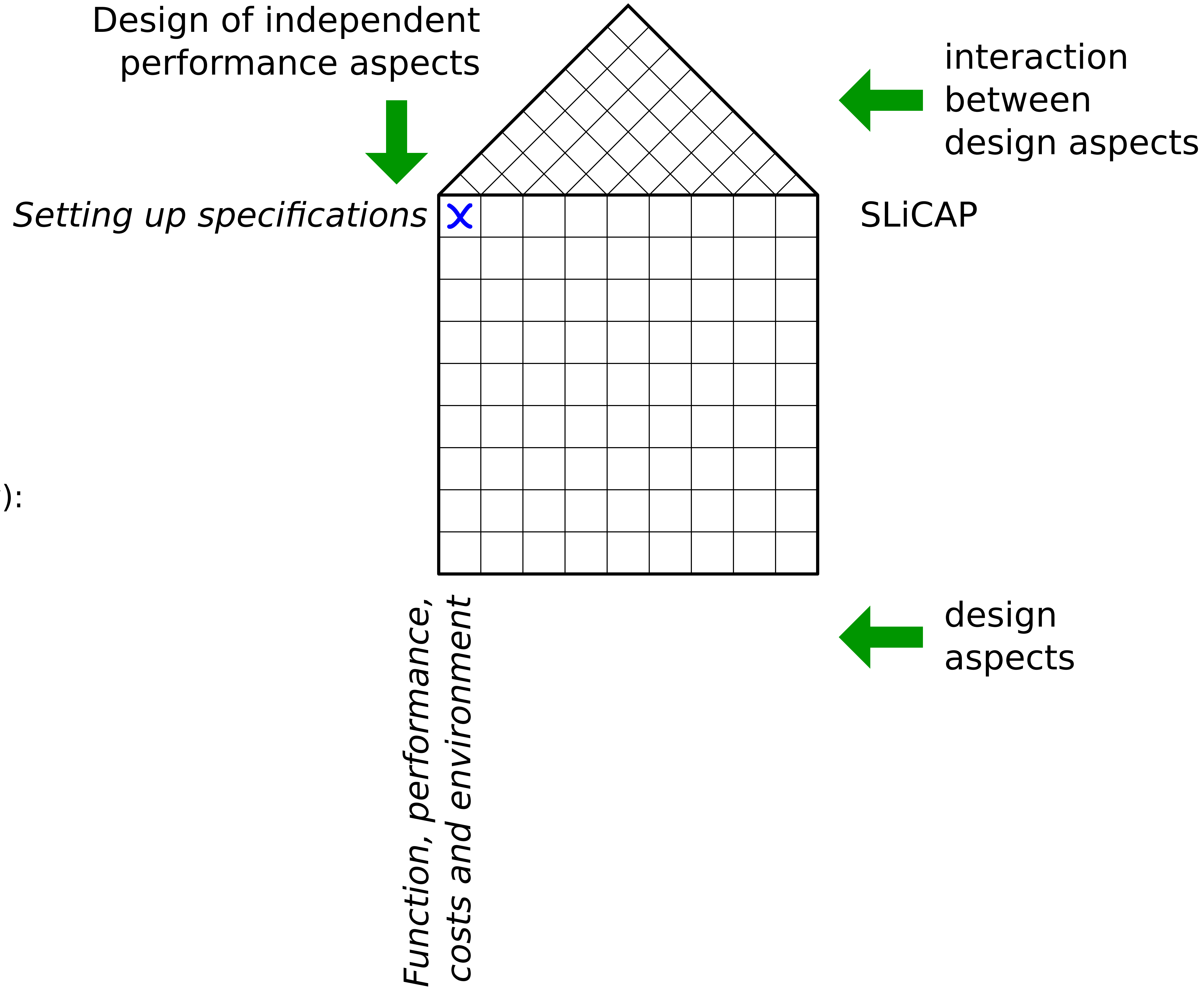
- Dimensions



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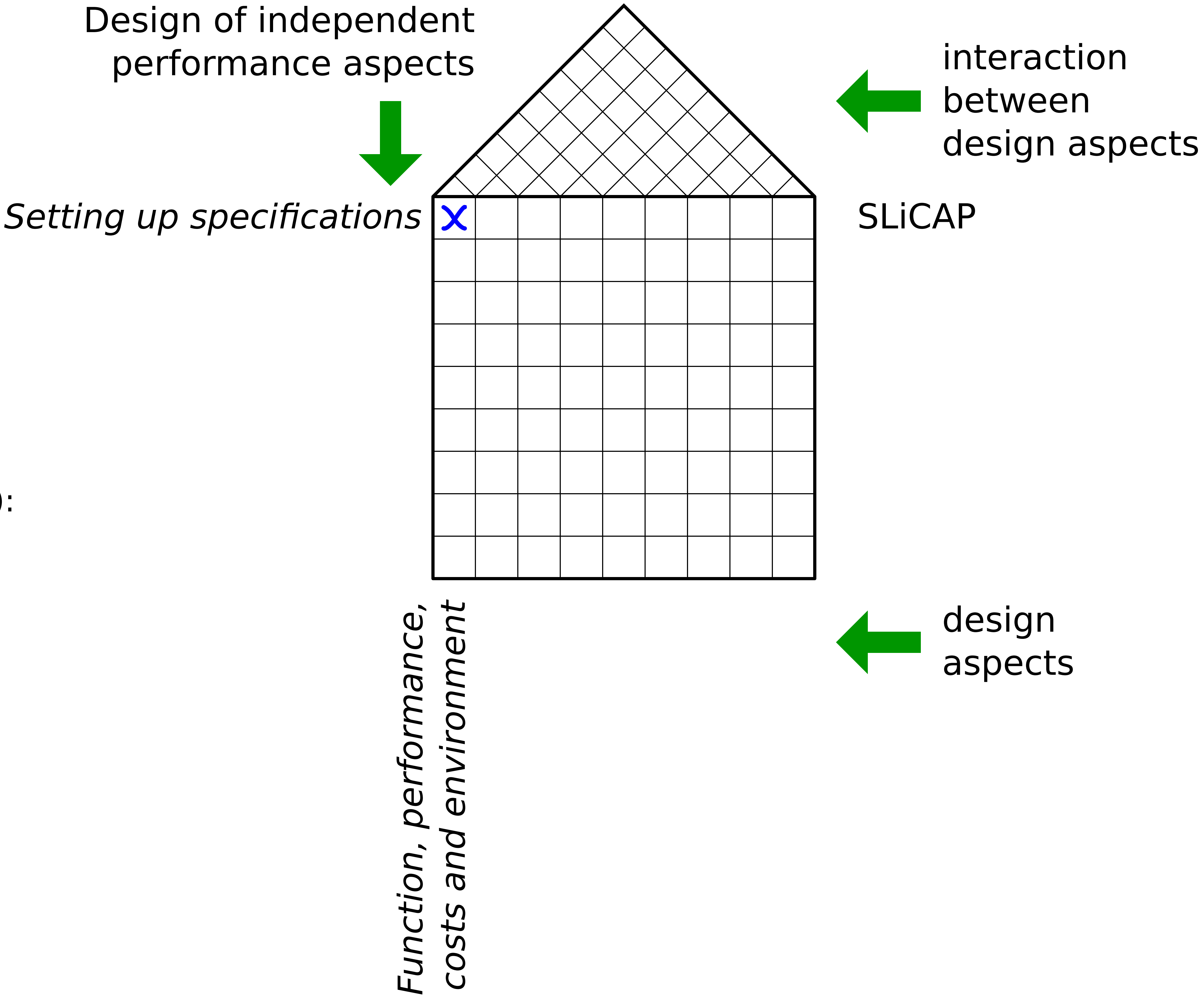
  - Dimensions
- Operating conditions:



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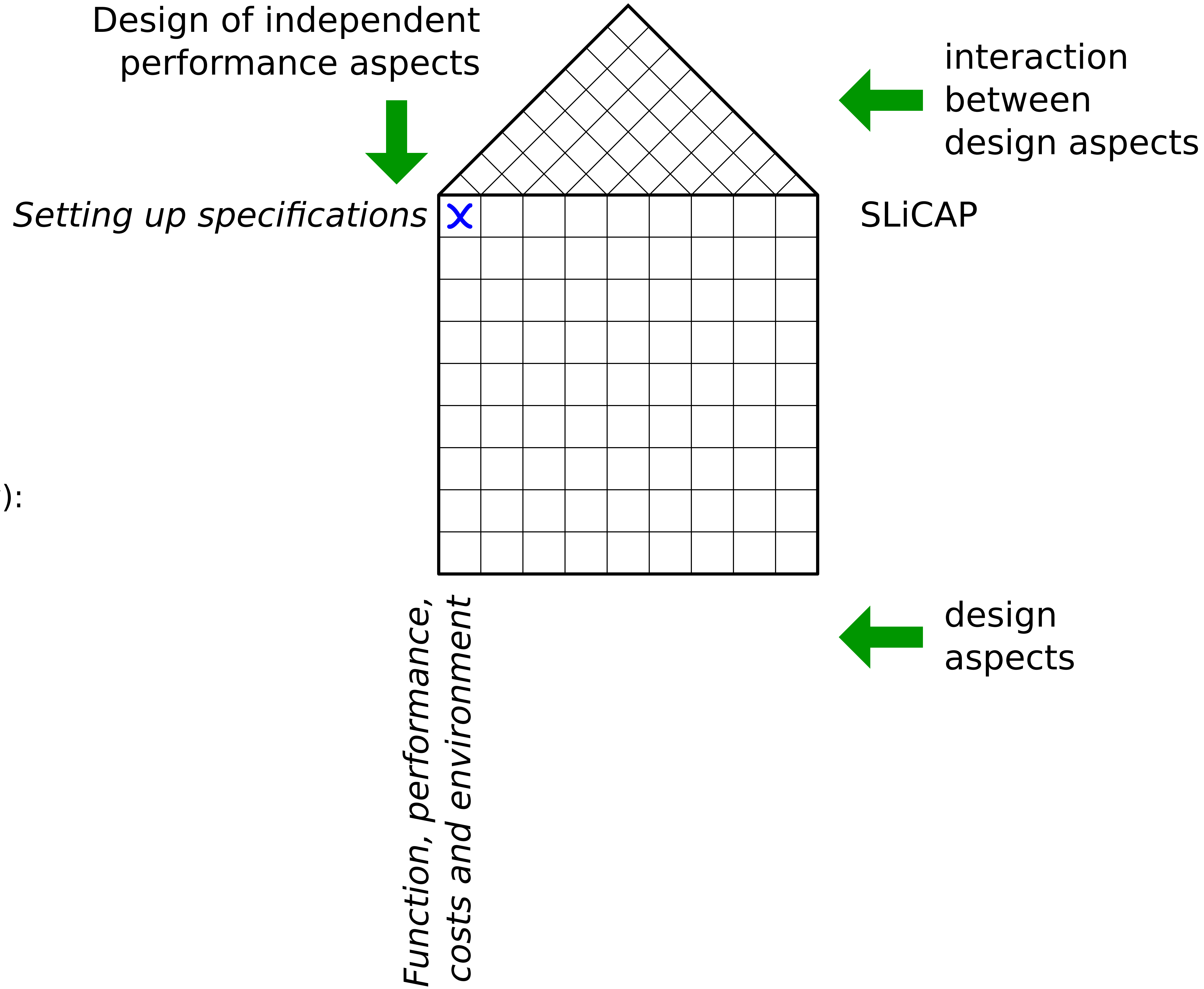
  - Current consumption
  - Dimensions
- Operating conditions:
  - Temperature range



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- Cost factors:
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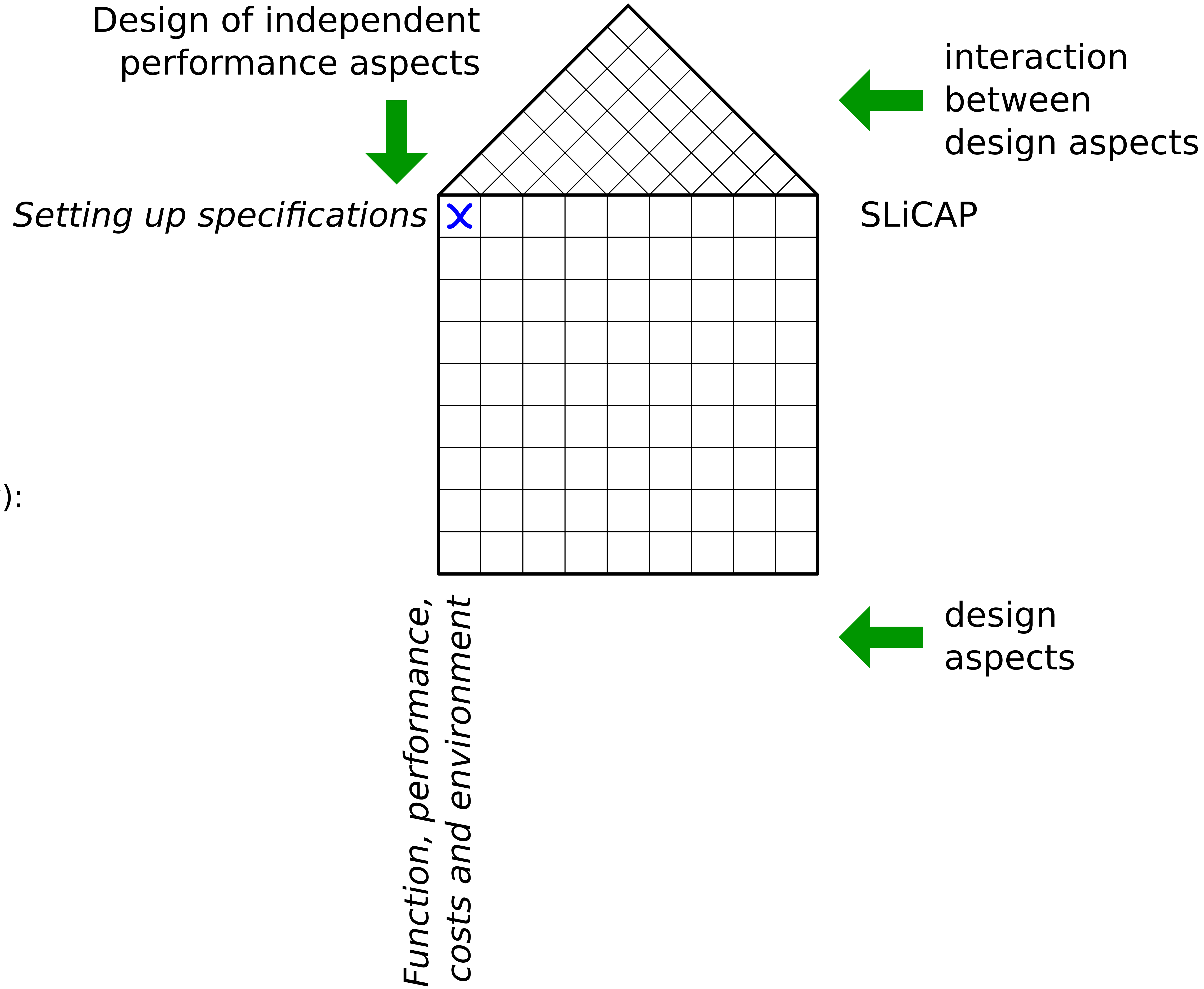
  - Current consumption
  - Dimensions
- Operating conditions:
  - Temperature range
  - EMI, ESD



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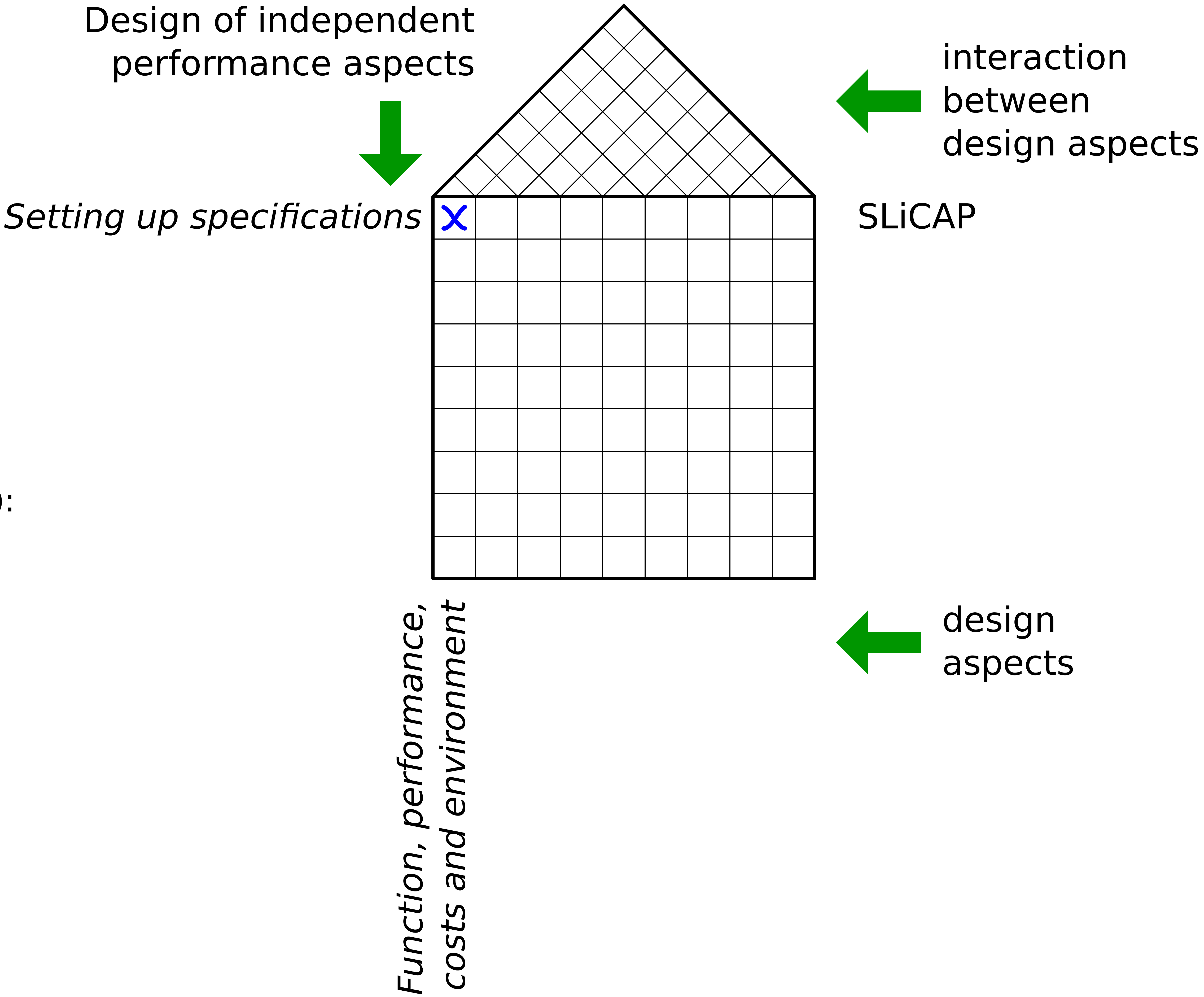
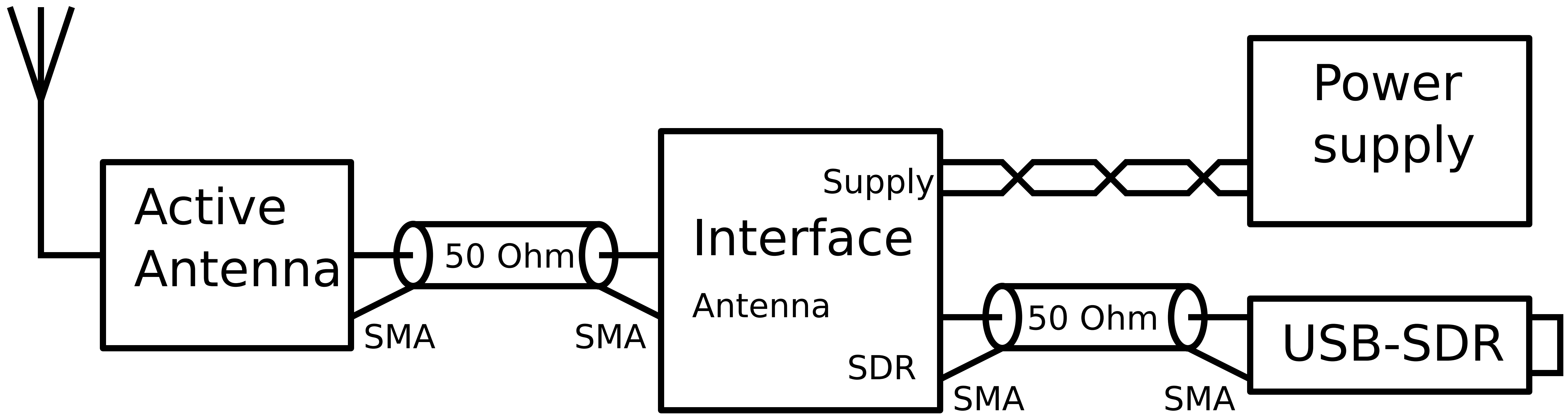
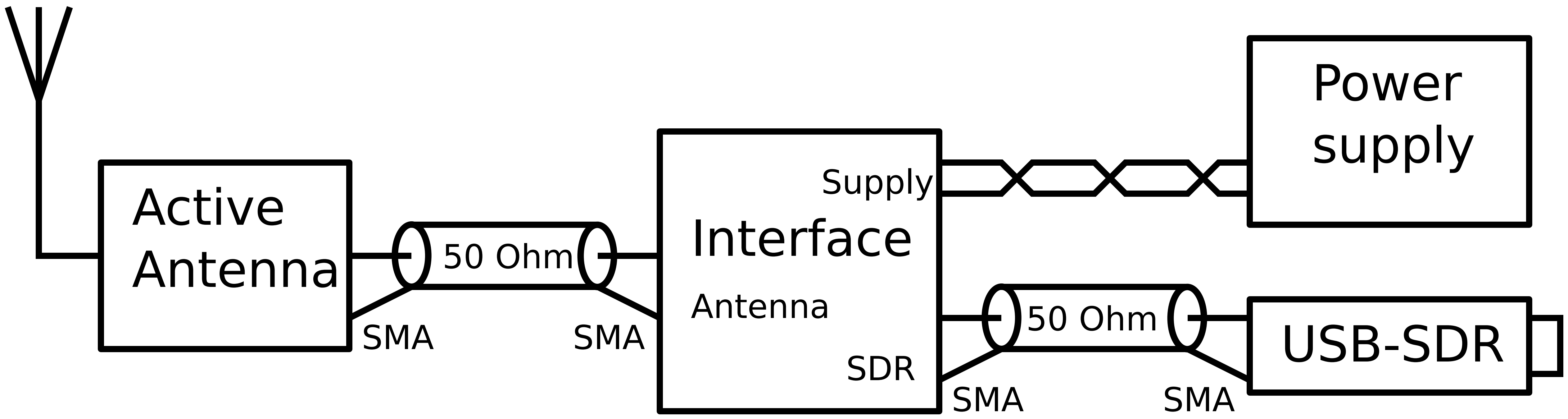
Operating conditions:

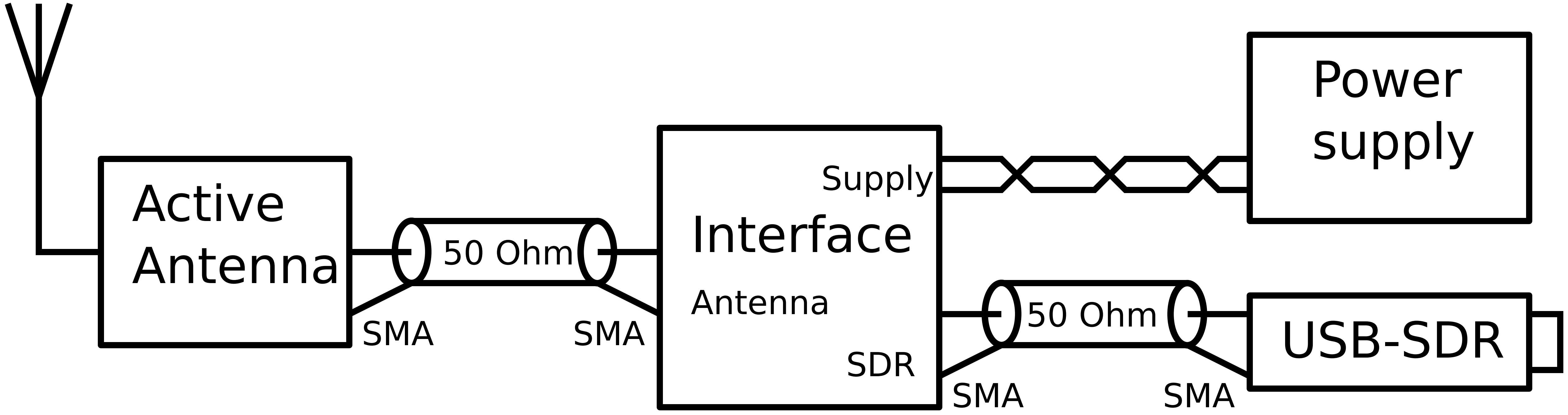
- Temperature range
- EMI, ESD




Active
Antenna
50 Ohm
SMA
SMA
Supply
Interface
Antenna
SDR
Power
supply
50 Ohm
USB-SDR
SMA
SMA

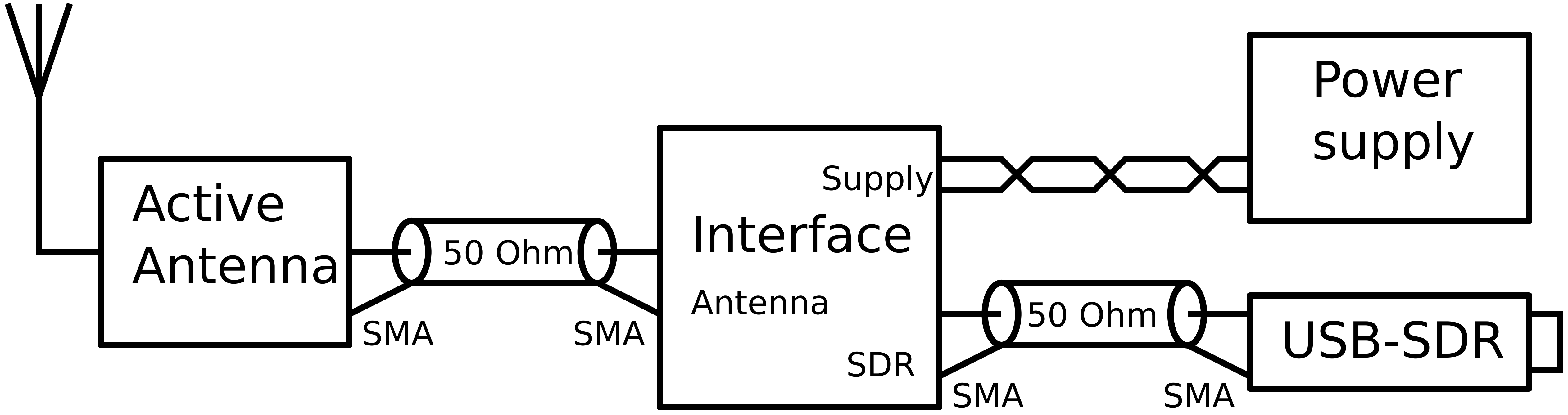


Performance



Performance

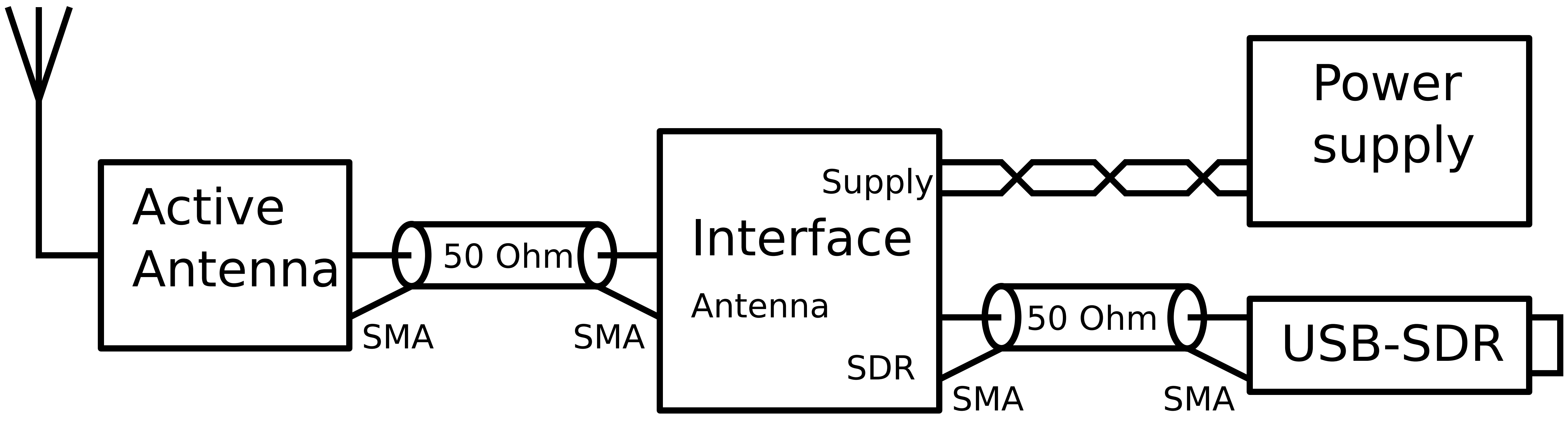
Maximum RMS input signal



Performance

Maximum RMS input signal

Maximum RMS output voltage across 50 Ohm

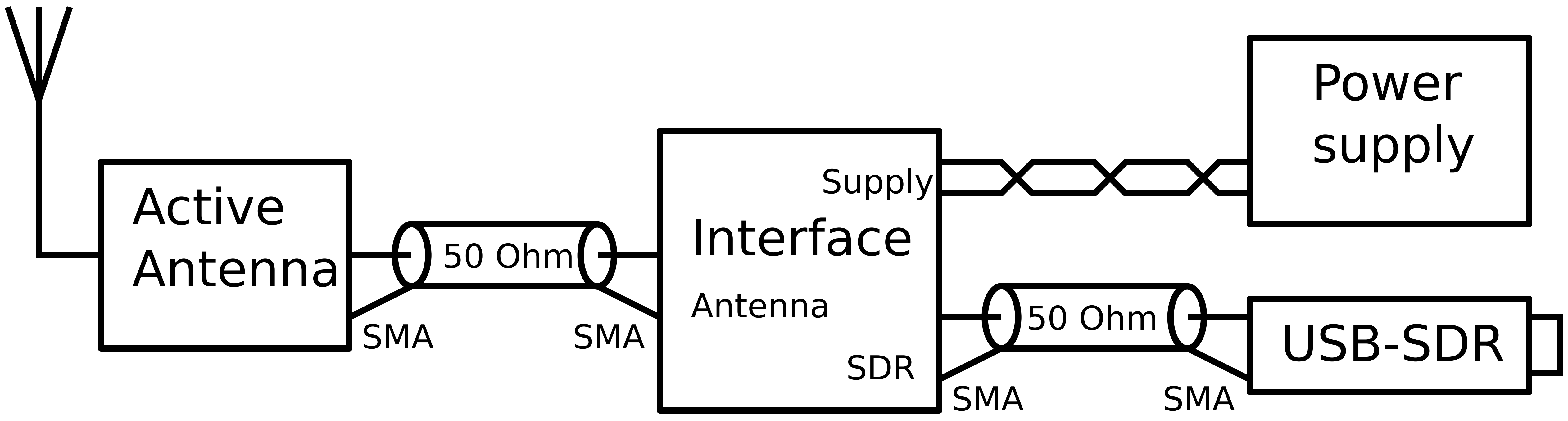


Performance

Maximum RMS input signal

Maximum RMS output voltage across 50 Ohm

Antenna referred noise



Performance

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Maximum RMS output voltage across 50 Ohm

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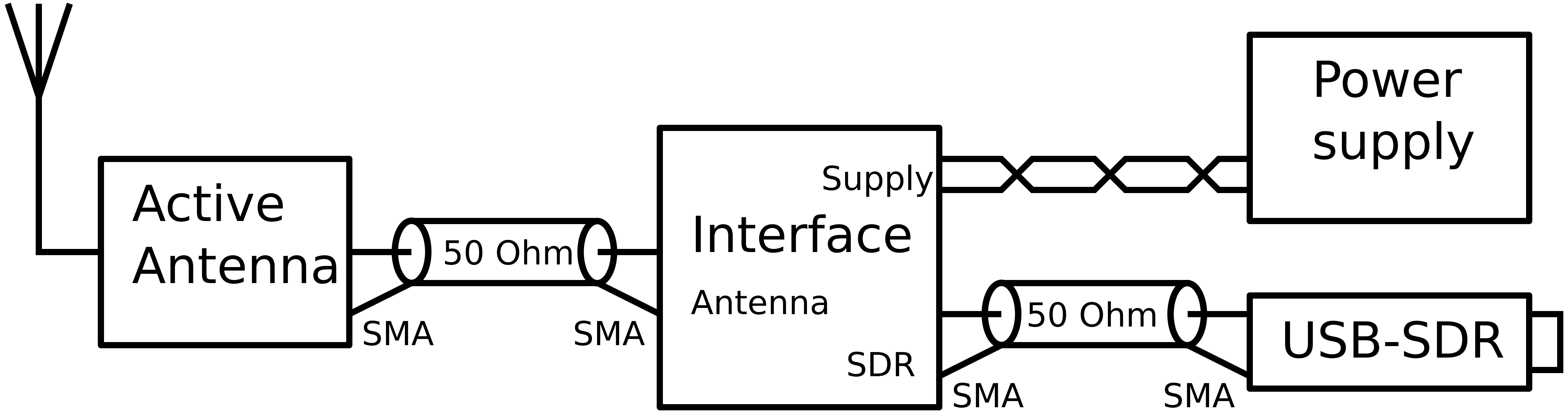
Output impedance



Performance

Maximum RMS input signal

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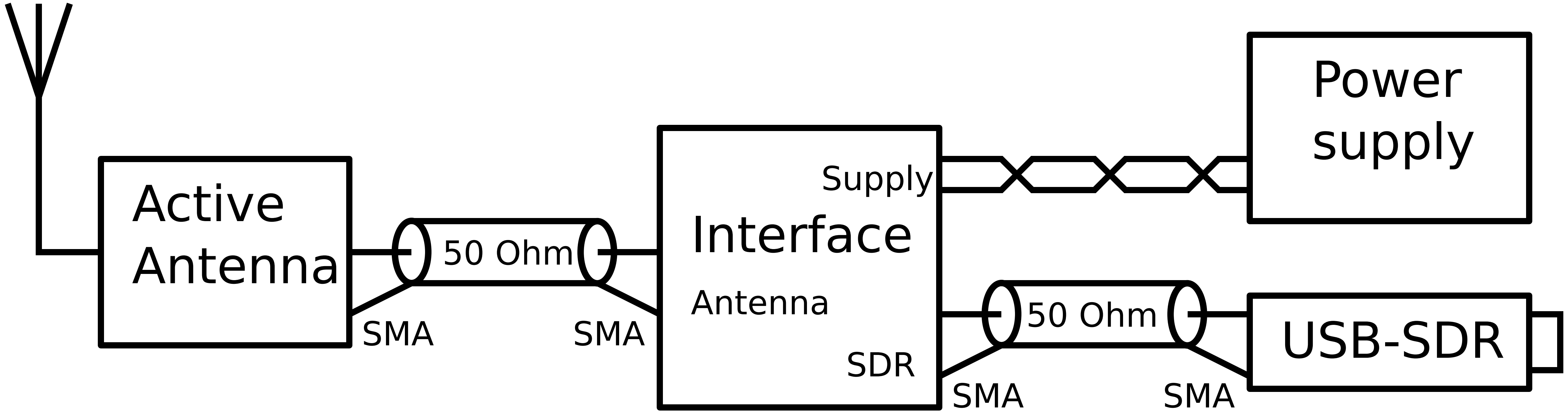
Output impedance

Frequency range of interest



Performance

Maximum RMS input signal

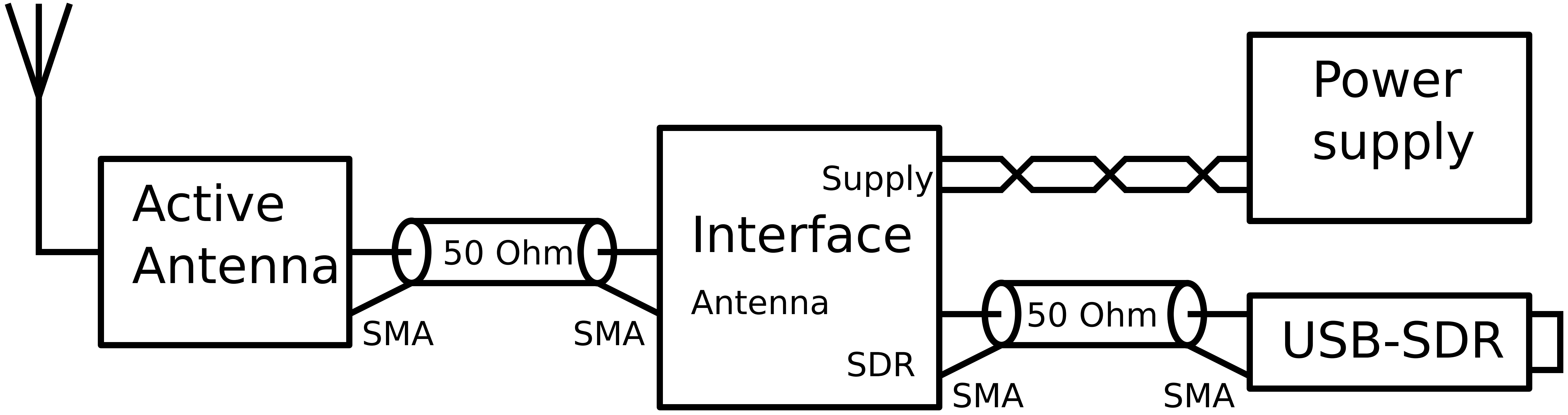
Maximum RMS output voltage across 50 Ohm

Antenna referred noise

Output impedance

Frequency range of interest

Response type



Performance

Maximum RMS input signal

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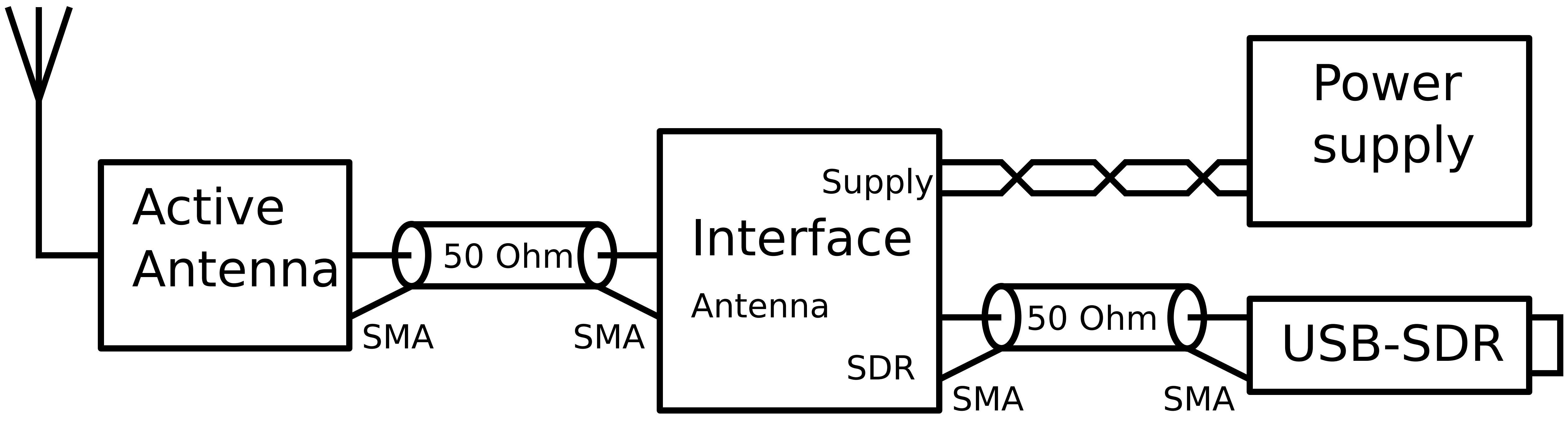
Output impedance

Frequency range of interest

Response type

IMD



Performance

Maximum RMS input signal

Maximum RMS output voltage across 50 Ohm

Antenna referred noise

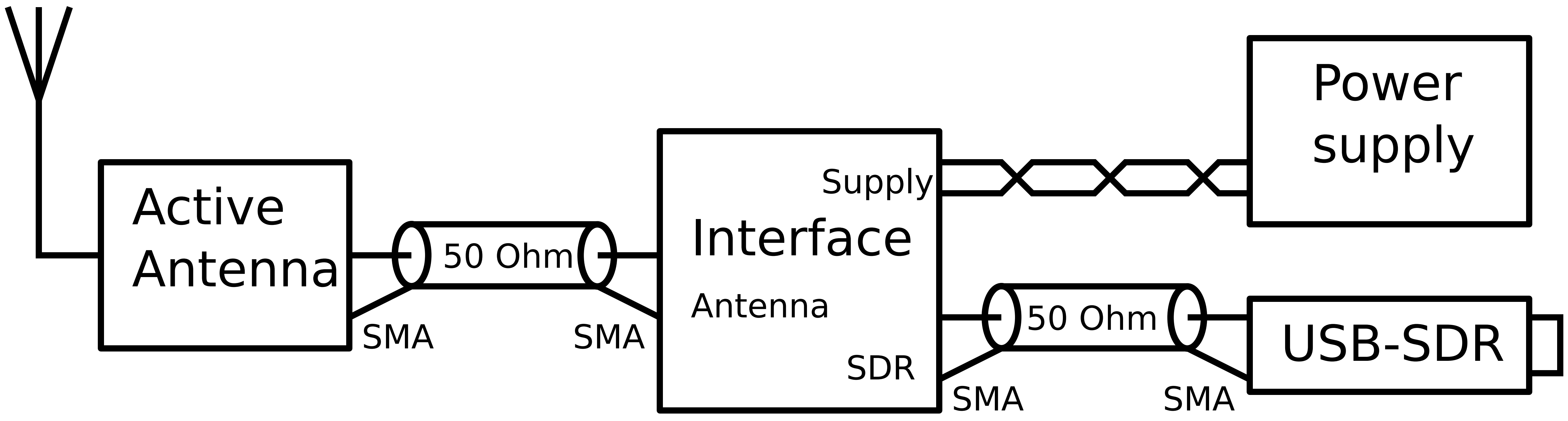
Output impedance

Frequency range of interest

Response type

IMD

Costs



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Frequency range of interest

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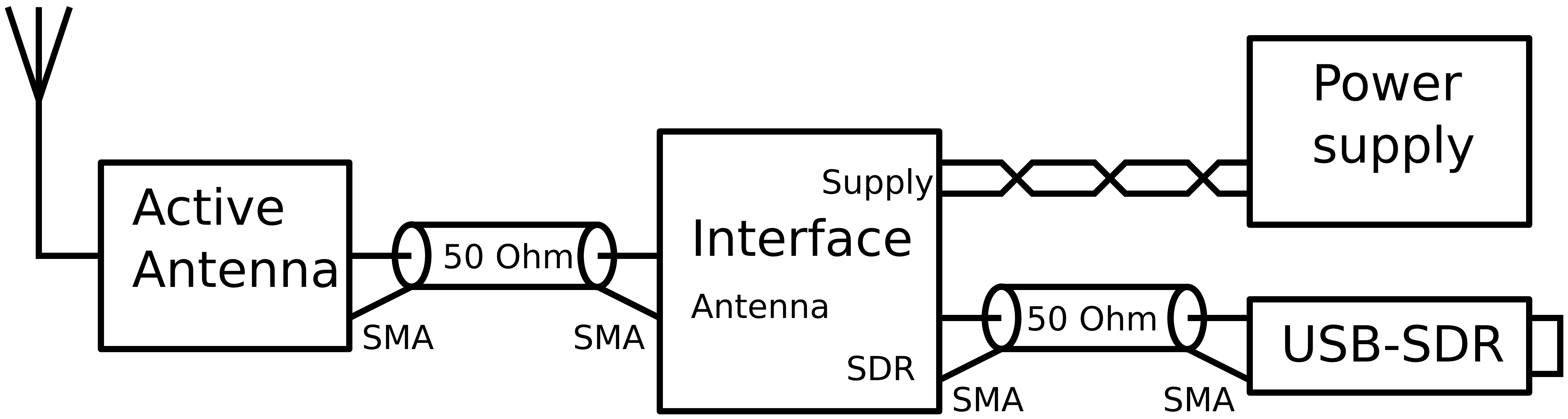
Antenne length



Performance

Maximum RMS input signal

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Antenna referred noise

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Frequency range of interest

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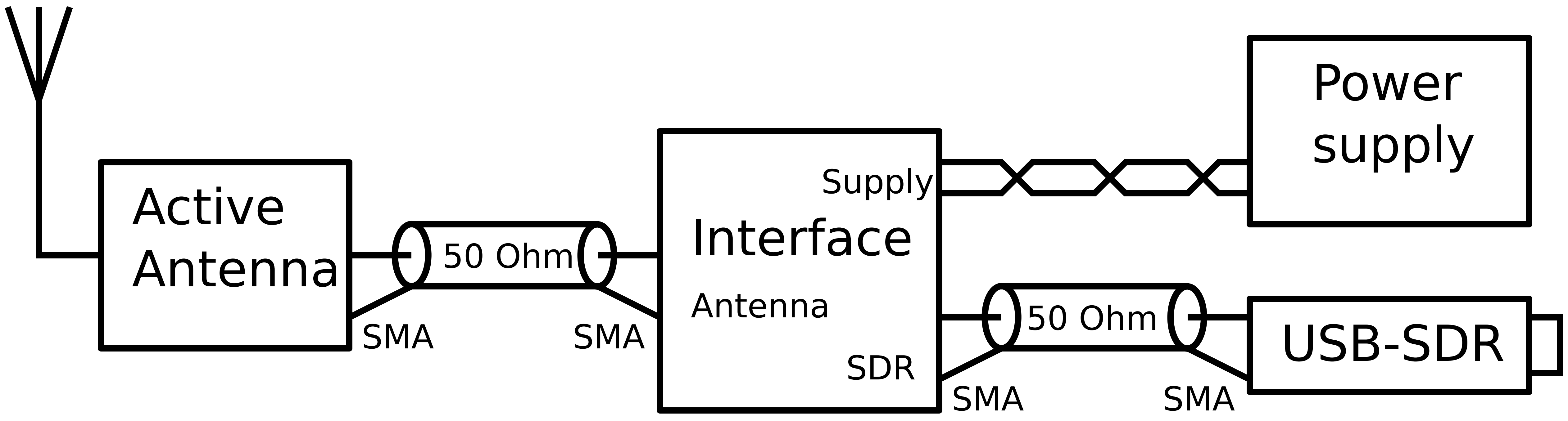
Costs

Antenne length

Supply voltage



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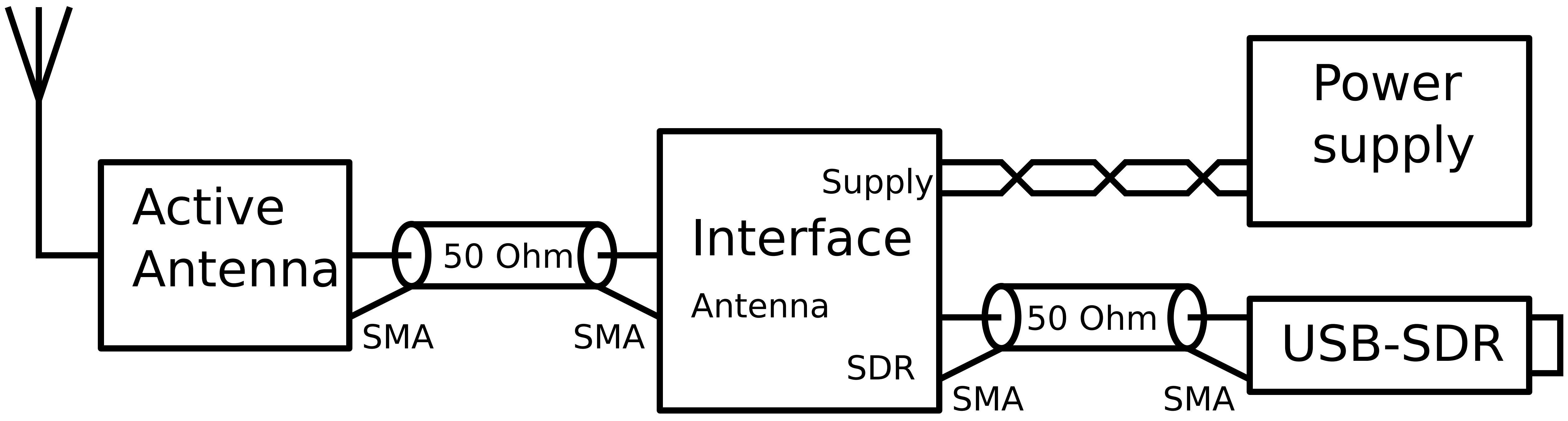

Performance

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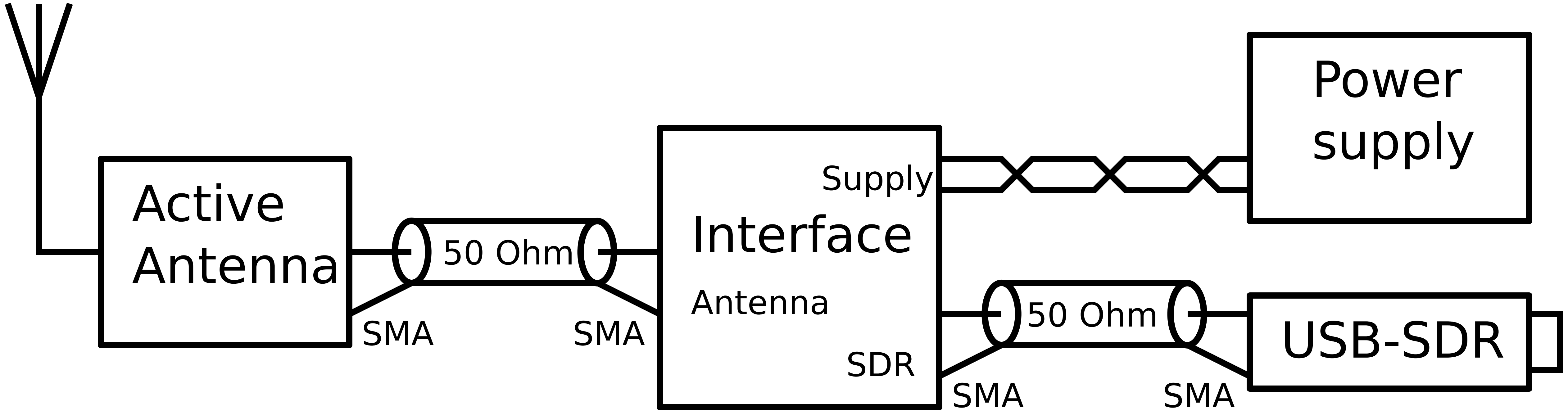

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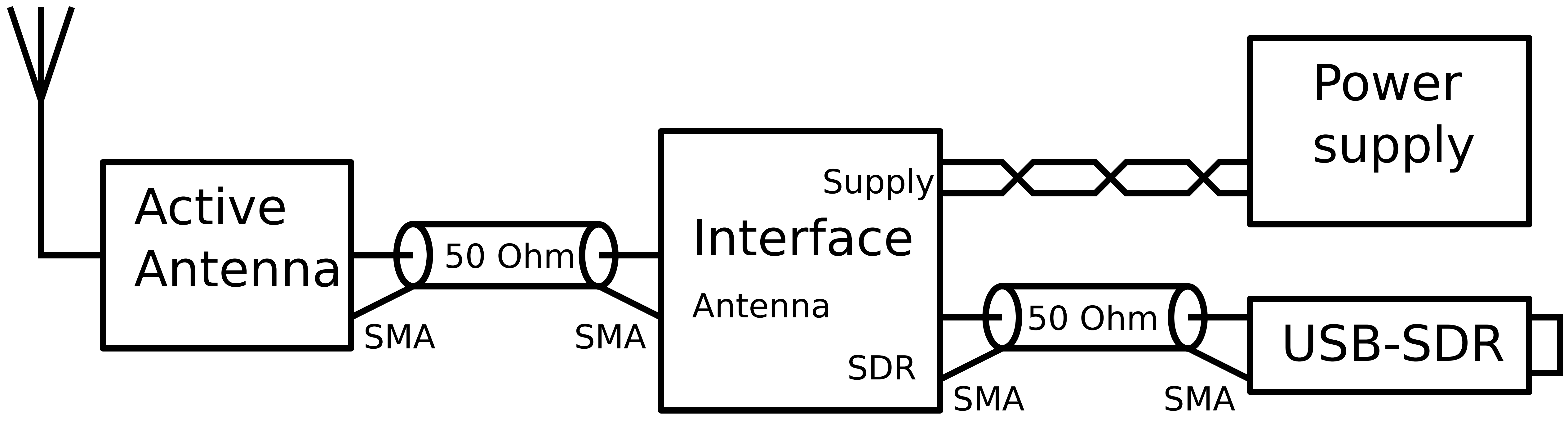

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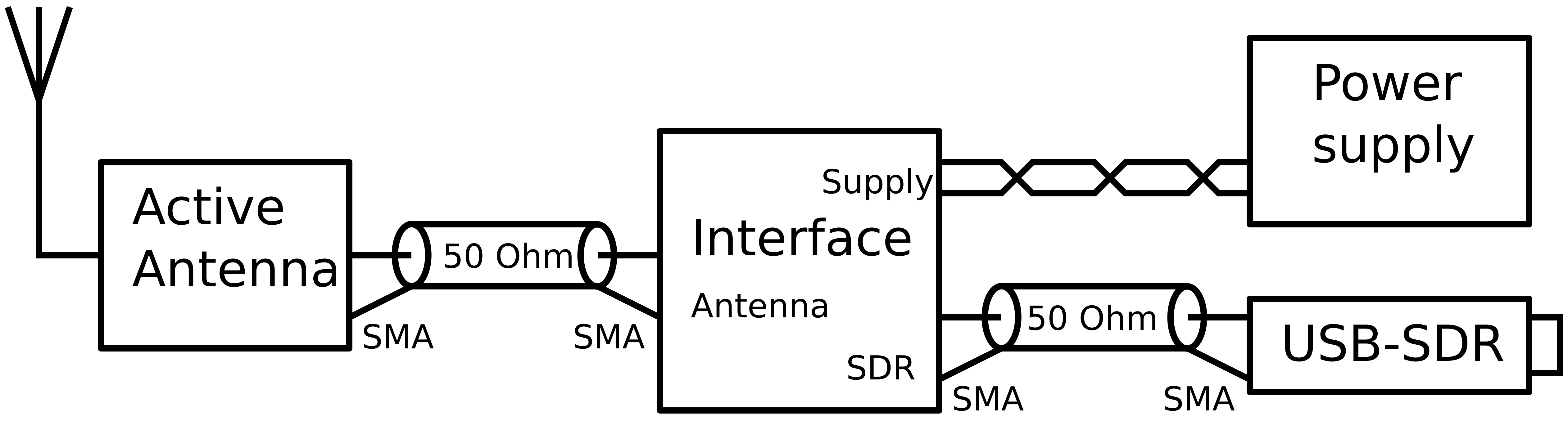

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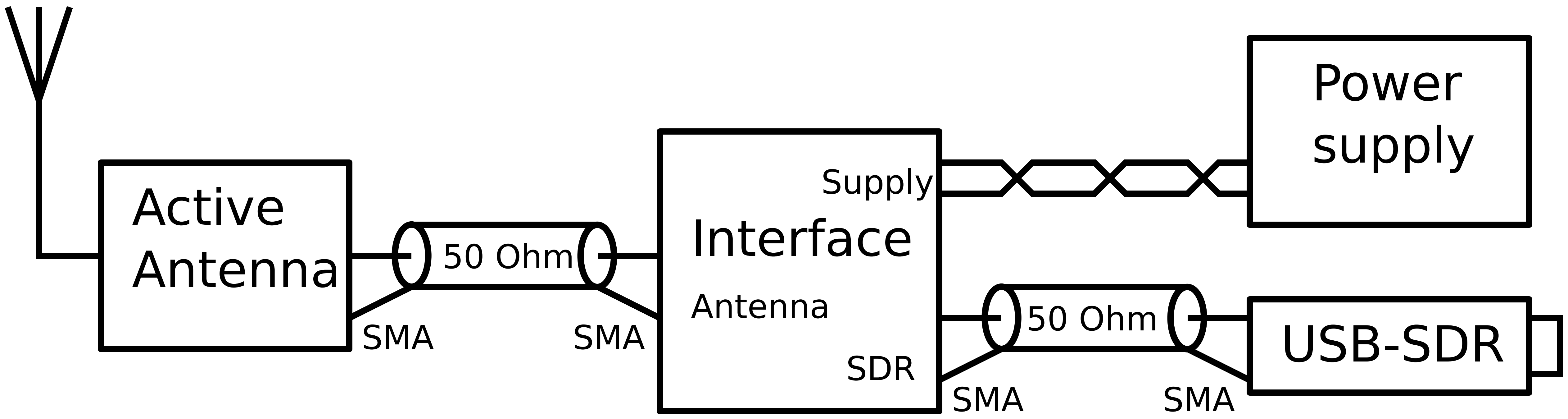

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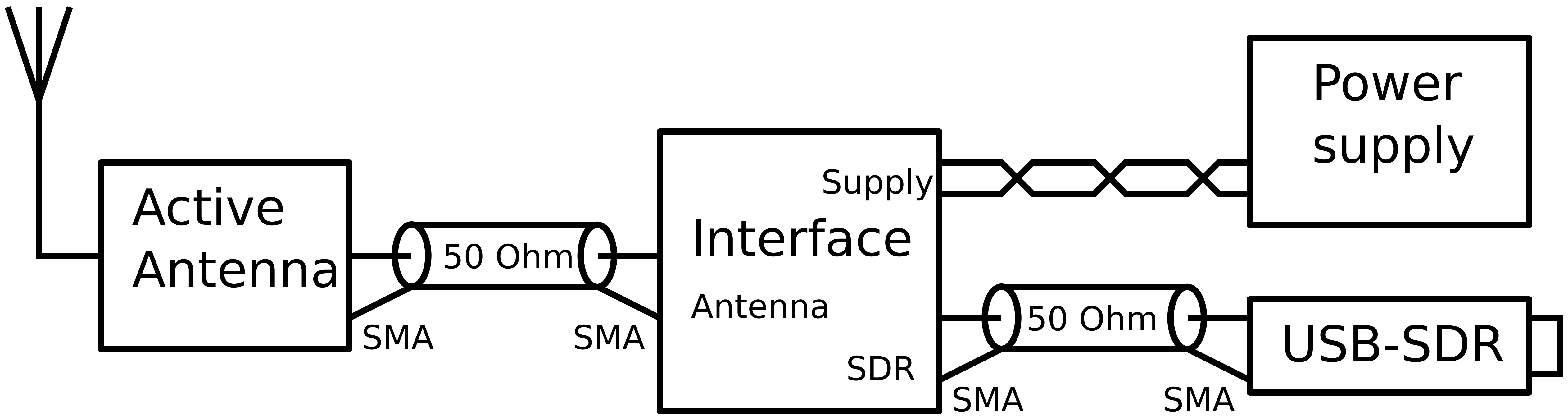

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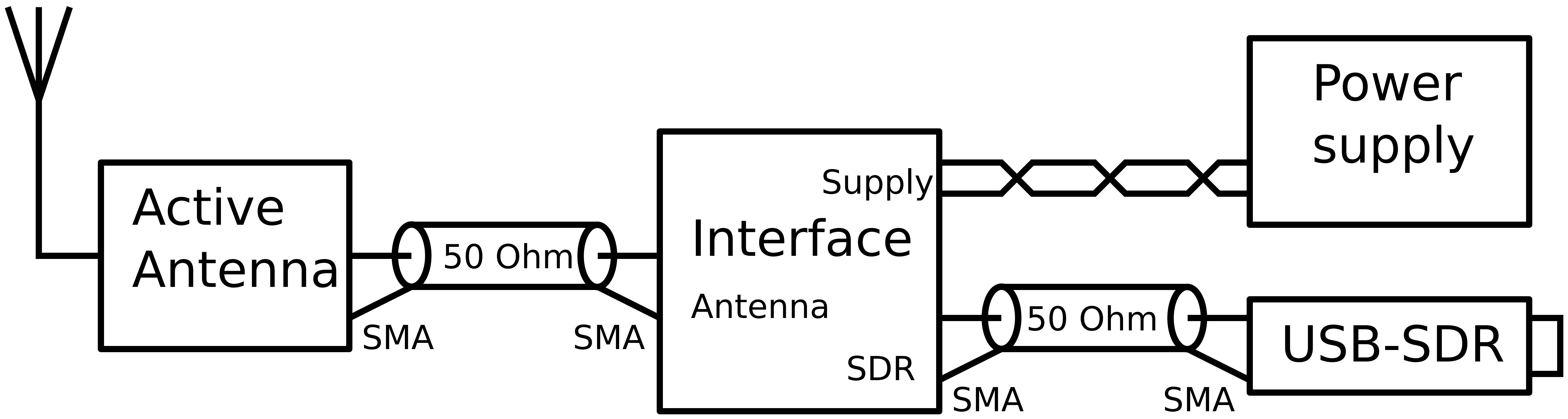
Temperature range



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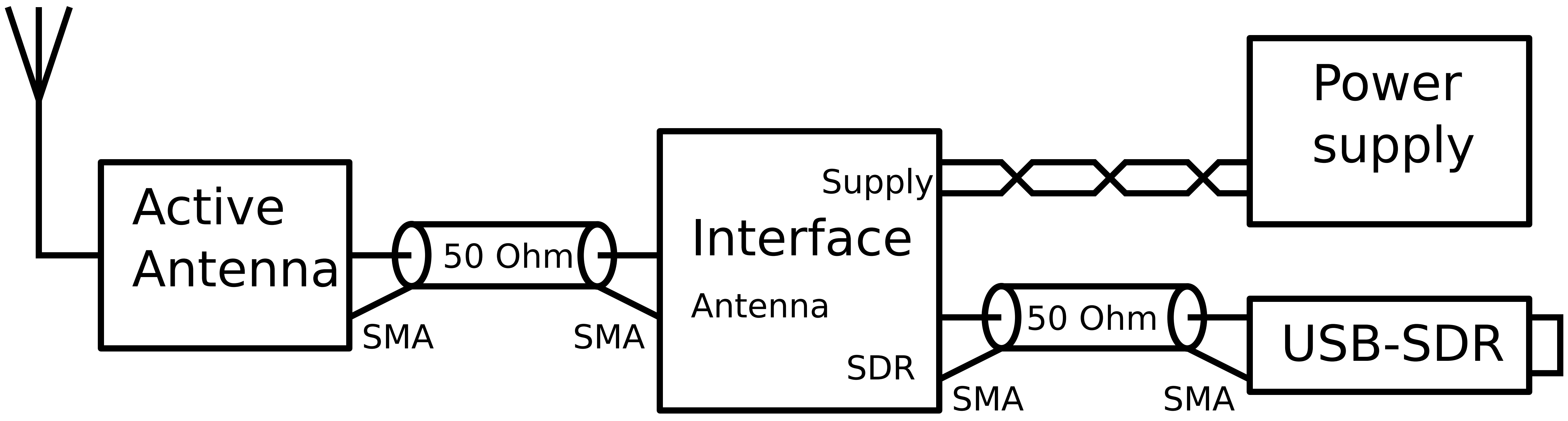

Performance	**Costs**	**Operating conditions**
Maximum RMS input signal	Antenne length	Temperature range
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Antenna referred noise	Power consumption	ESD
Output impedance	Dimensions	
Frequency range of interest	Technology	
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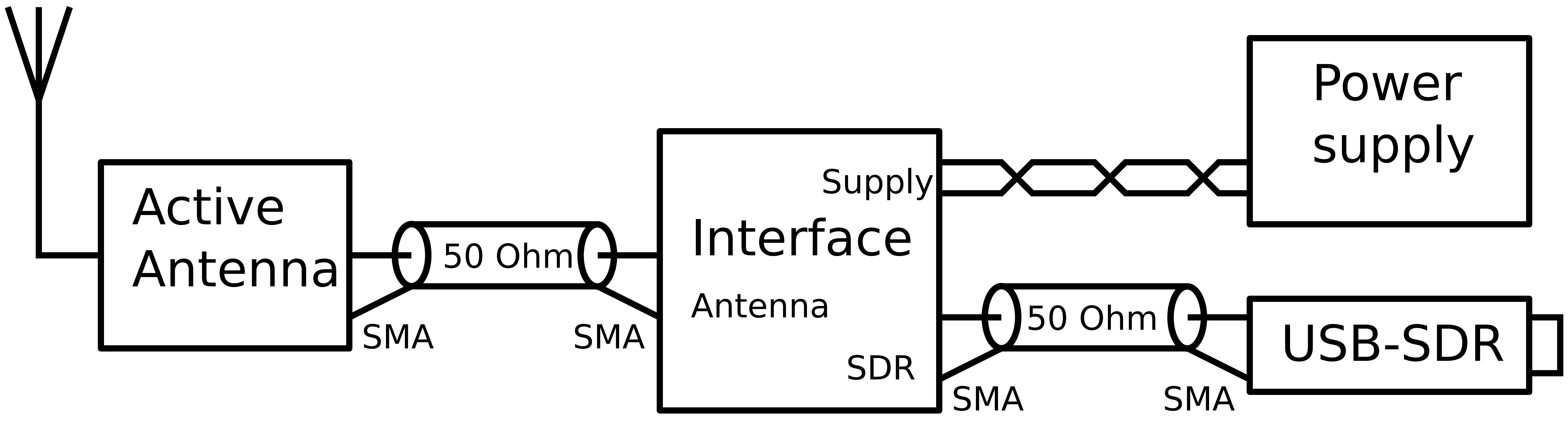
IMD	Package	



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Operating conditions

Temperature range

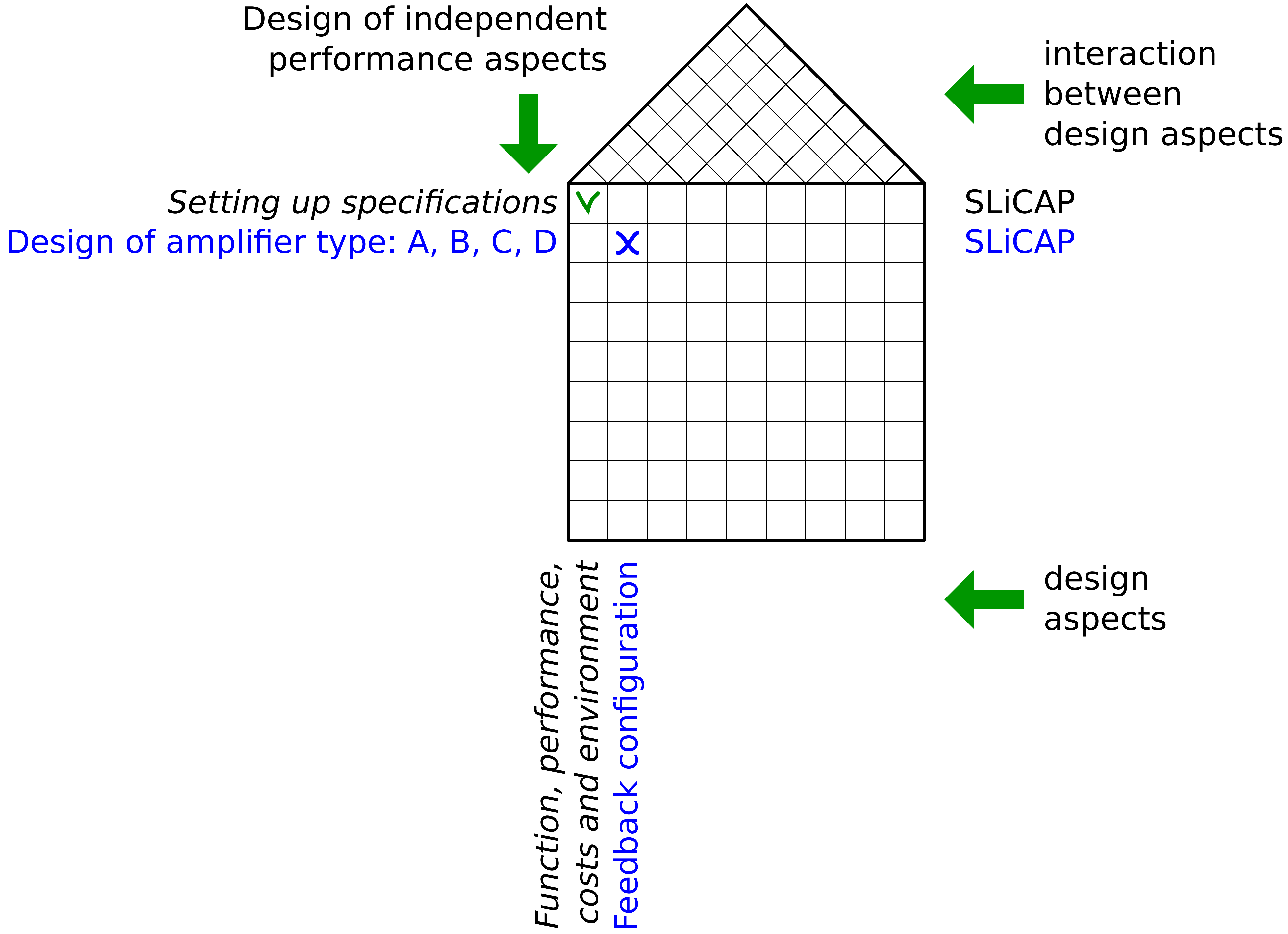
EMI

ESD

Structured Electronic Design

Step 2
Design of the amplifier type

Anton J.M. Montagne


Design of independent
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interaction
between
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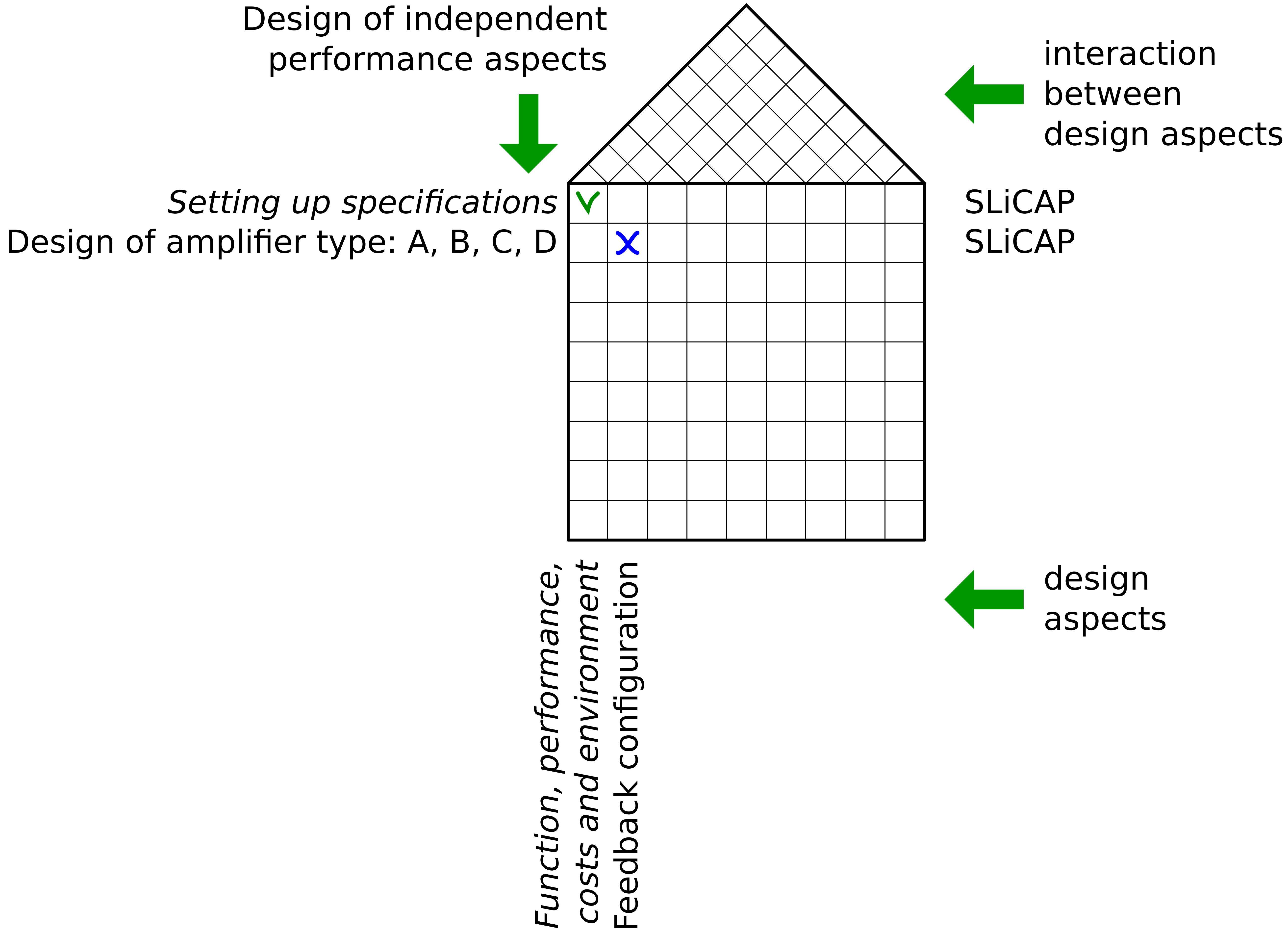
Setting up specifications
Design of amplifier type: A, B, C, D
SLiCAP
SLiCAP
design
aspects
Function, performance,
costs and environment
Feedback configuration

Negative feedback amplifiers generally outperform non-feedback amplifiers



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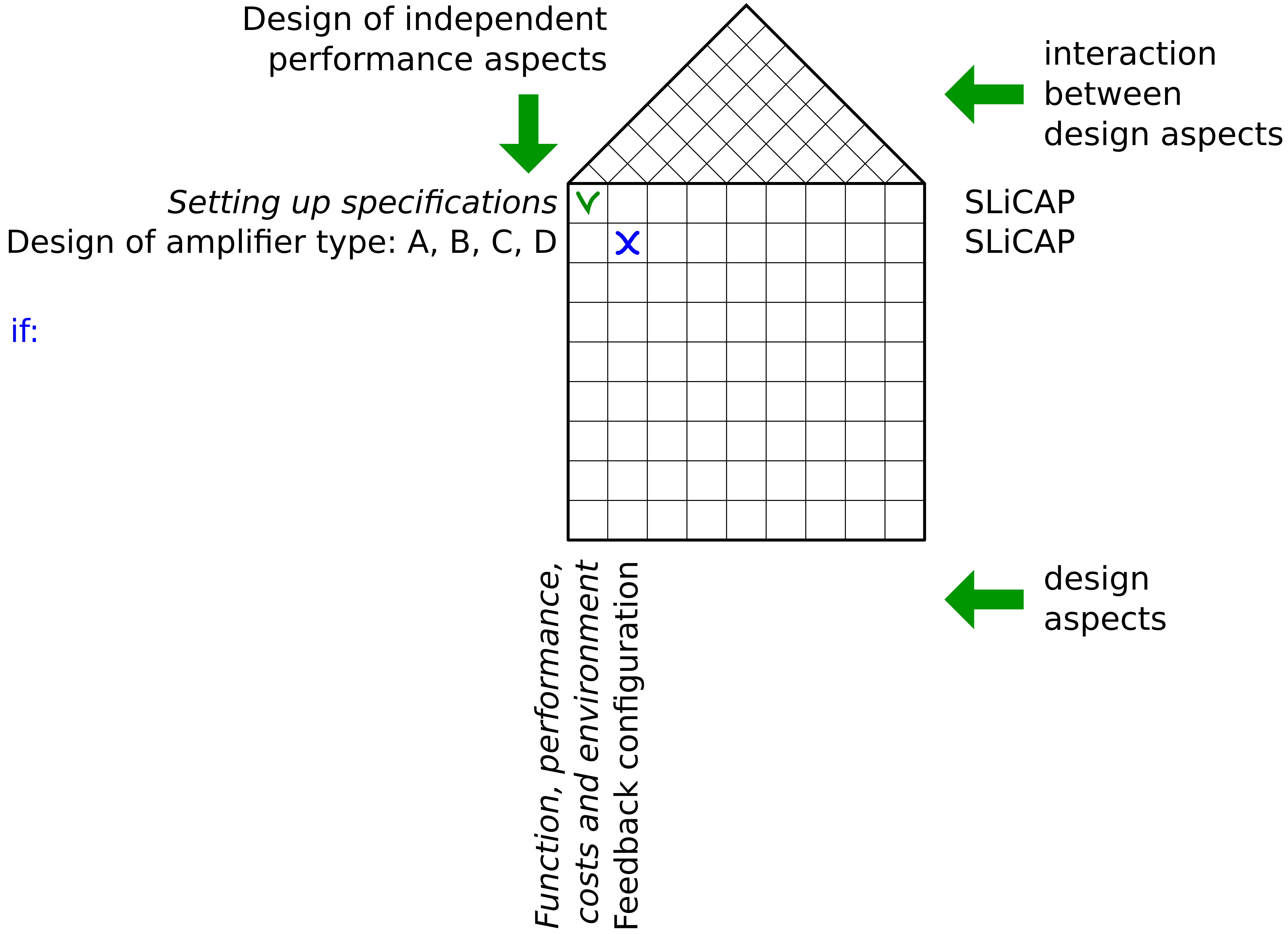

Negative feedback can be applied if:

Negative feedback amplifiers generally outperform non-feedback amplifiers

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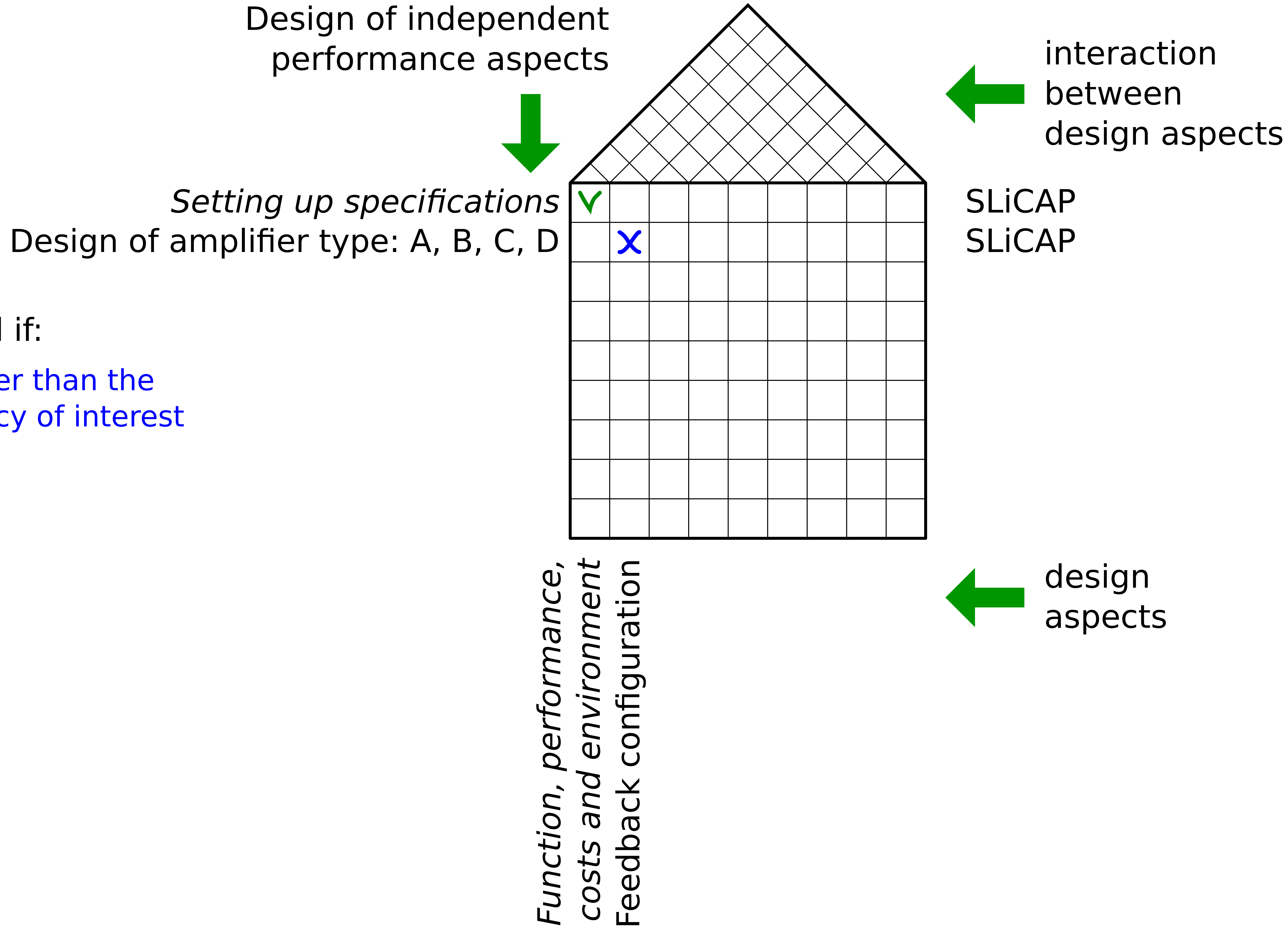
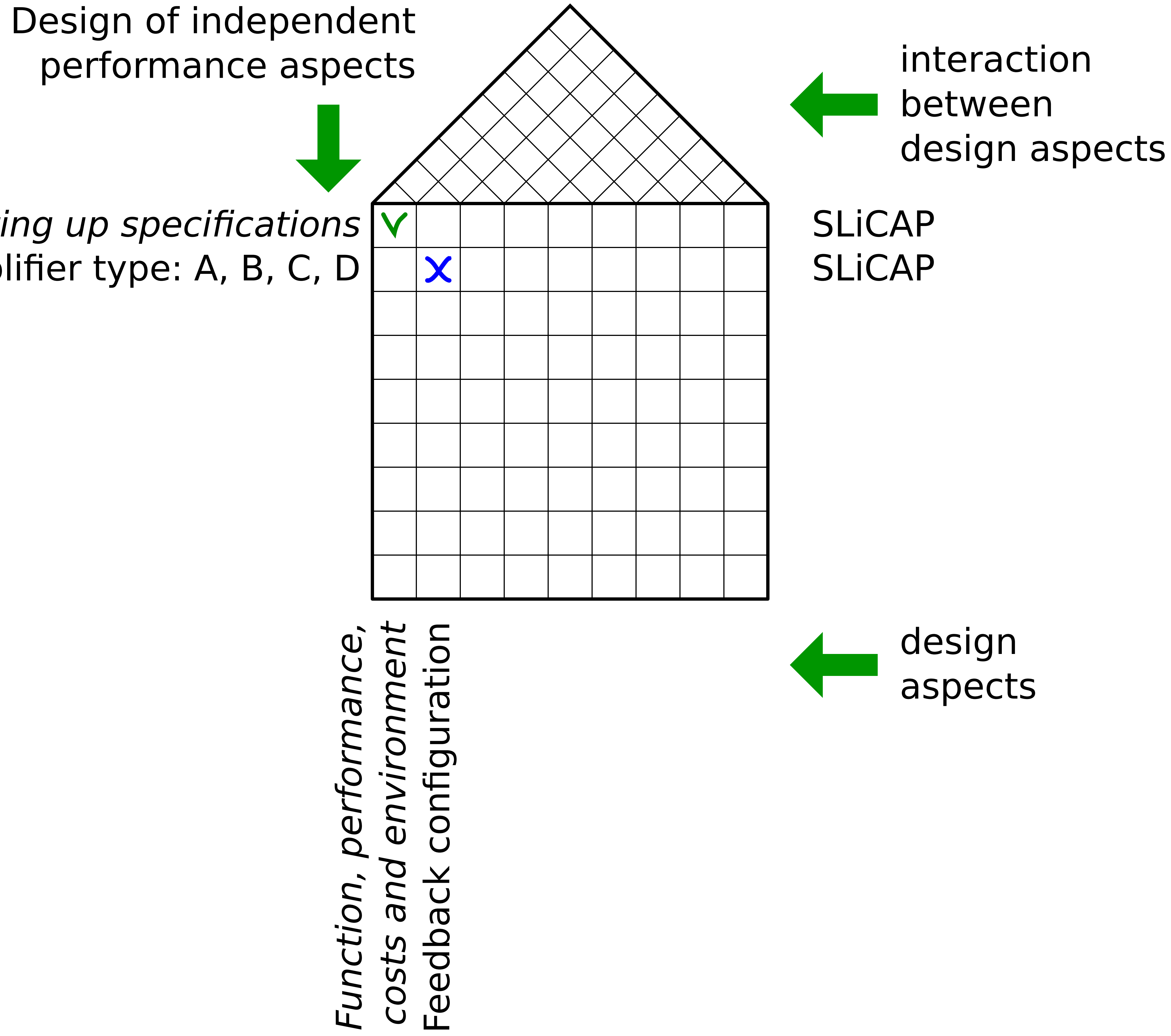
Circuit dimensions are much smaller than the wavelength of the highest frequency of interest



Negative feedback amplifiers generally outperform non-feedback amplifiers

Negative feedback can be applied if:

- Circuit dimensions are much smaller than the wavelength of the highest frequency of interest
- Process cut-off frequency is much larger than the highest frequency of interest



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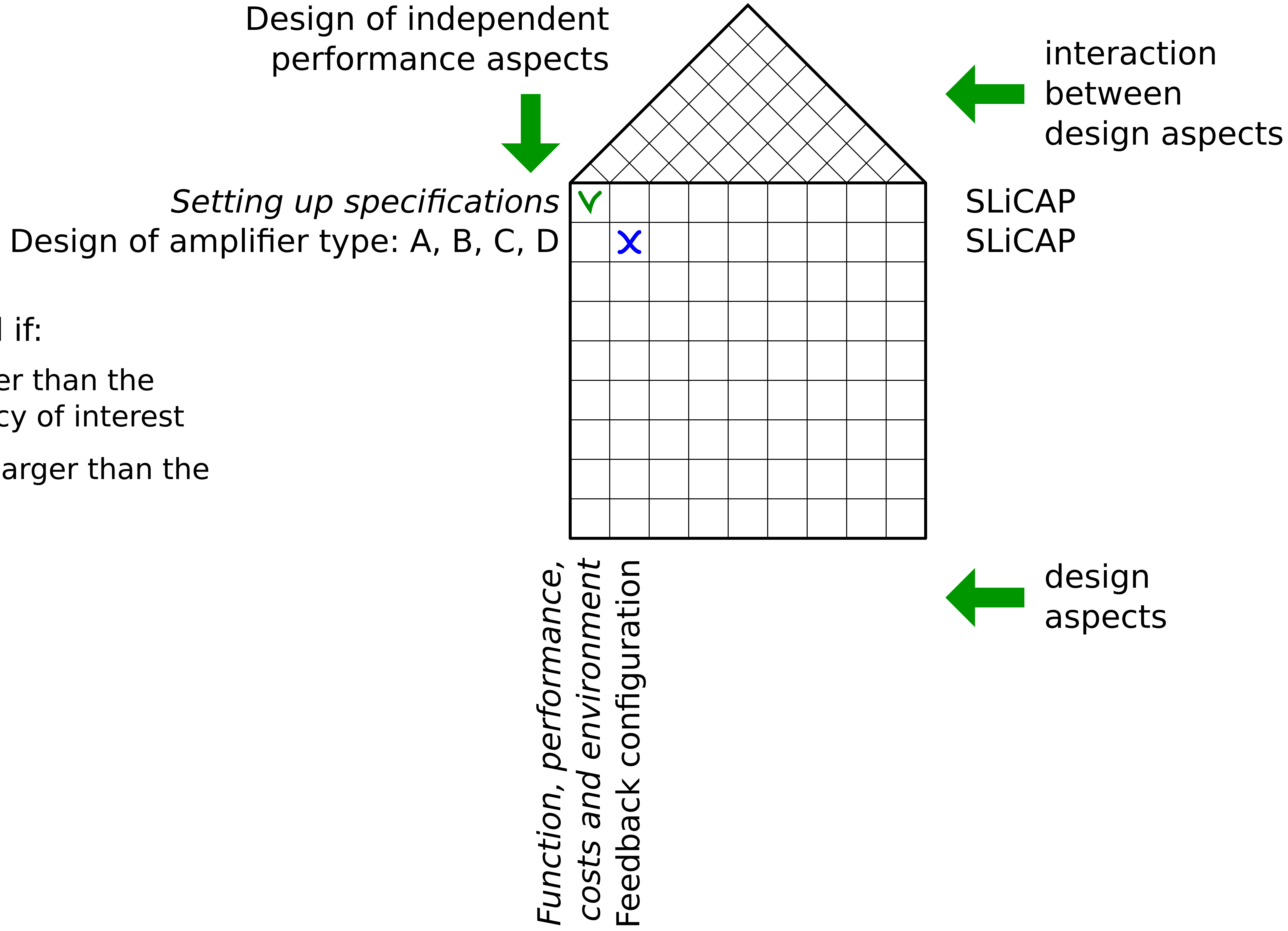

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Design of the active antenna:

Negative feedback amplifiers generally outperform non-feedback amplifiers

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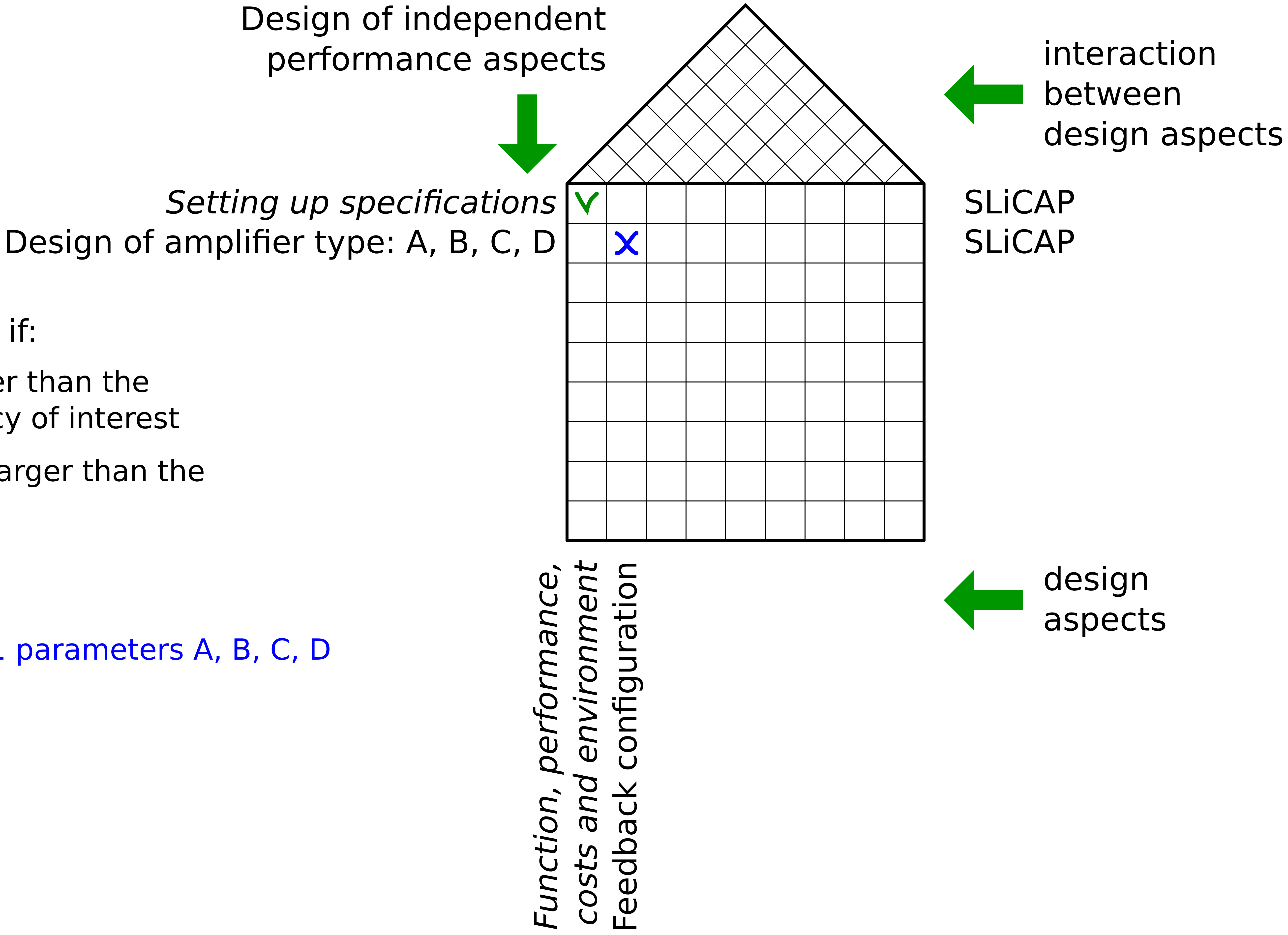
- Circuit dimensions are much smaller than the wavelength of the highest frequency of interest
- Process cut-off frequency is much larger than the highest frequency of interest

Design of the active antenna:

- Determine valid combinations of T1 parameters A, B, C, D



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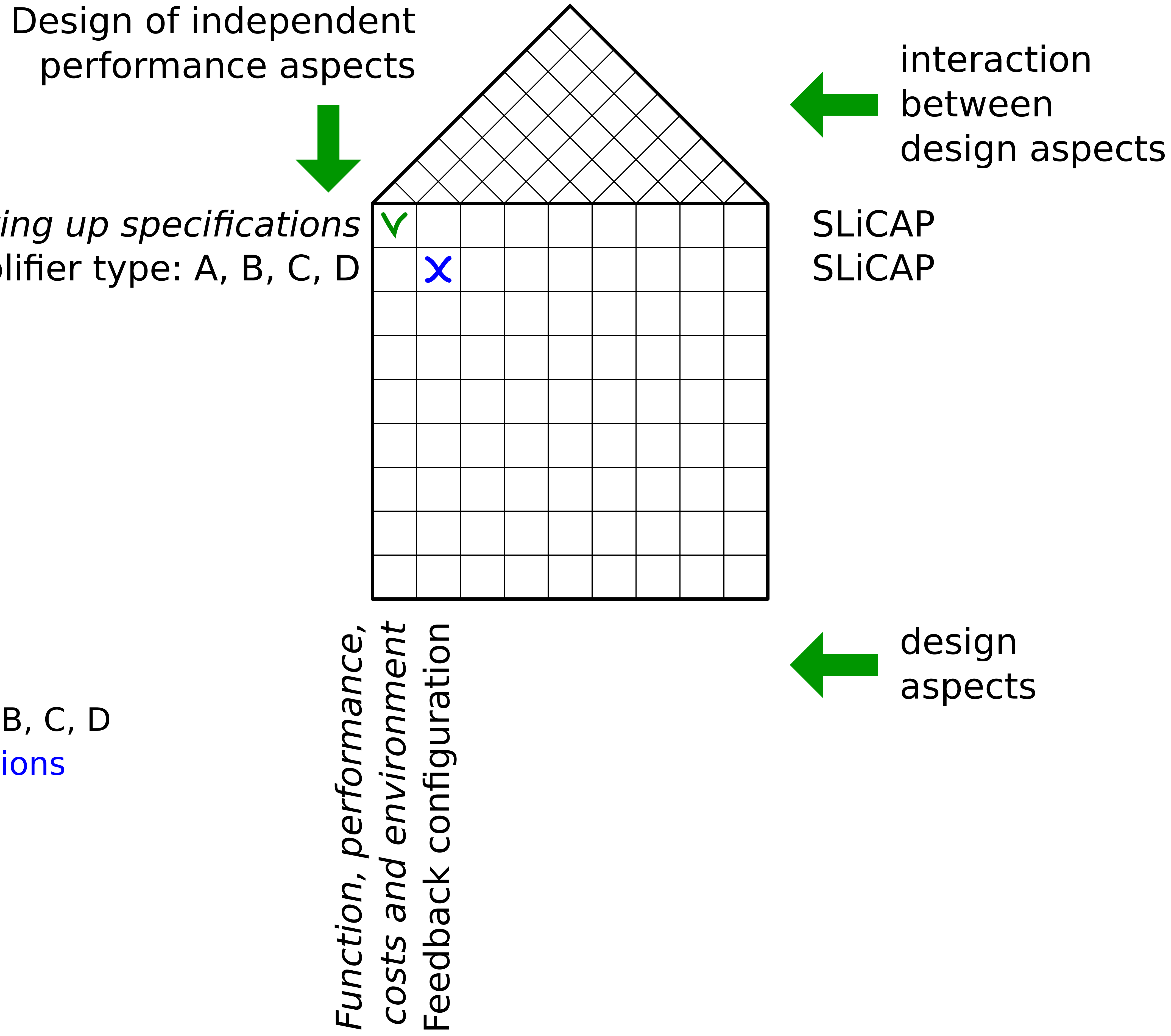

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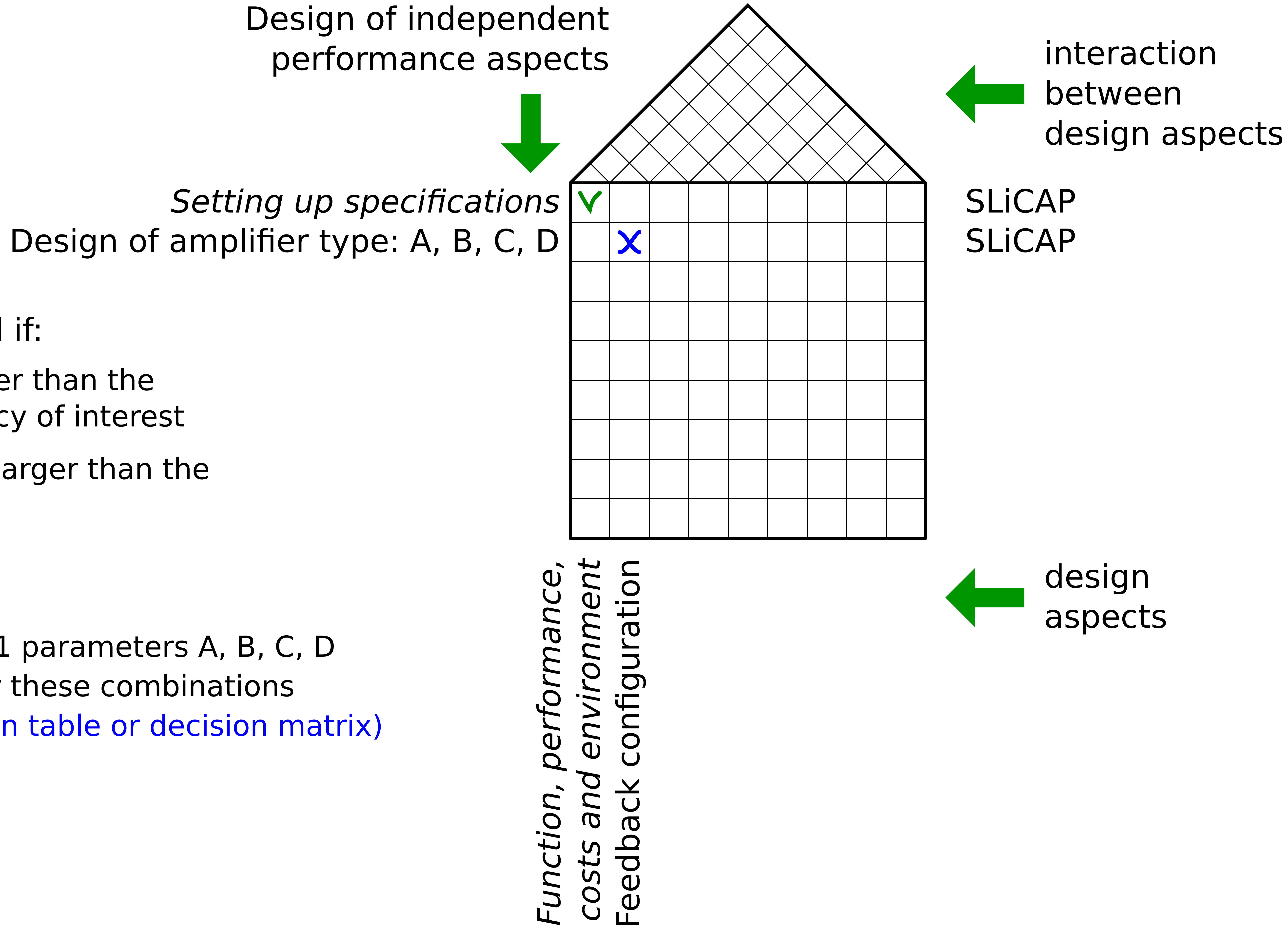


Negative feedback amplifiers generally outperform non-feedback amplifiers

Design of independent performance aspects

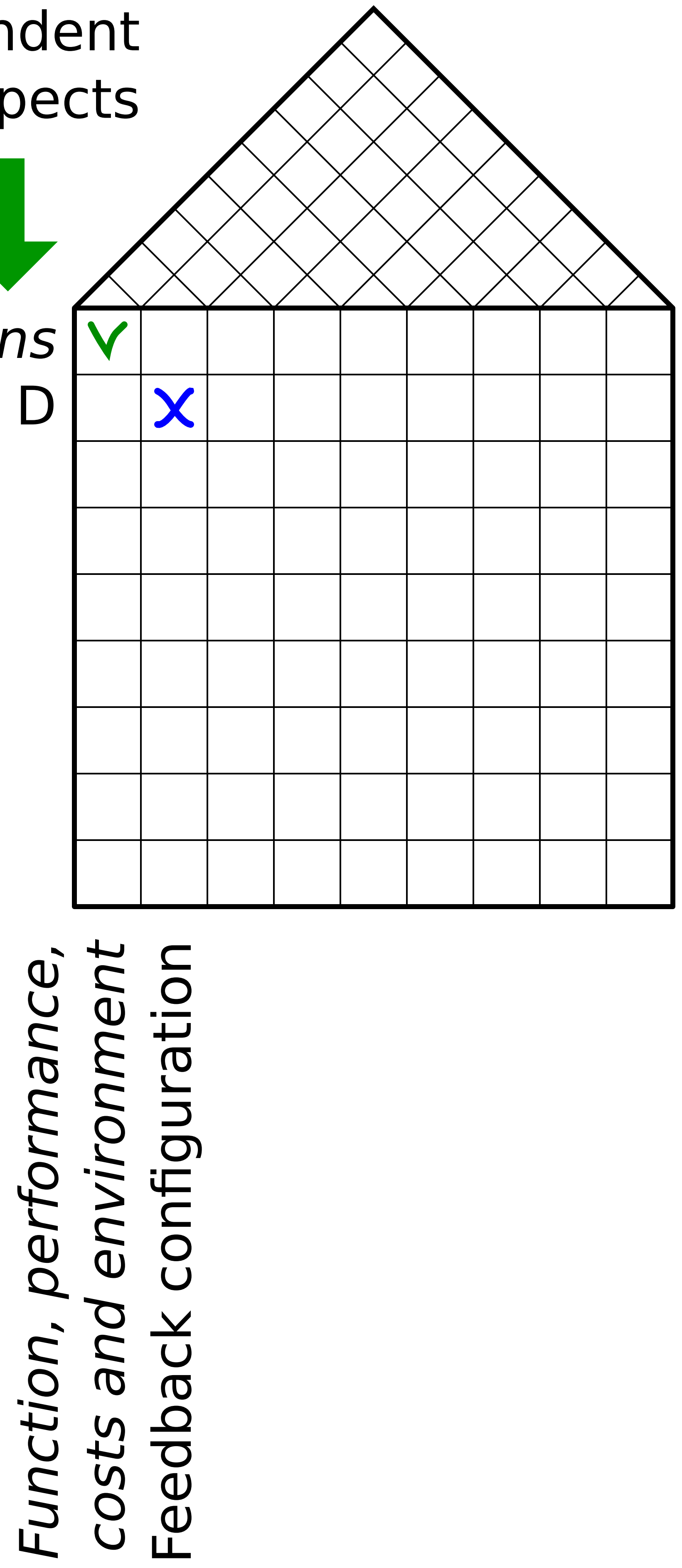
interaction between design aspects

Setting up specifications

Design of amplifier type: A, B, C, D

SLiCAP

SLiCAP



design aspects

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Design studies
level fo detailing
depends on experience

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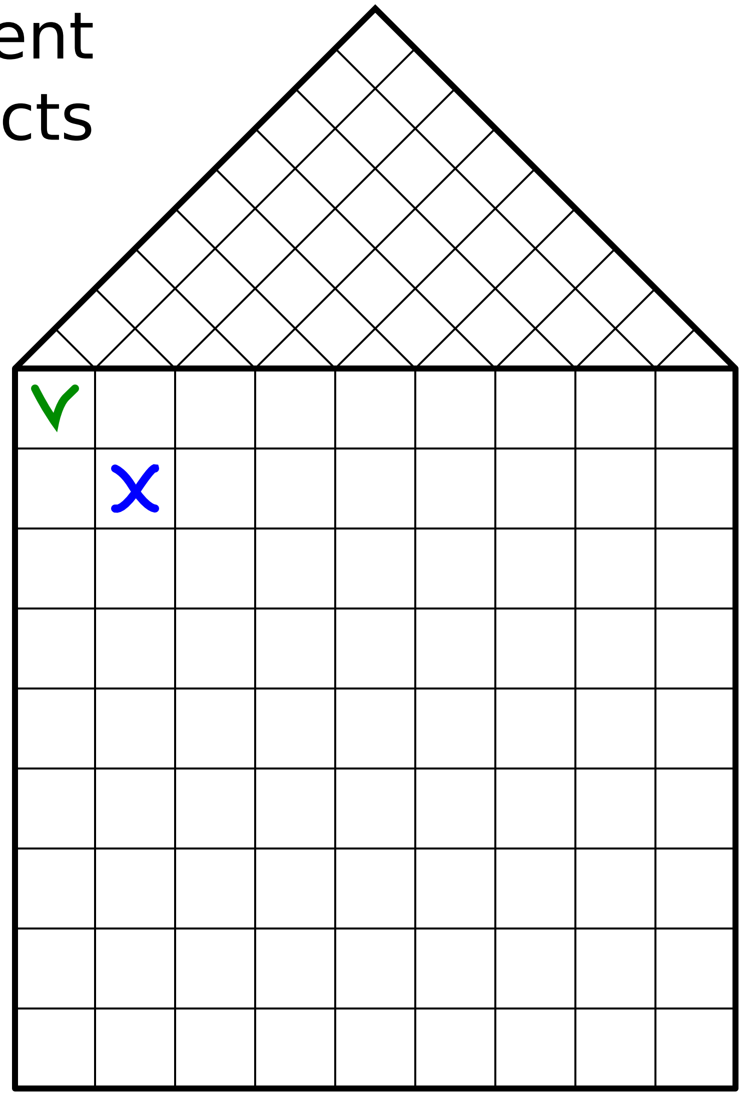

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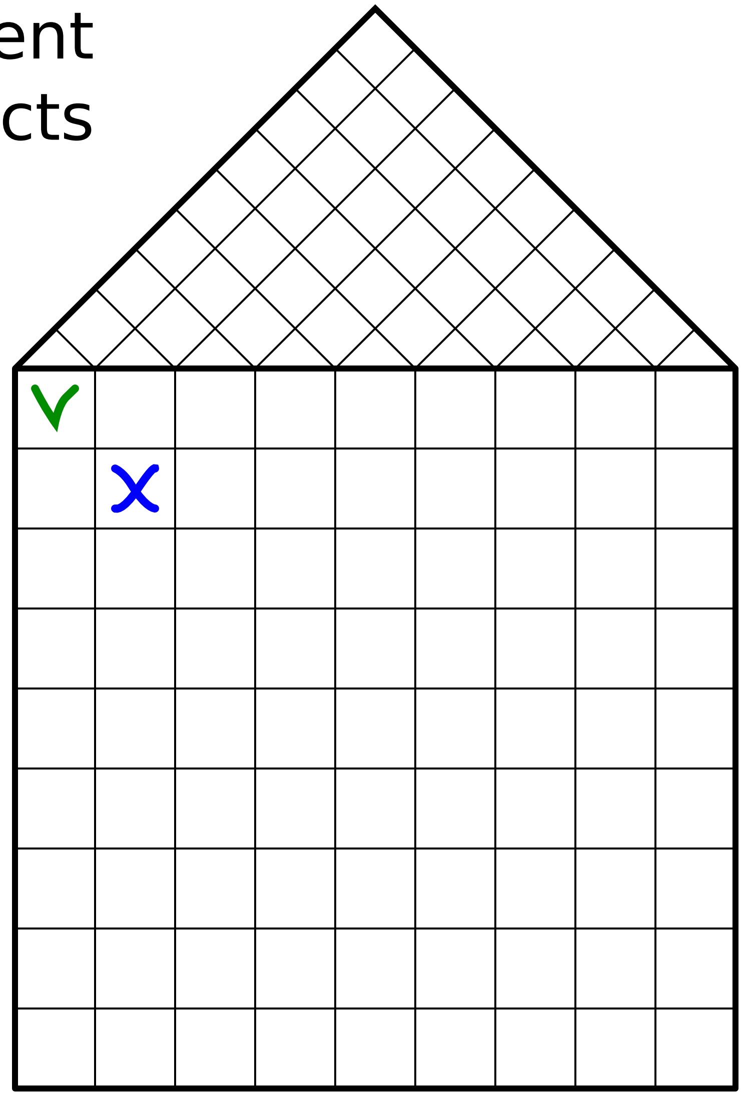

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Result is a functional design or concept design which is assumed feasible

Design studies
level fo detailing
depends on experience

Function, performance, costs and environment

Feedback configuration

design aspects

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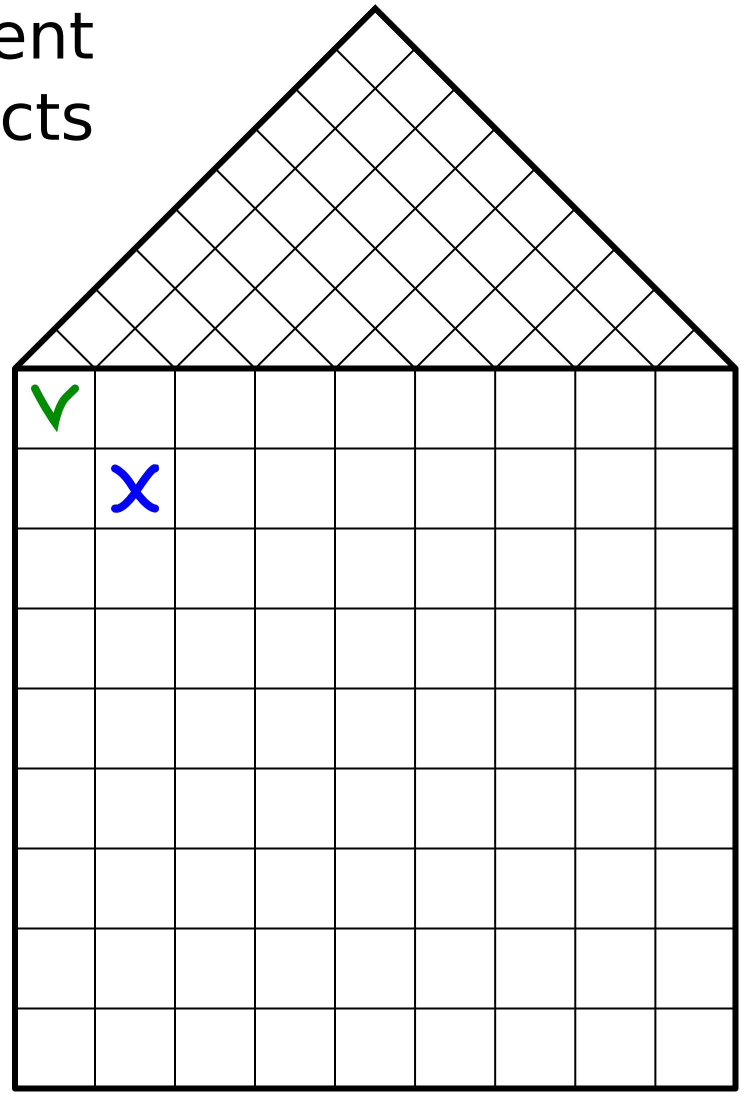
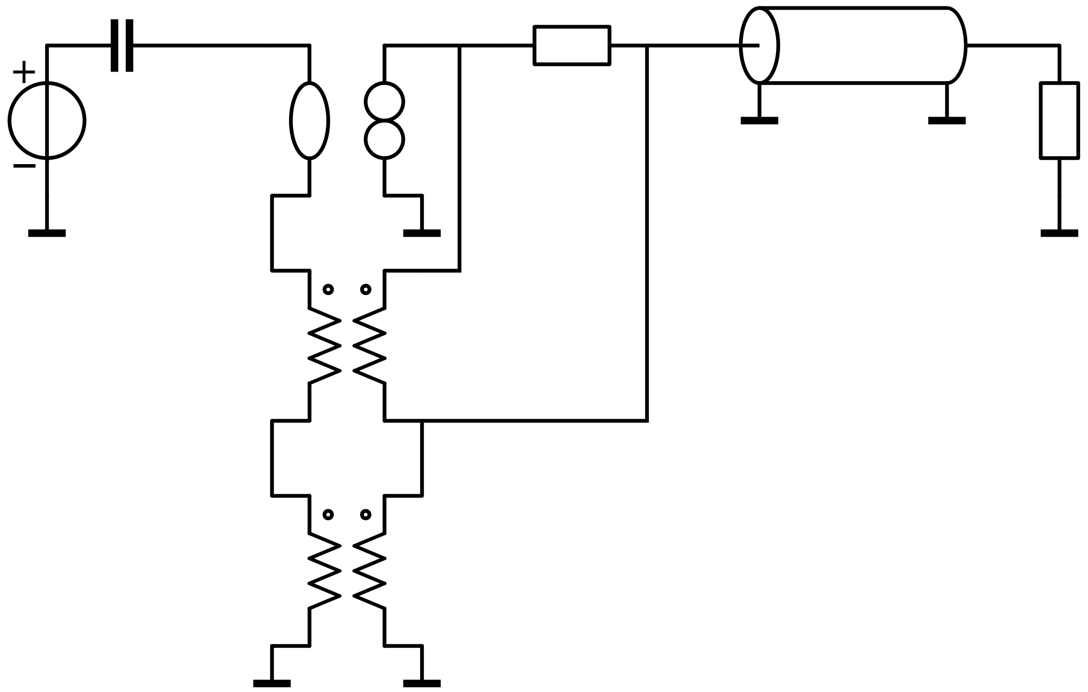


Active antenna configurations

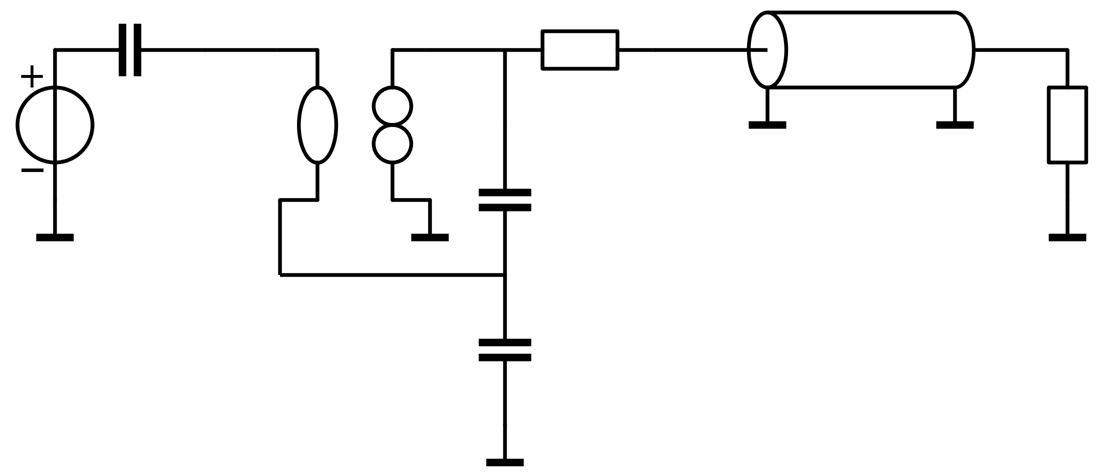
Active antenna configurations

A, B



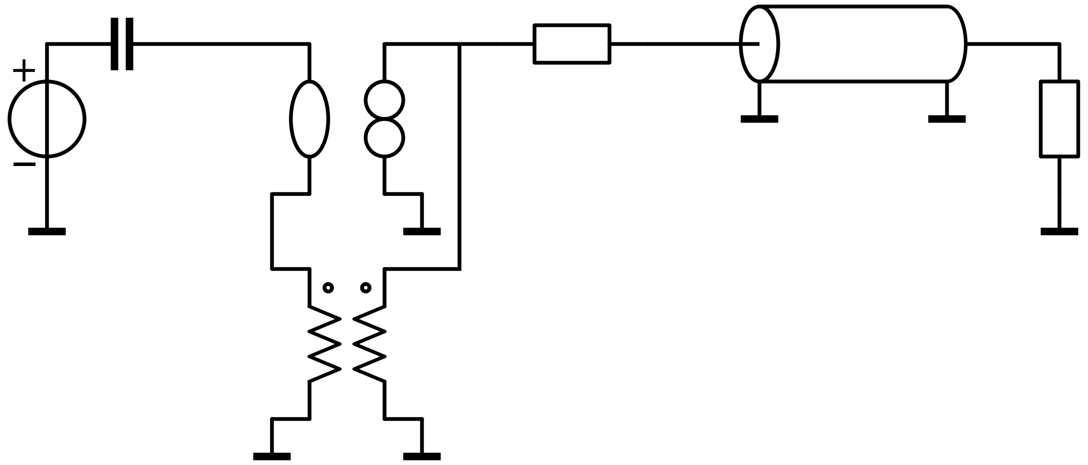
Active antenna configurations

A, B



Active antenna configurations

A, B



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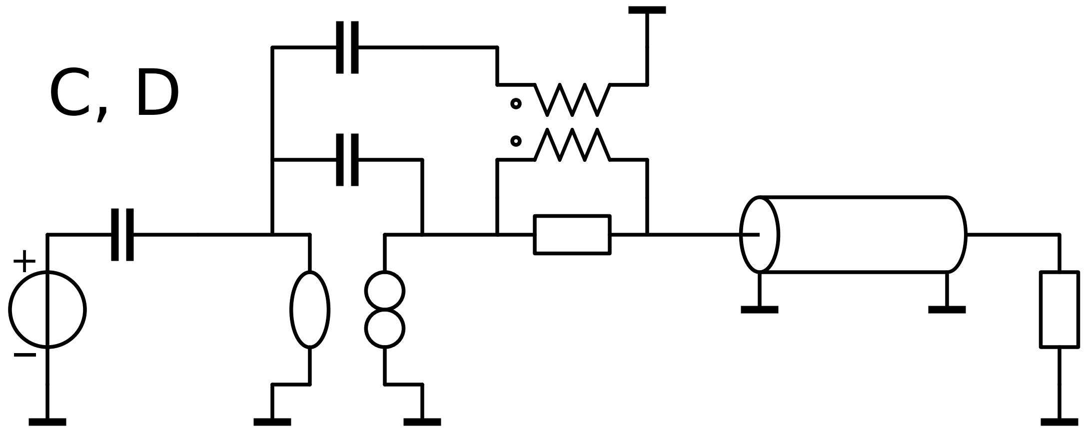
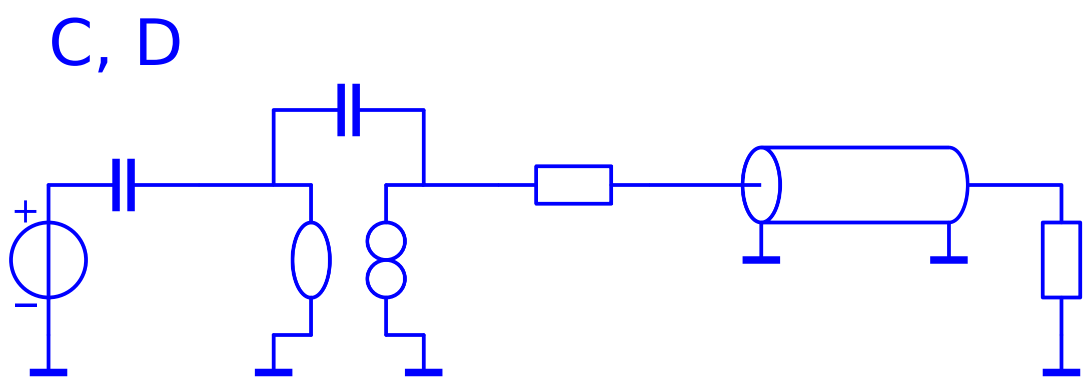
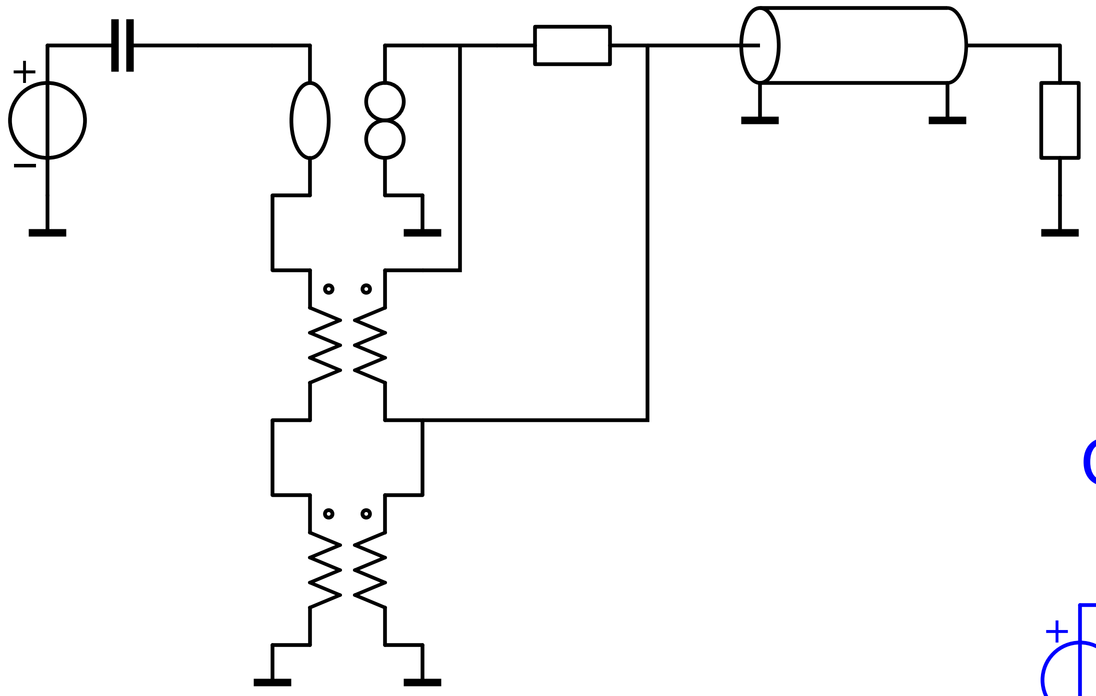


Active antenna configurations

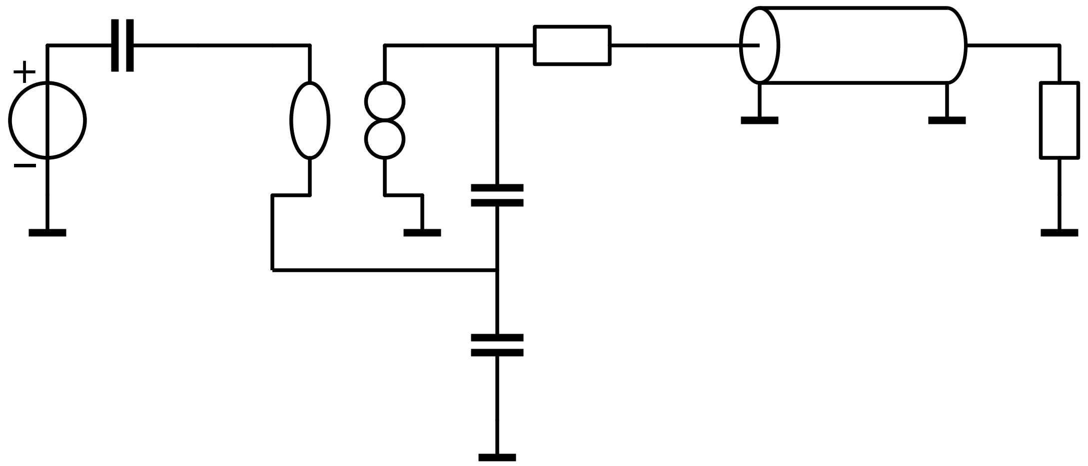


Active antenna configurations

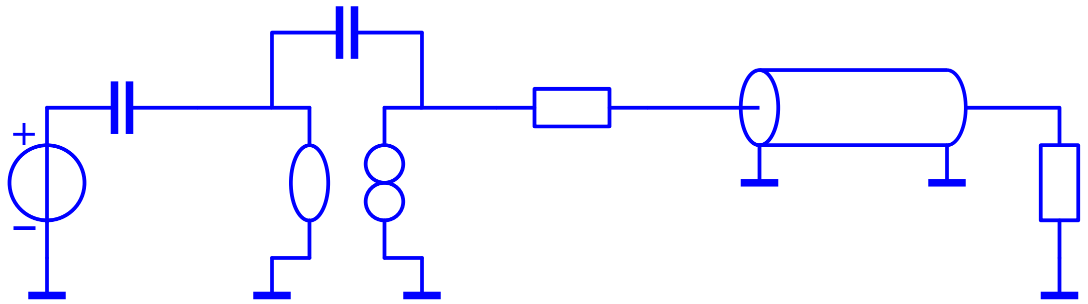
A, B



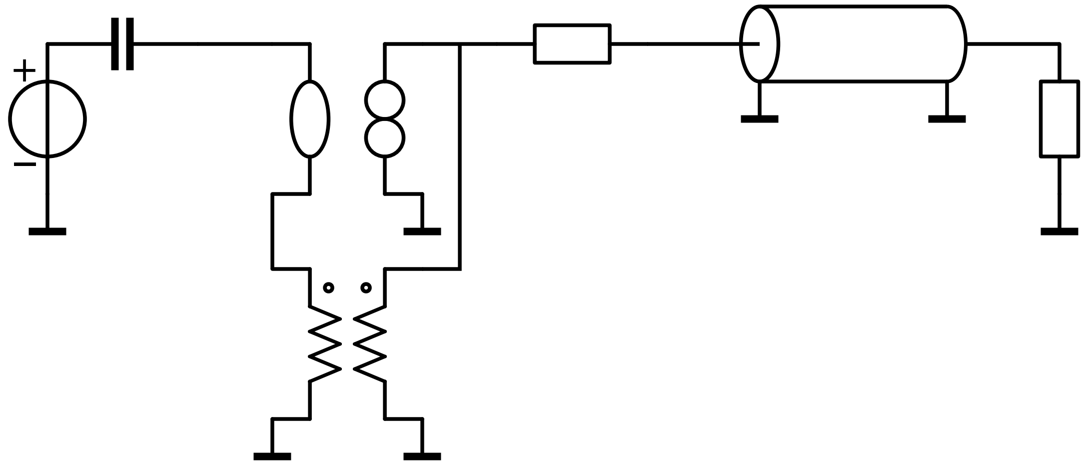
A, B



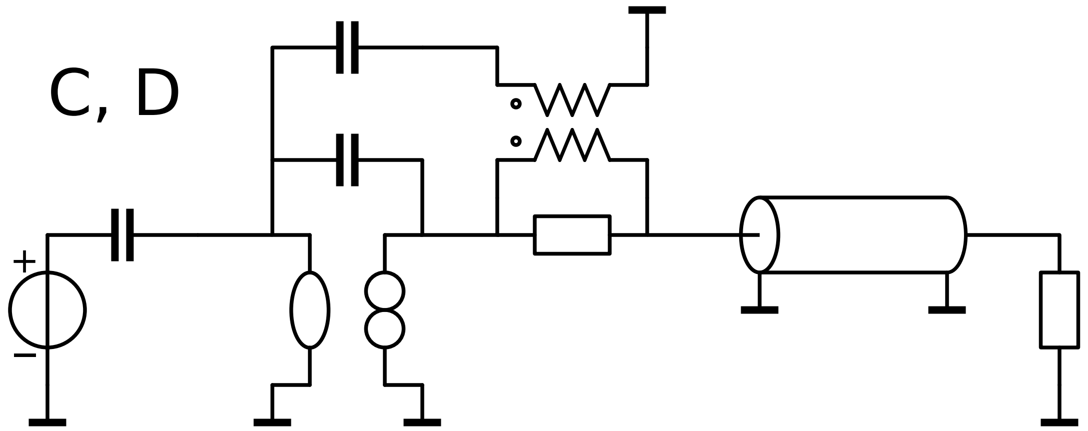
C, D



A, B



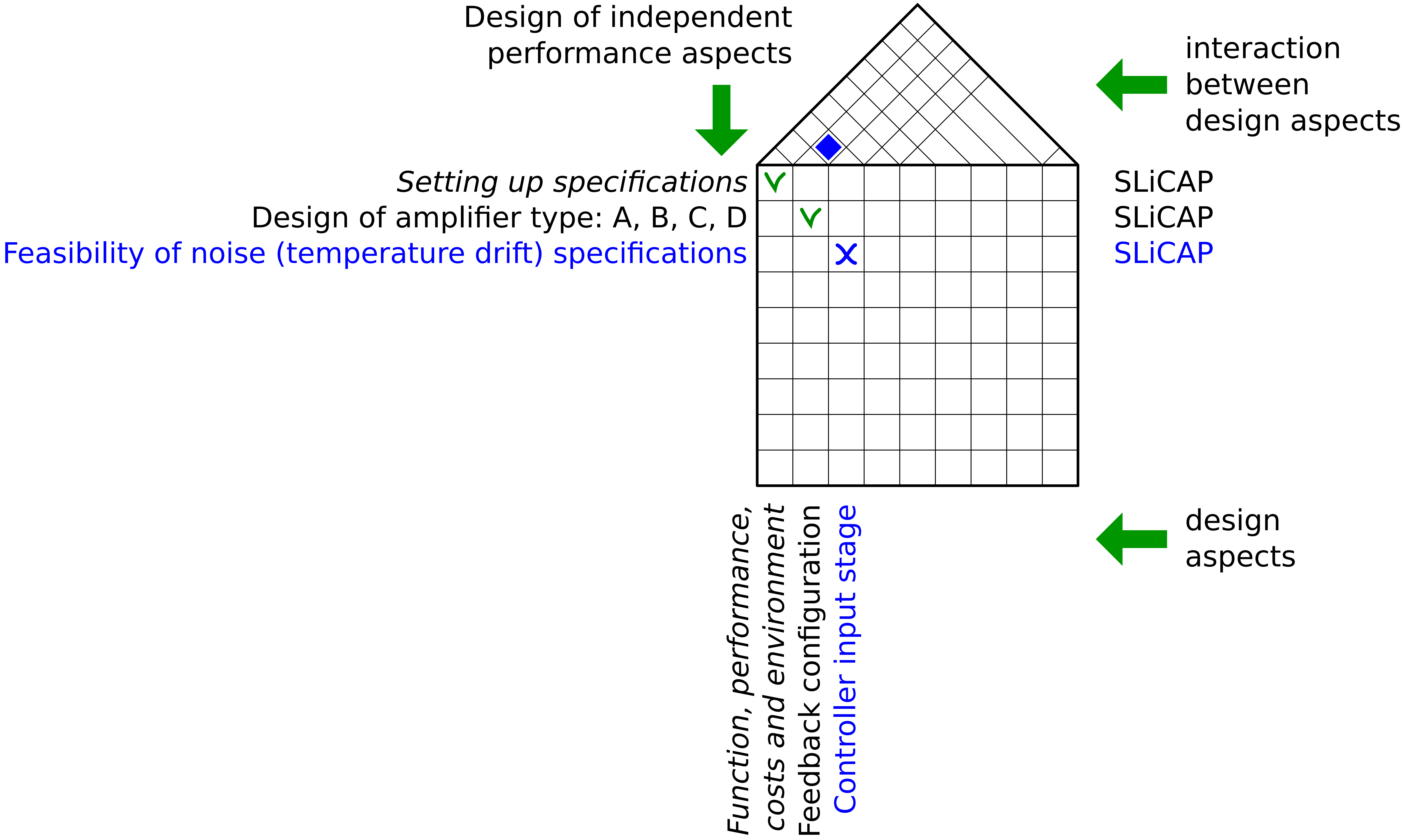
C, D



Structured Electronic Design

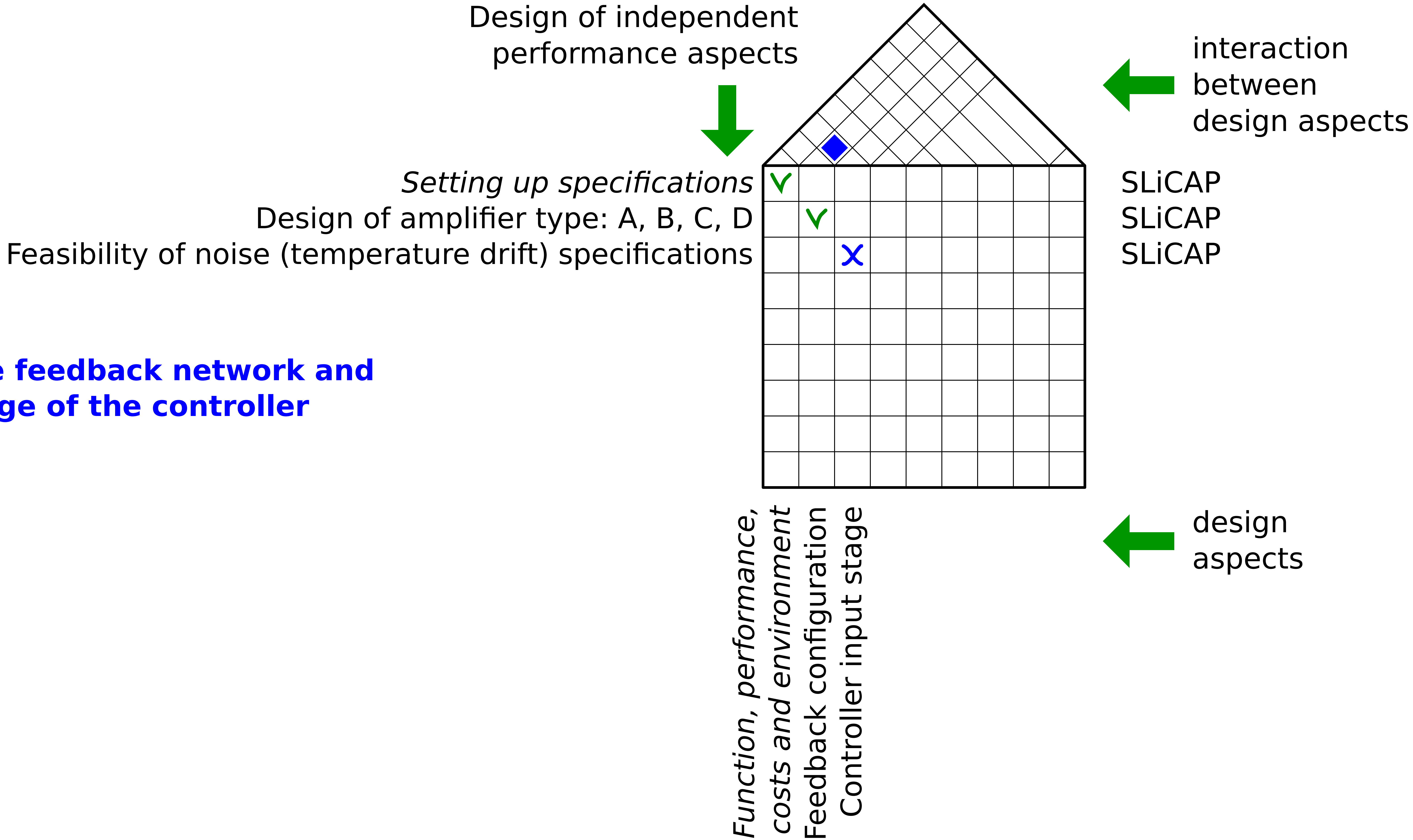
Step 3
Feasibility of the noise requirements

Anton J.M. Montagne



Design of independent
performance aspects
interaction
between
design aspects
Setting up specifications
Design of amplifier type: A, B, C, D
Feasibility of noise (temperature drift) specifications
SLiCAP
SLiCAP
SLiCAP
design
aspects
Function, performance, costs and environment
Feedback configuration
Controller input stage

Design of the feedback network and the input stage of the controller



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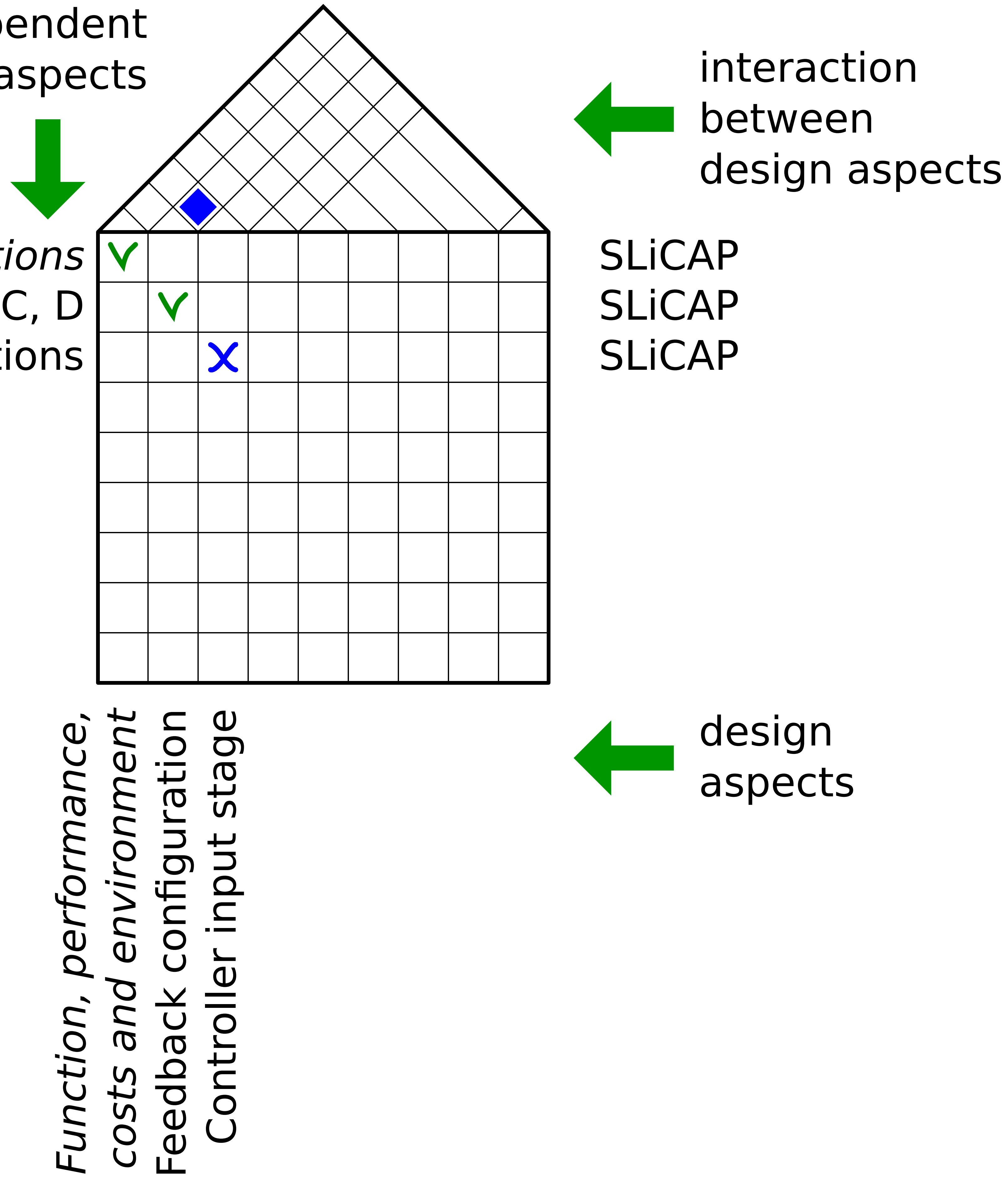
If the frequency range of temperature variations overlaps with that of the signal, equivalent input offset and bias variations have to be considered as input noise sources.



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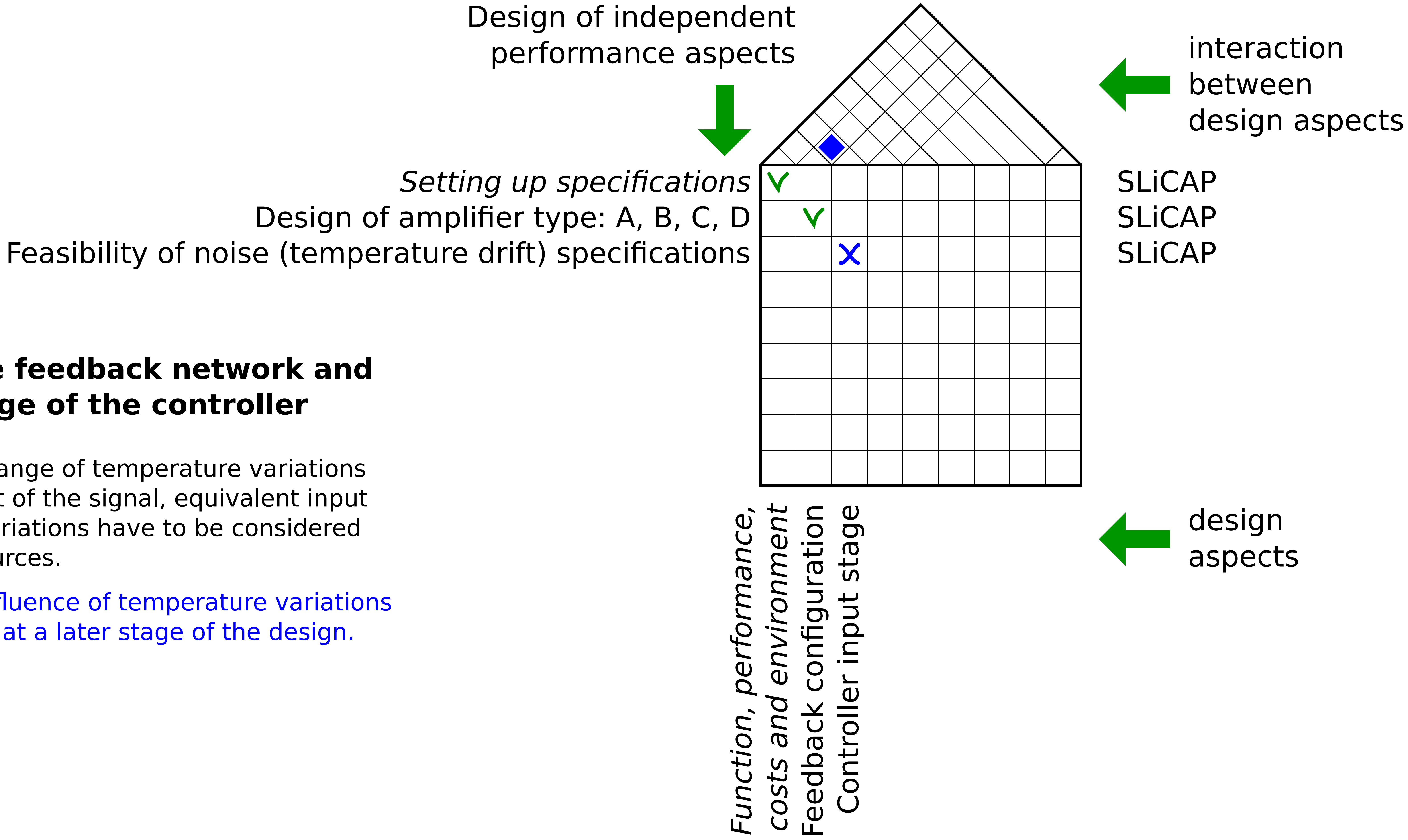

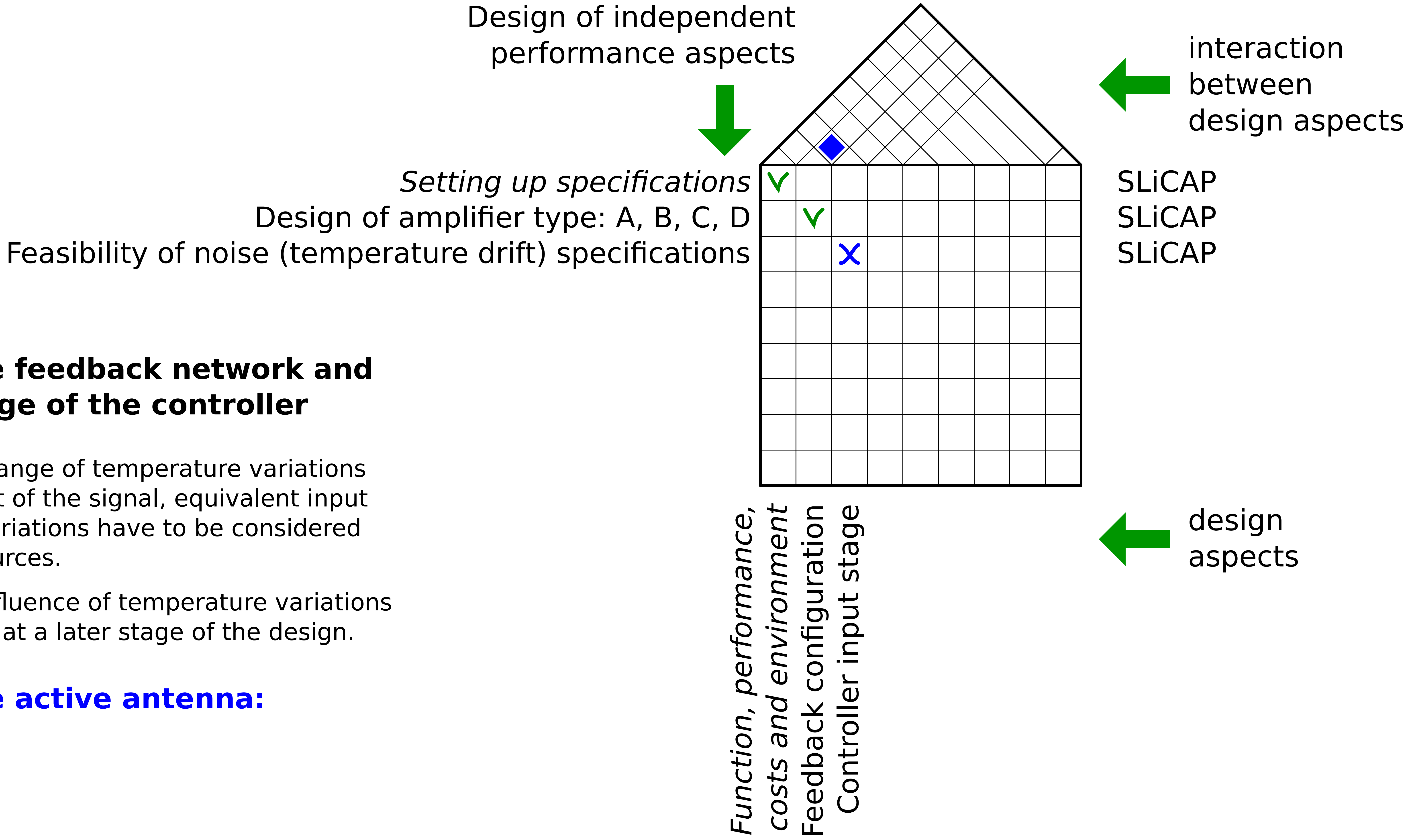

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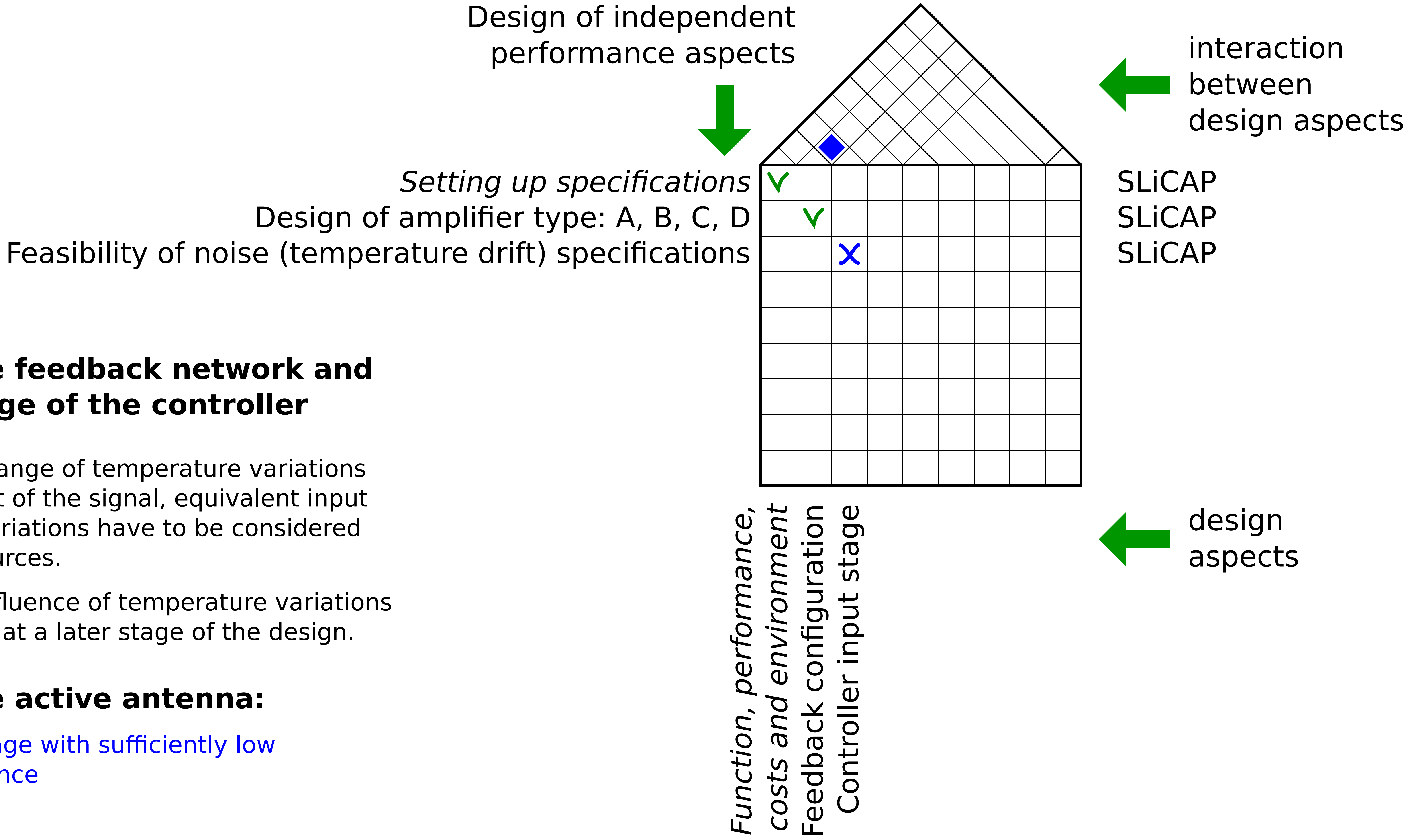

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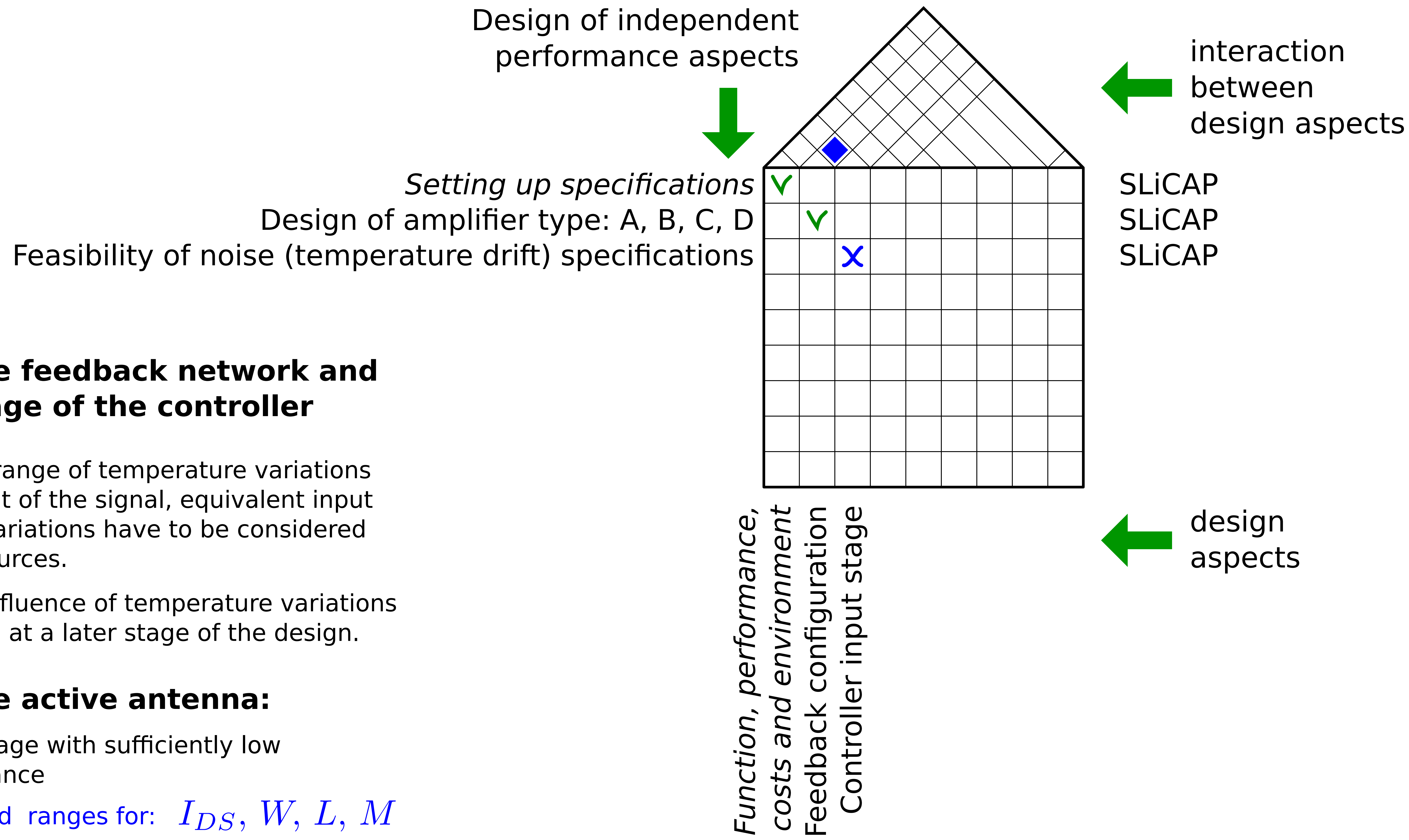
Design of the active antenna:

Design a CS stage with sufficiently low noise performance



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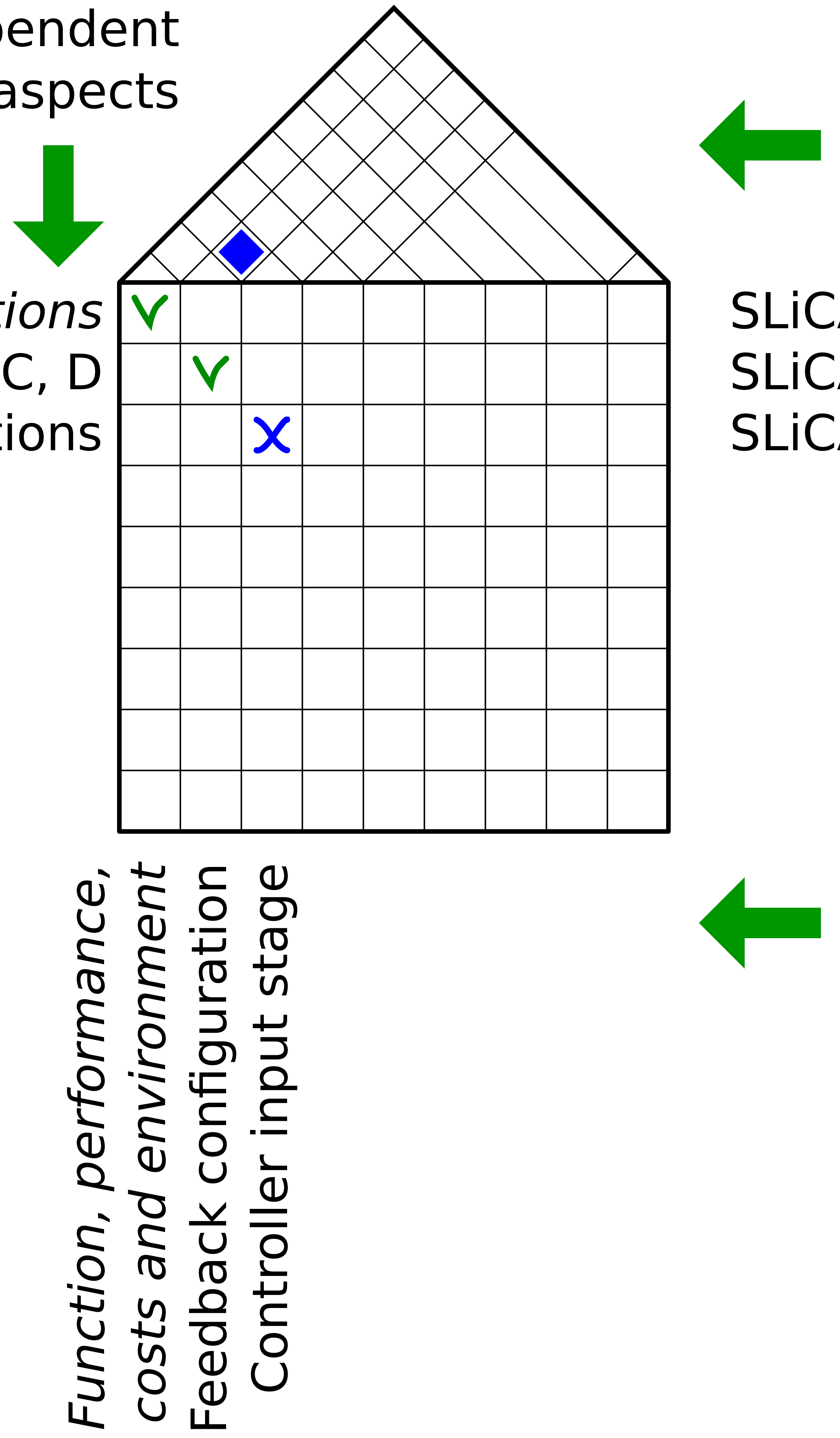
Determine valid ranges for: I_{DS}, W, L, M



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CS input stage design

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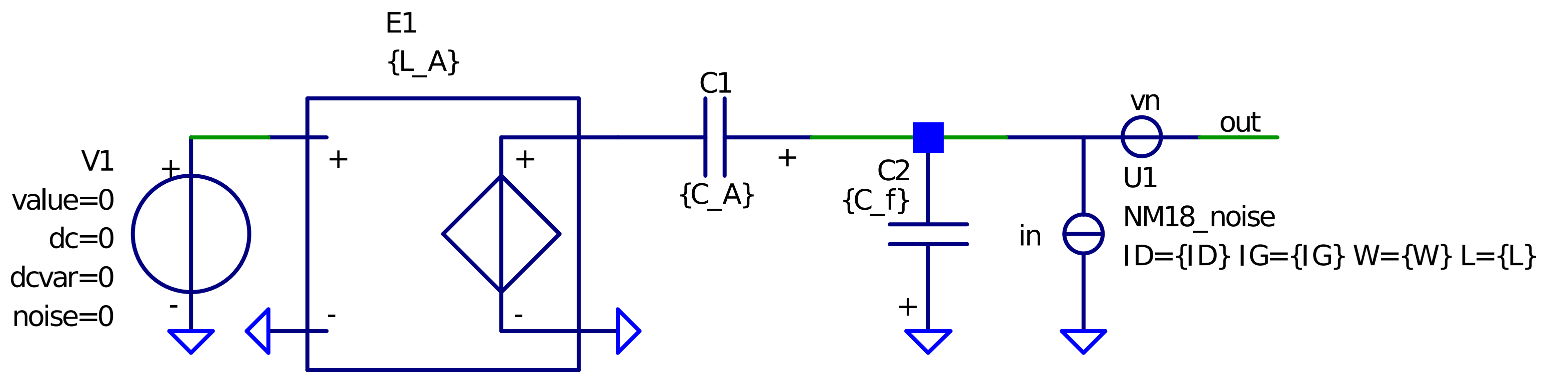

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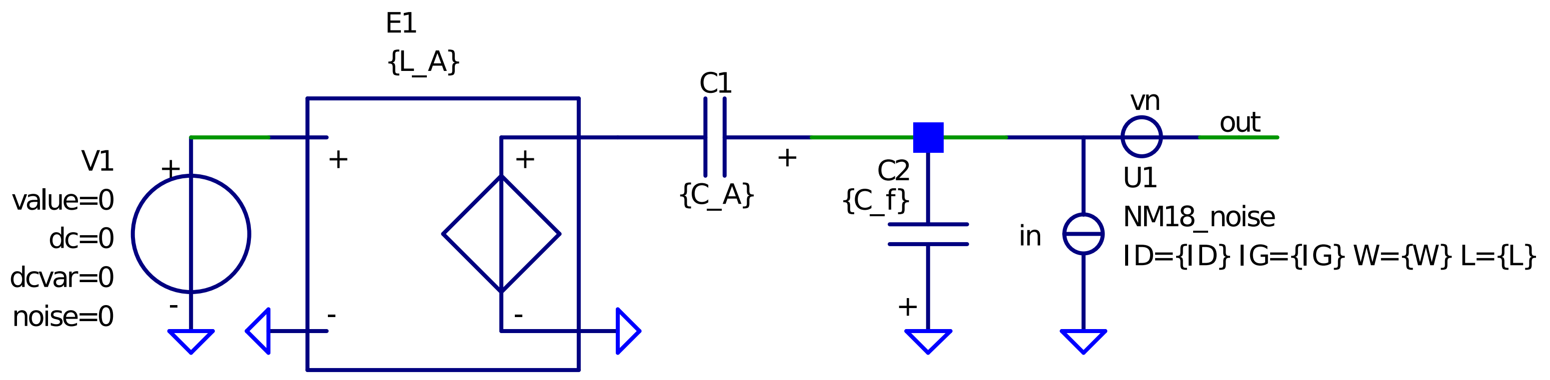
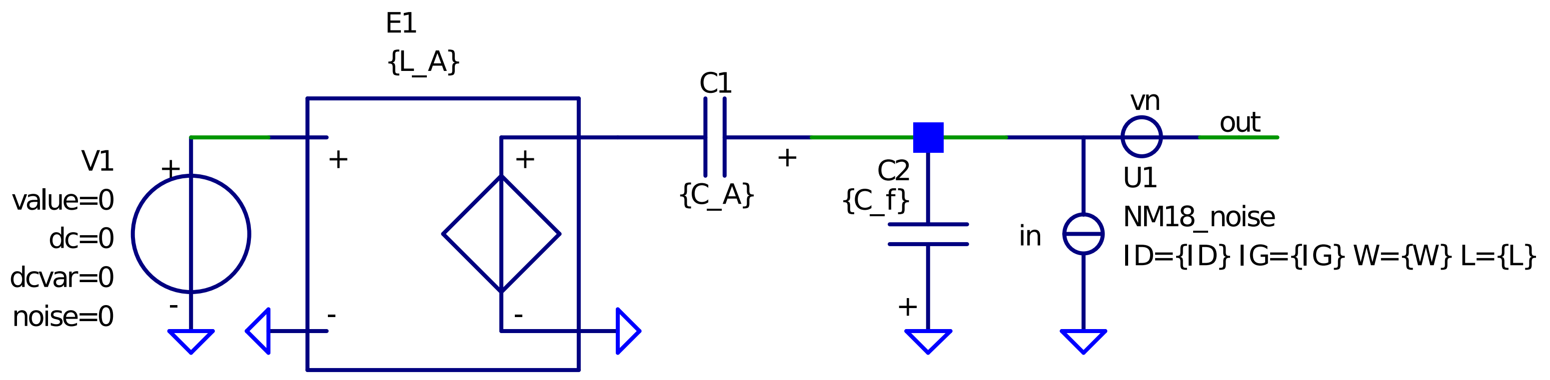


Source-referred noise at the output of E1:

CS input stage design



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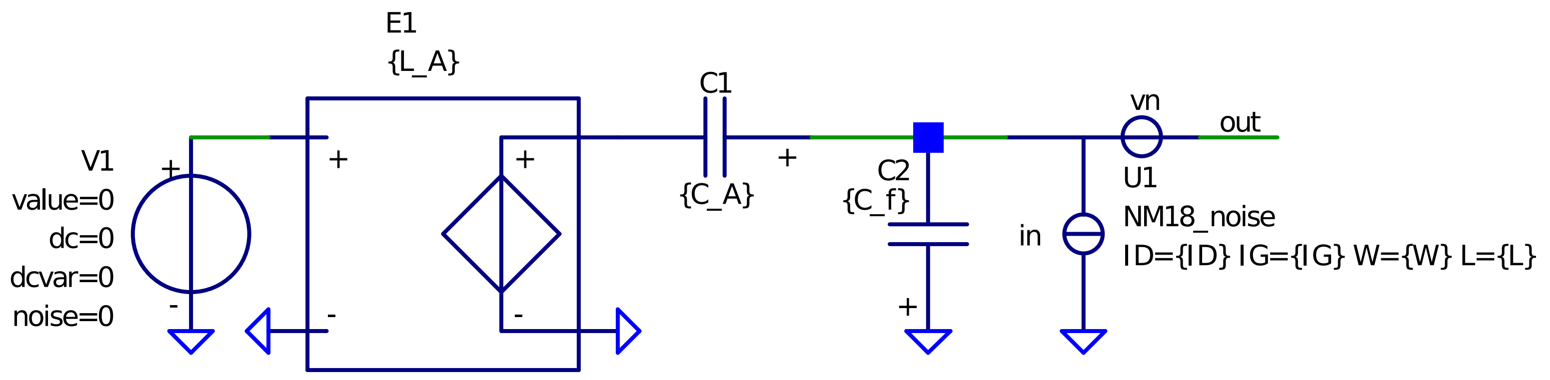
$$S_{v_n} = \frac{4kTn\Gamma}{g_m}\left(1 + \frac{c_{iss}}{C_s}\right)^2\left(1 + \frac{f_\ell}{f}\right)$$

$$f_\ell = \alpha f_T = \alpha \frac{g_m}{2\pi c_{iss}}$$

α: process parameter

CS input stage design



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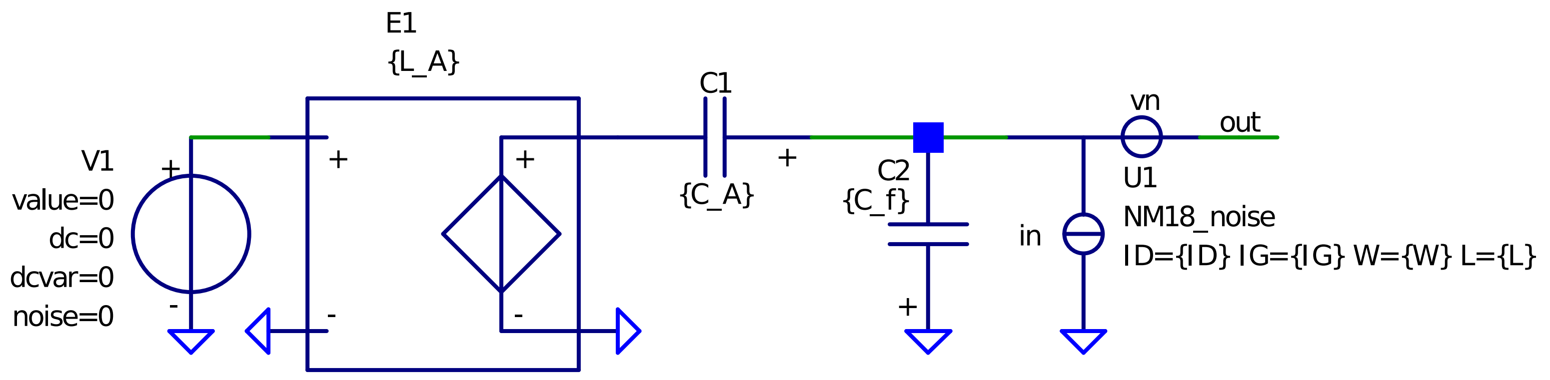

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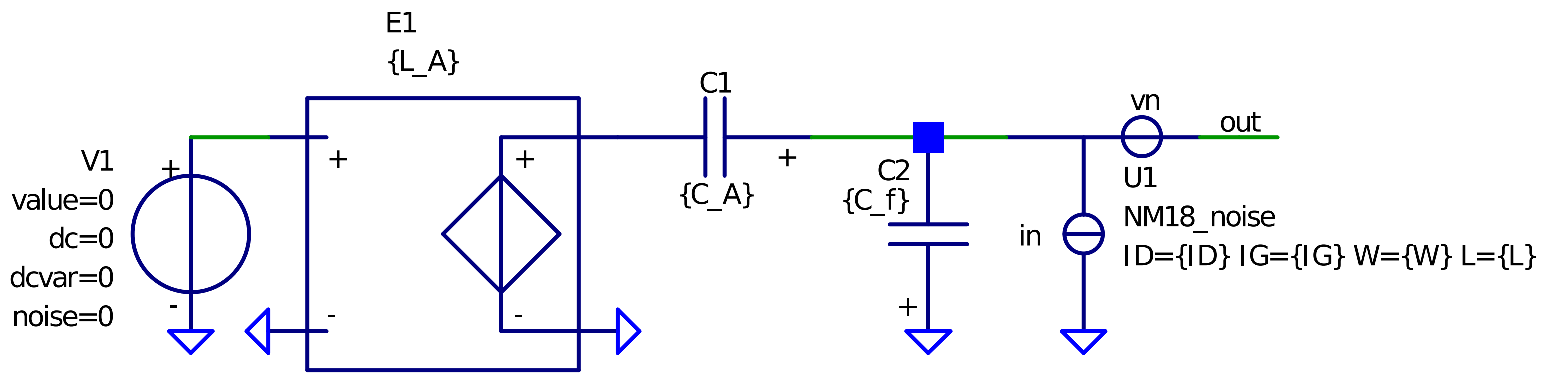

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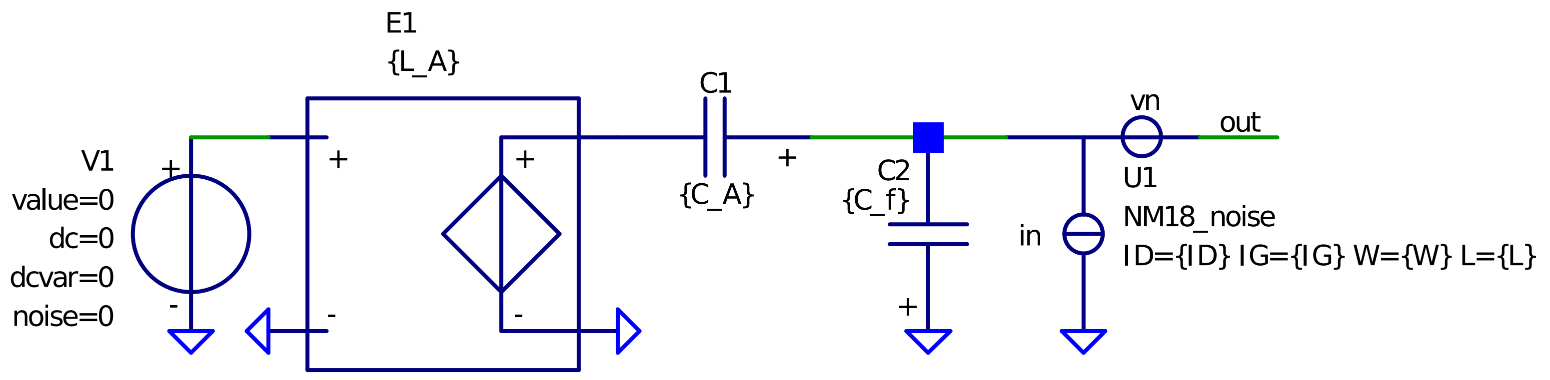

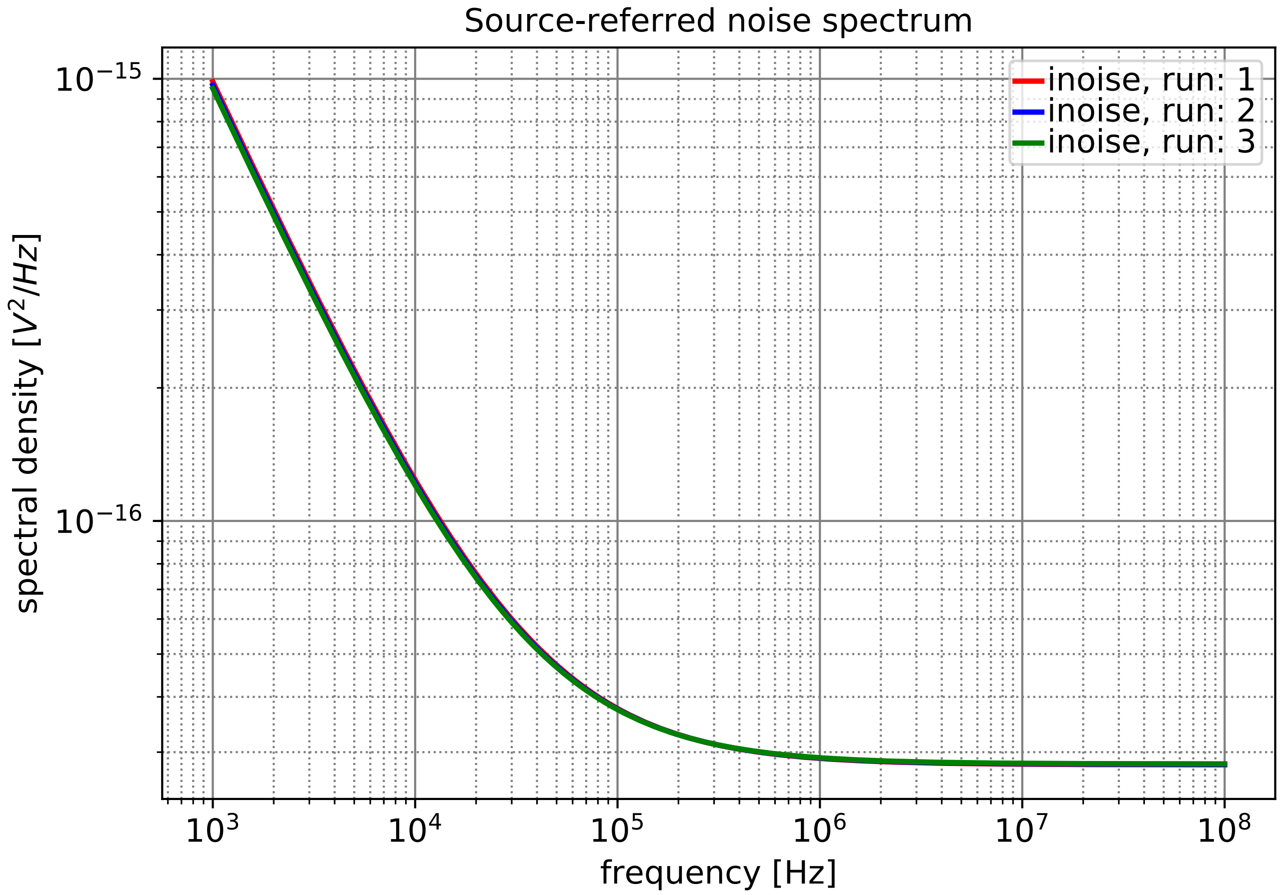

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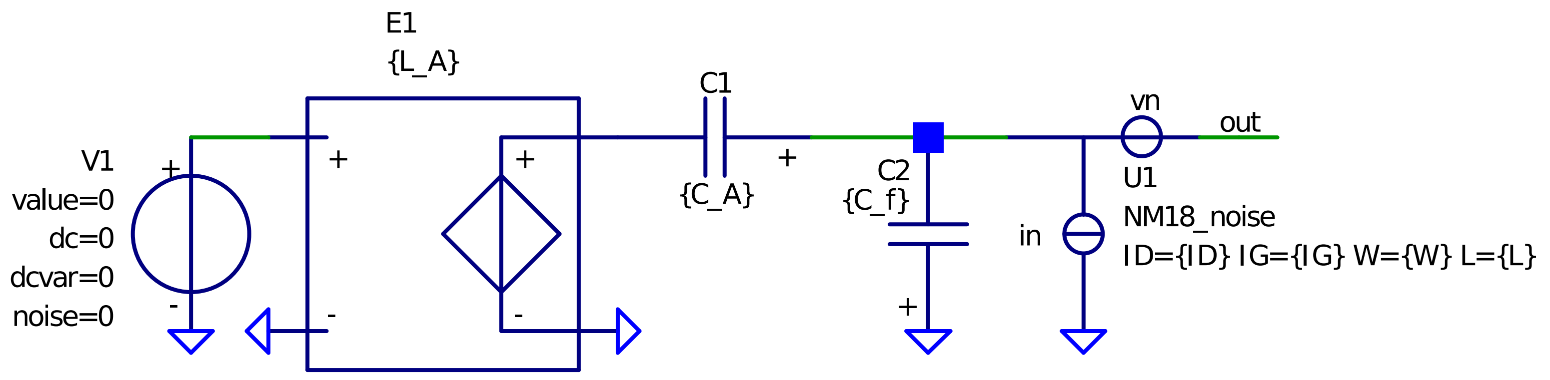
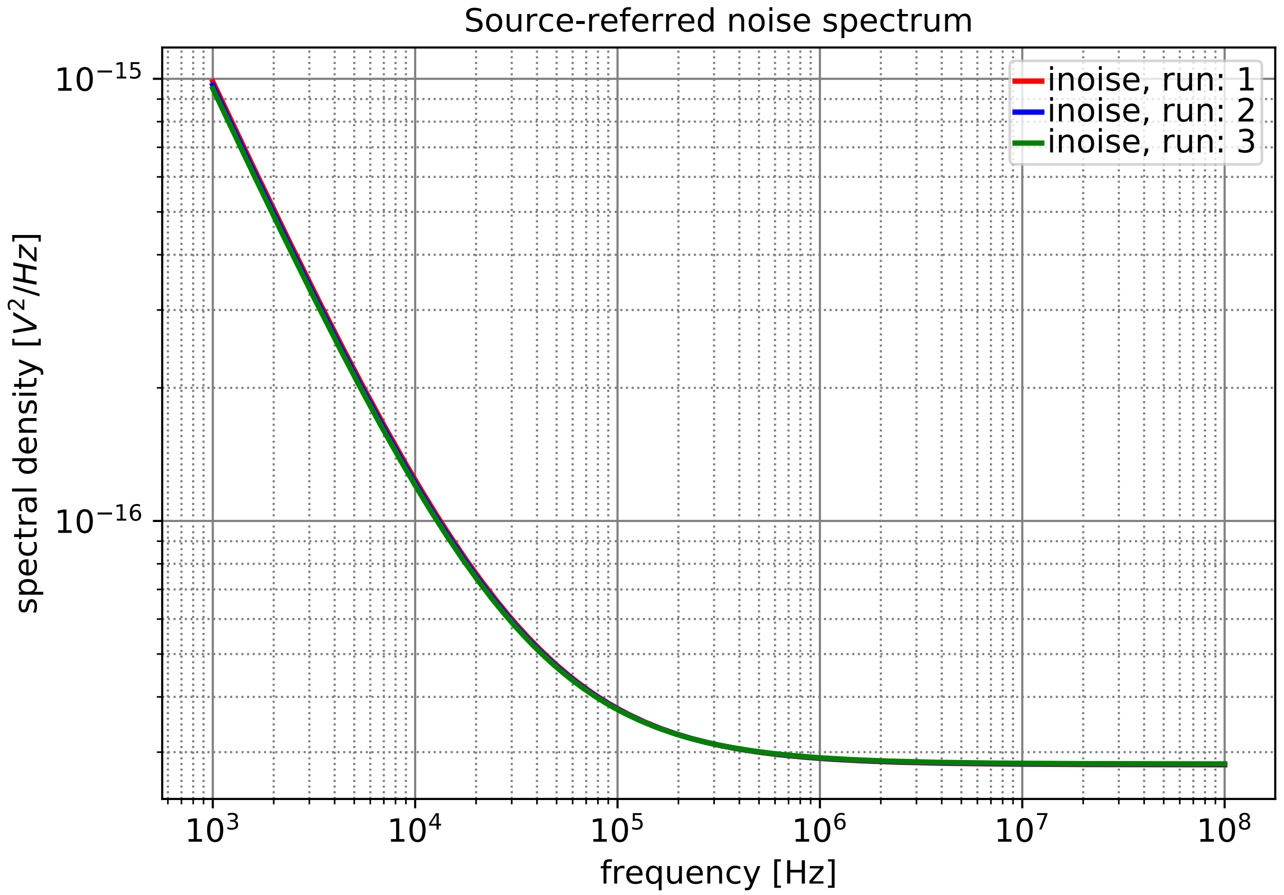
Antenna-referred noise:

CS input stage design





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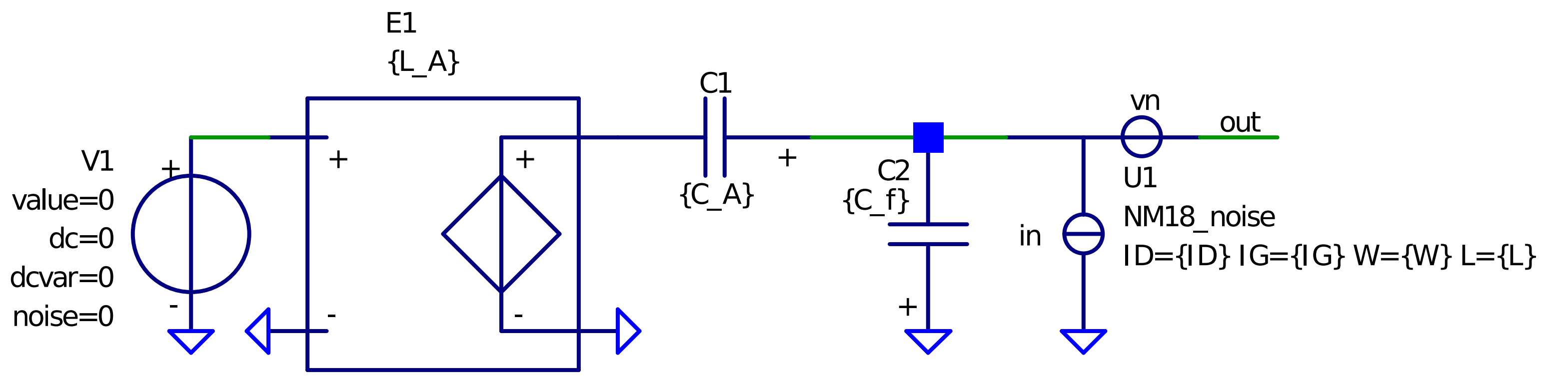
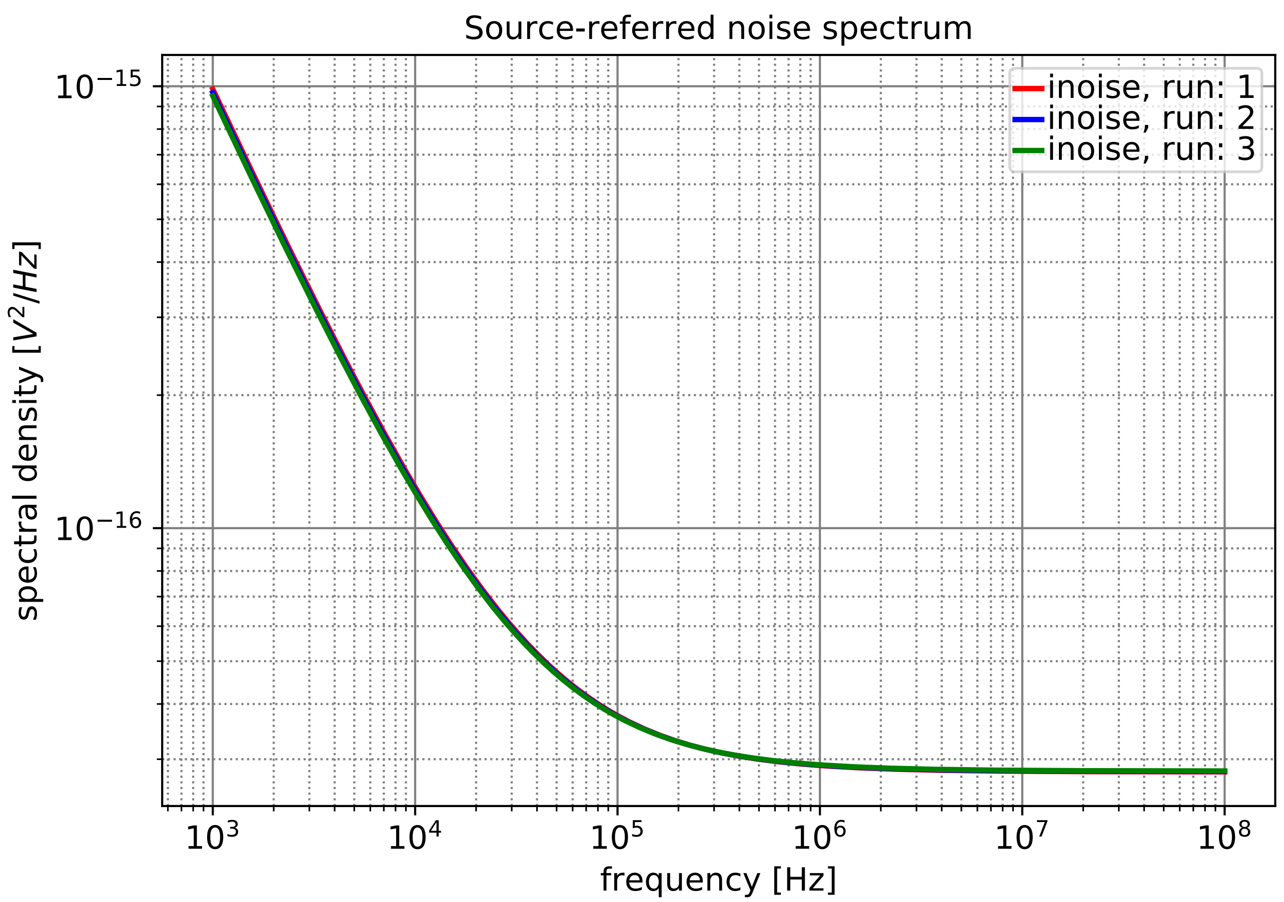
Antenna-referred noise:

1 : W = 1.20e-3, L = 1.25e-6, ID = 1.39e-03, S_f = 2.81e-17, f_ell = 3.41e+4, Ciss = 1.03e-11, IC=2.27e+0.

CS input stage design





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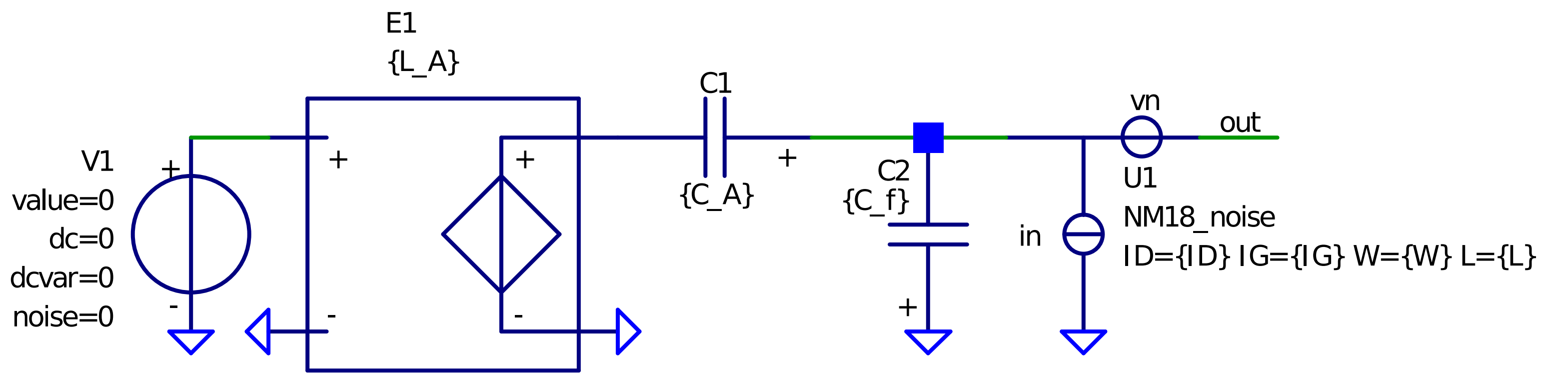
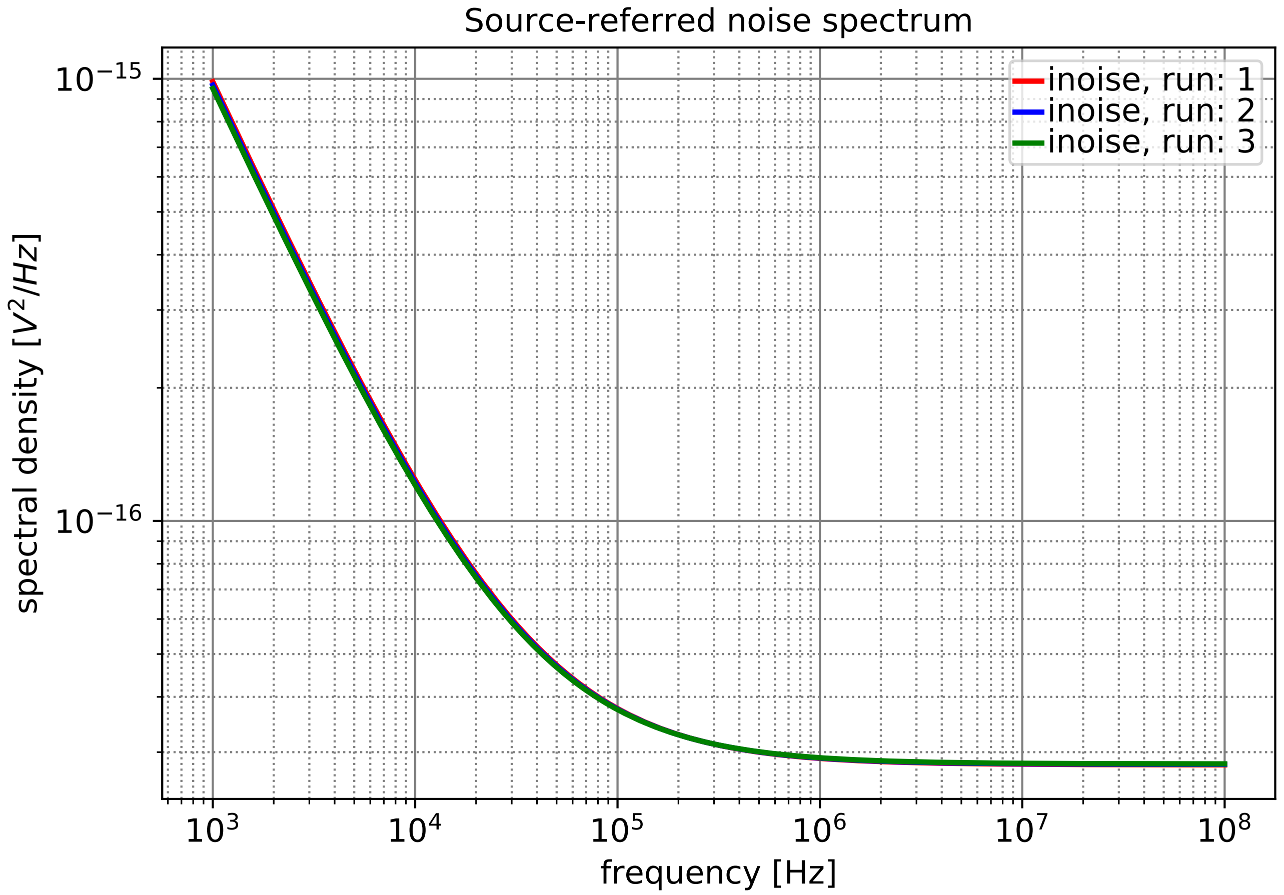
2 : W = 9.00e-4, L = 1.71e-6, ID = 2.13e-03, S_f = 2.82e-17, f_ell = 3.34e+4, Ciss = 1.03e-11, IC=6.31e+0.

CS input stage design





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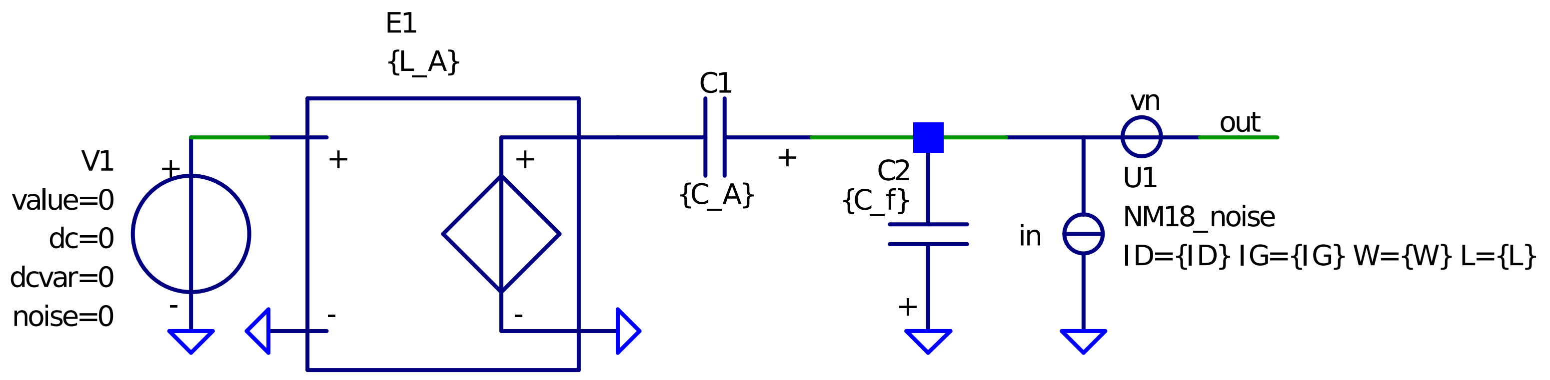
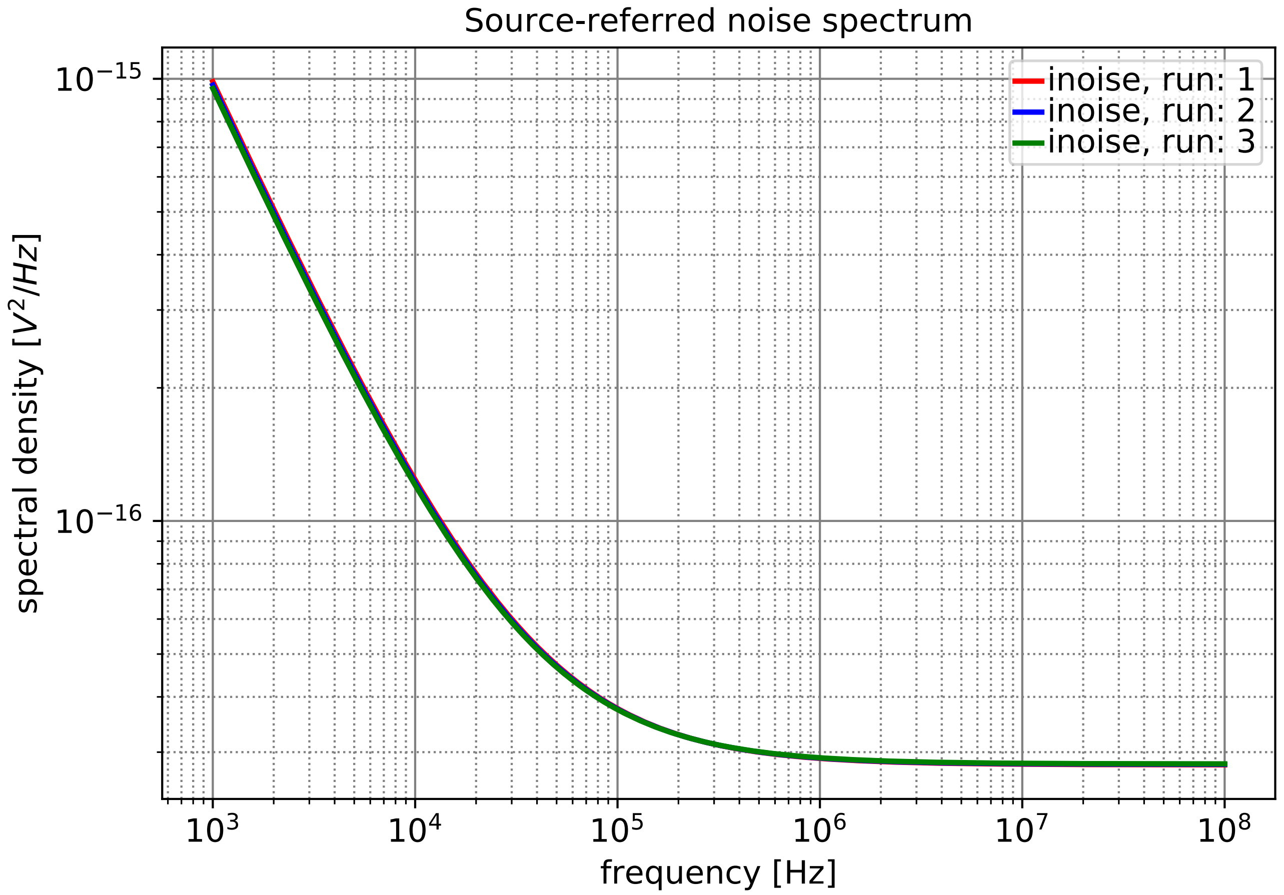
3 : W = 6.00e-4, L = 2.61e-6, ID = 4.50e-03, S_f = 2.82e-17, f_ell = 3.27e+4, Ciss = 1.03e-11, IC=3.06e+1.

CS input stage design





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Foor noise: $$S_{v_n} = \frac{4kTn\Gamma}{g_m}\left(1+\frac{c_{iss}}{C_s}\right)^2$$

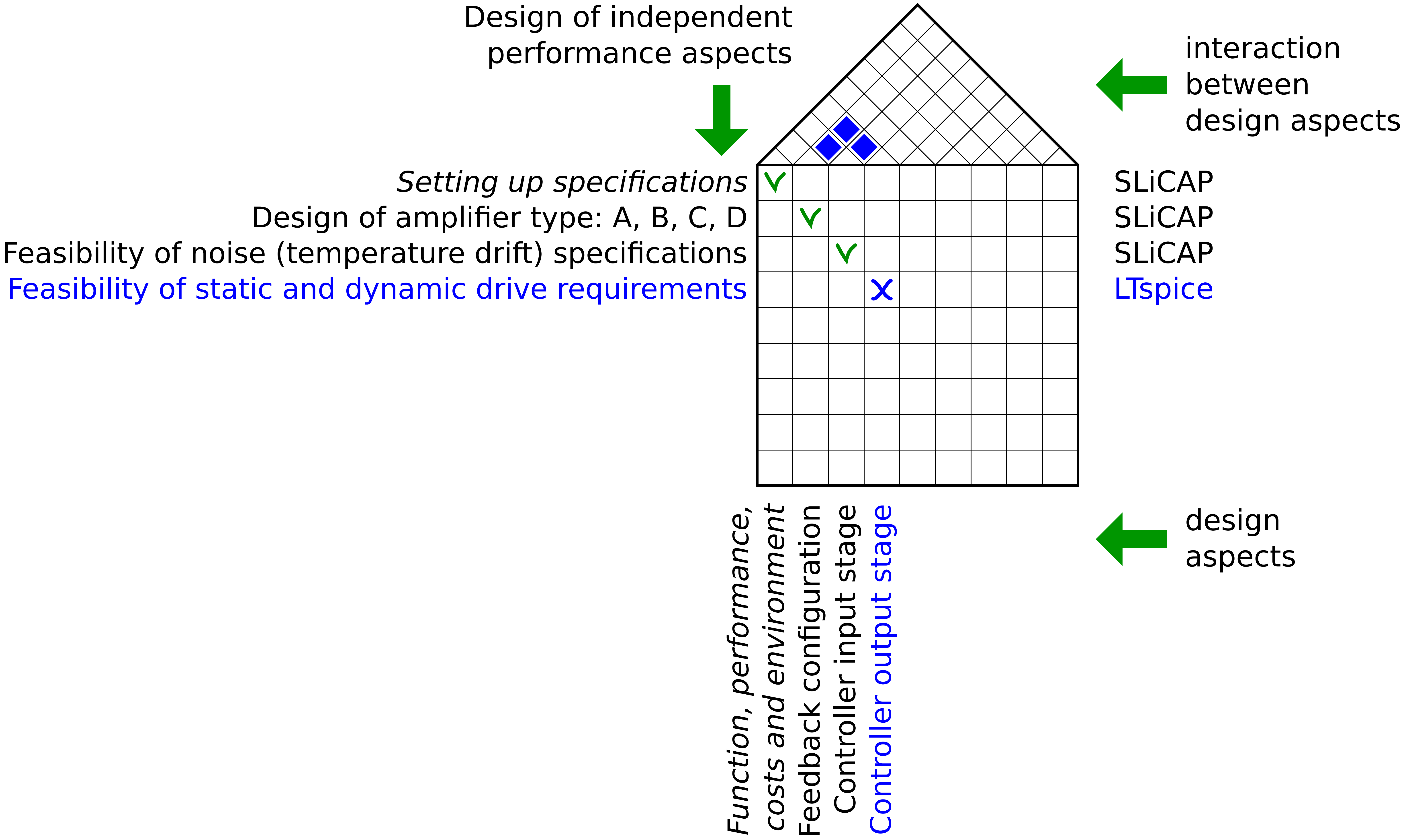
Antenna-referred noise:

1 : W = 1.20e-3, L = 1.25e-6, ID = 1.39e-03, S_f = 2.81e-17, f_ell = 3.41e+4, Ciss = 1.03e-11, IC=2.27e+0.
2 : W = 9.00e-4, L = 1.71e-6, ID = 2.13e-03, S_f = 2.82e-17, f_ell = 3.34e+4, Ciss = 1.03e-11, IC=6.31e+0.
3 : W = 6.00e-4, L = 2.61e-6, ID = 4.50e-03, S_f = 2.82e-17, f_ell = 3.27e+4, Ciss = 1.03e-11, IC=3.06e+1.

Structured Electronic Design

Step 4
Feasibility load drive requirements

Anton J.M. Montagne



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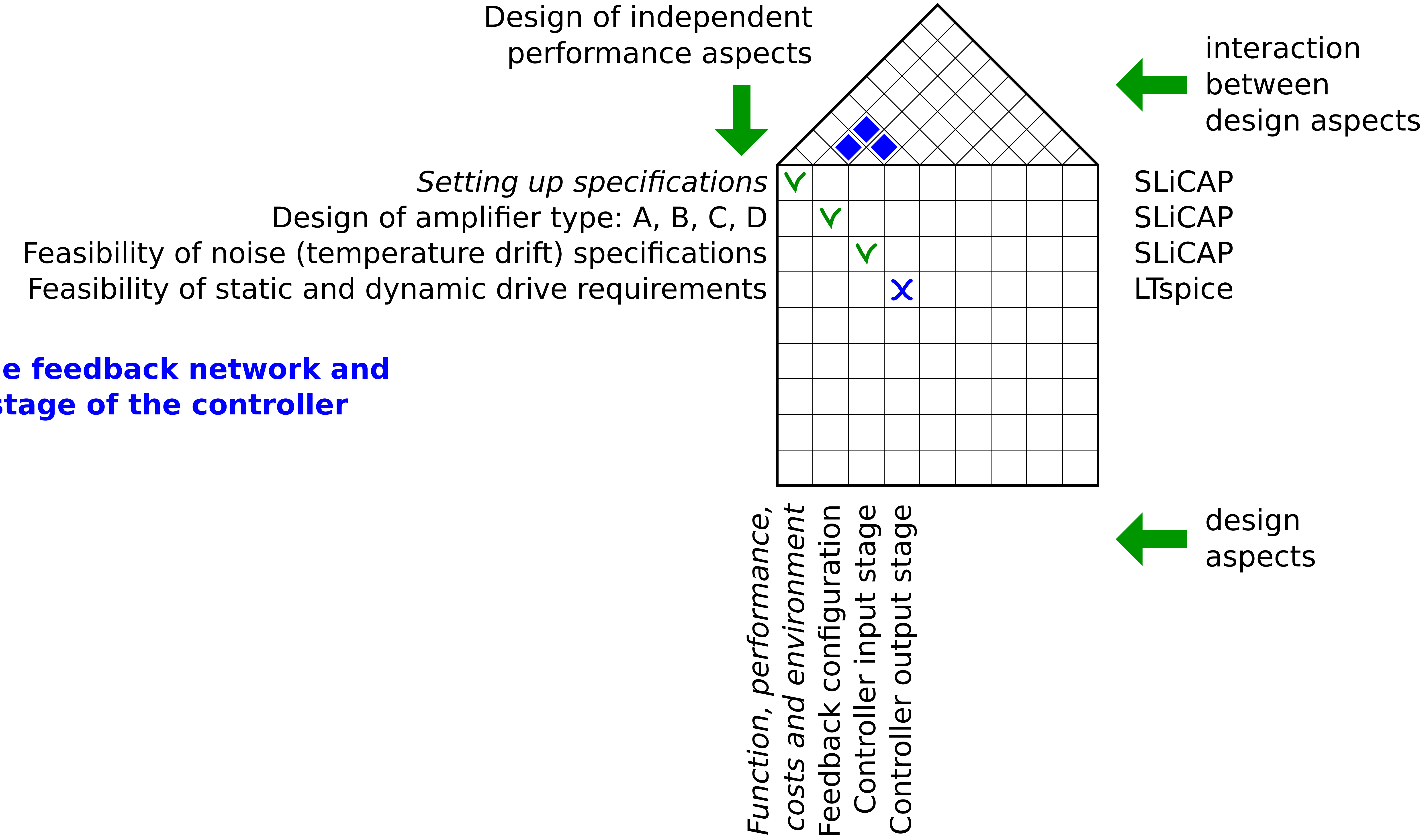
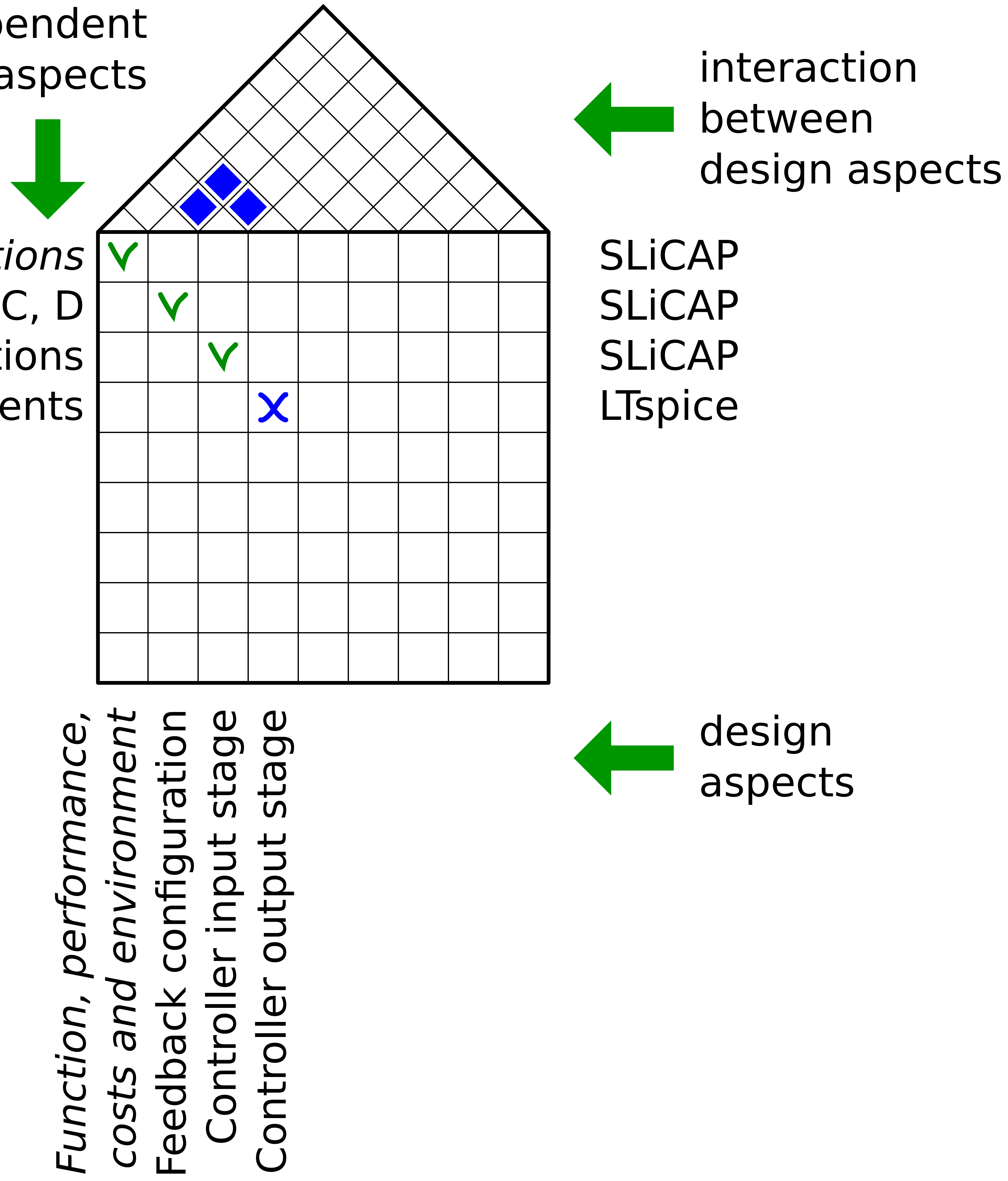
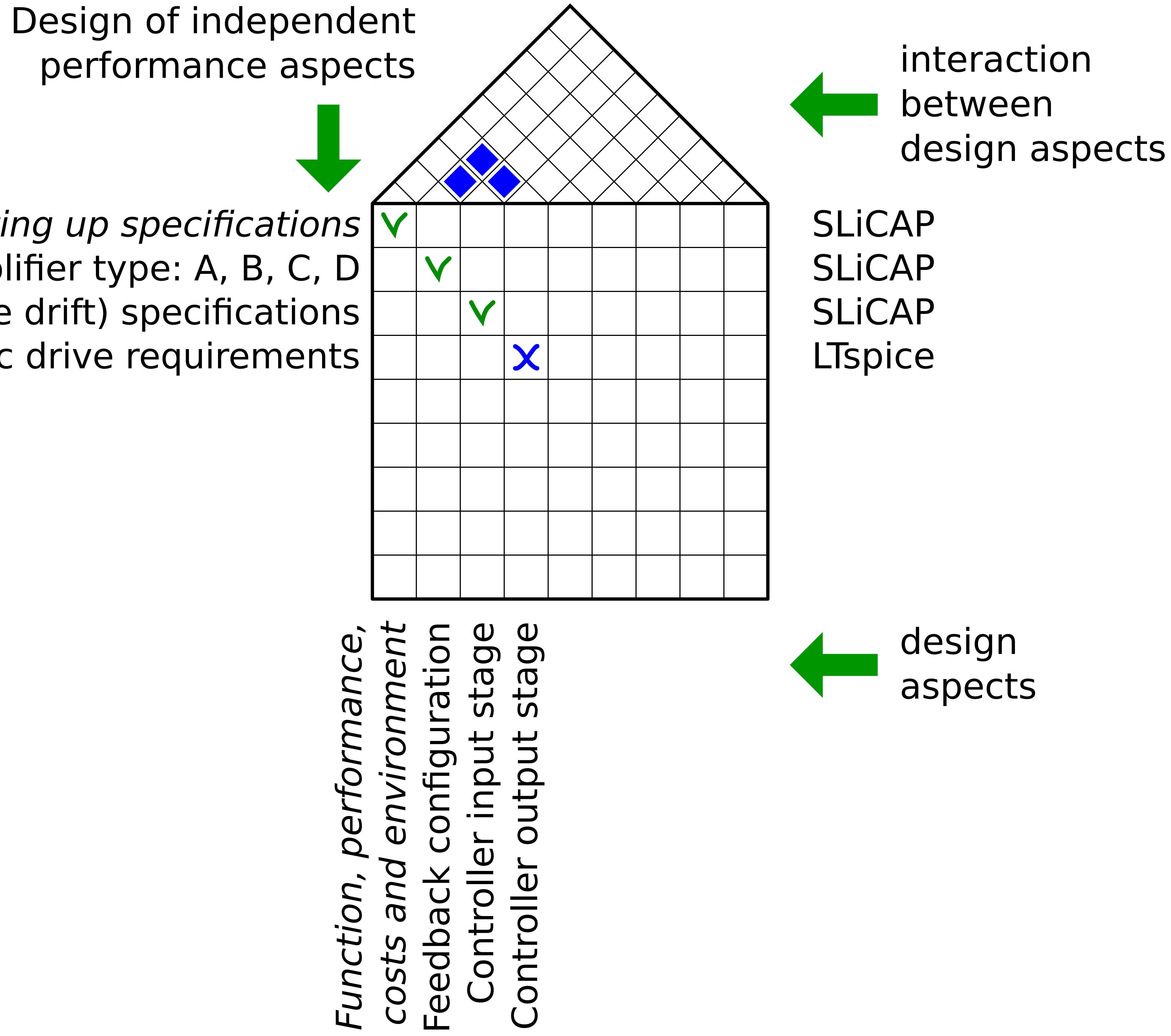


Design of the feedback network and the output stage of the controller

Design of the feedback network and the output stage of the controller

Design of the active antenna:





Design of the feedback network and the output stage of the controller

Design of the active antenna:

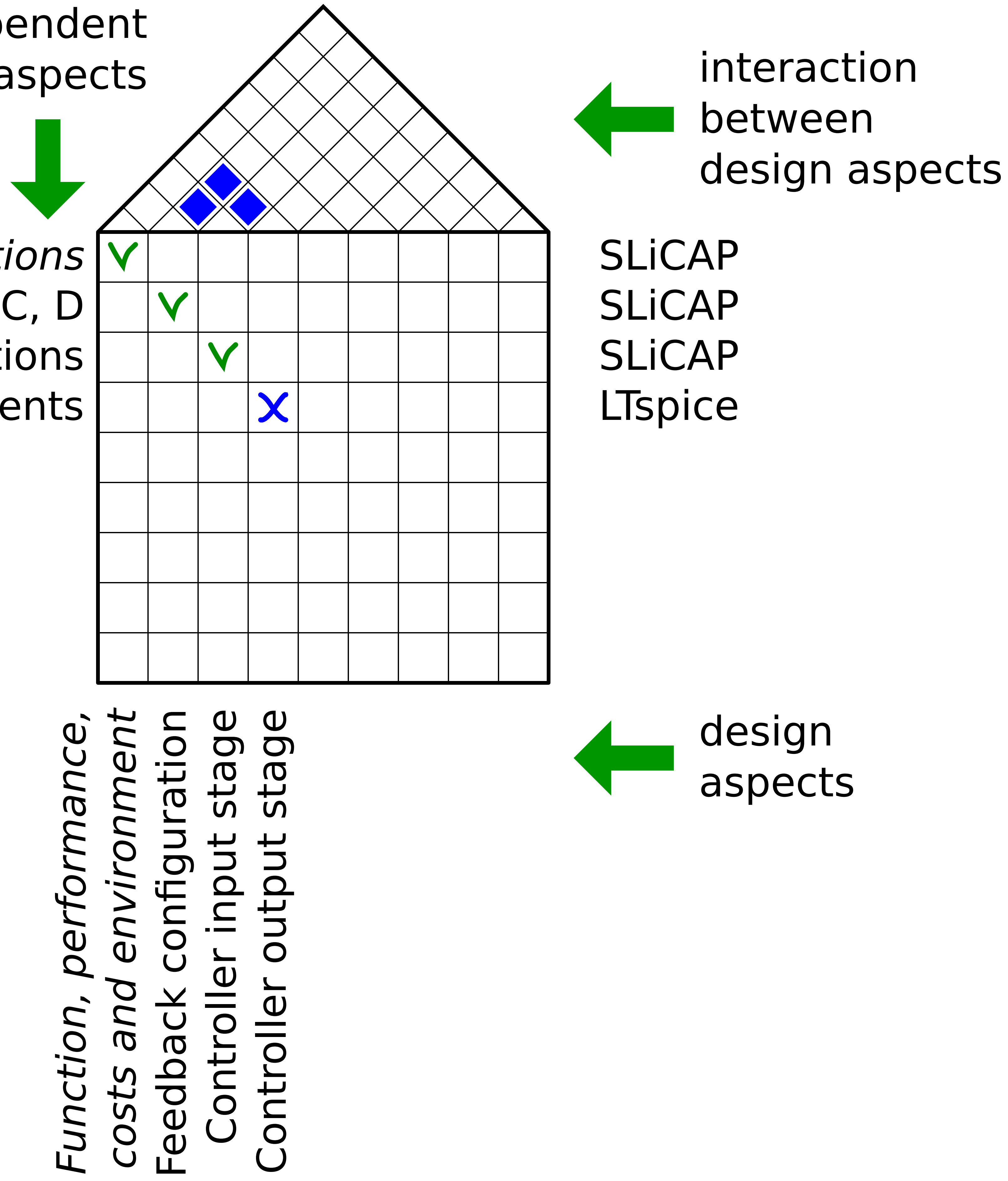
Design a CS stage with sufficient static and dynamic drive capability

Design of the feedback network and the output stage of the controller

Design of the active antenna:

Design a CS stage with sufficient static and dynamic drive capability

Determine valid ranges for: I_{DS}, V_{DS}, W, L, M



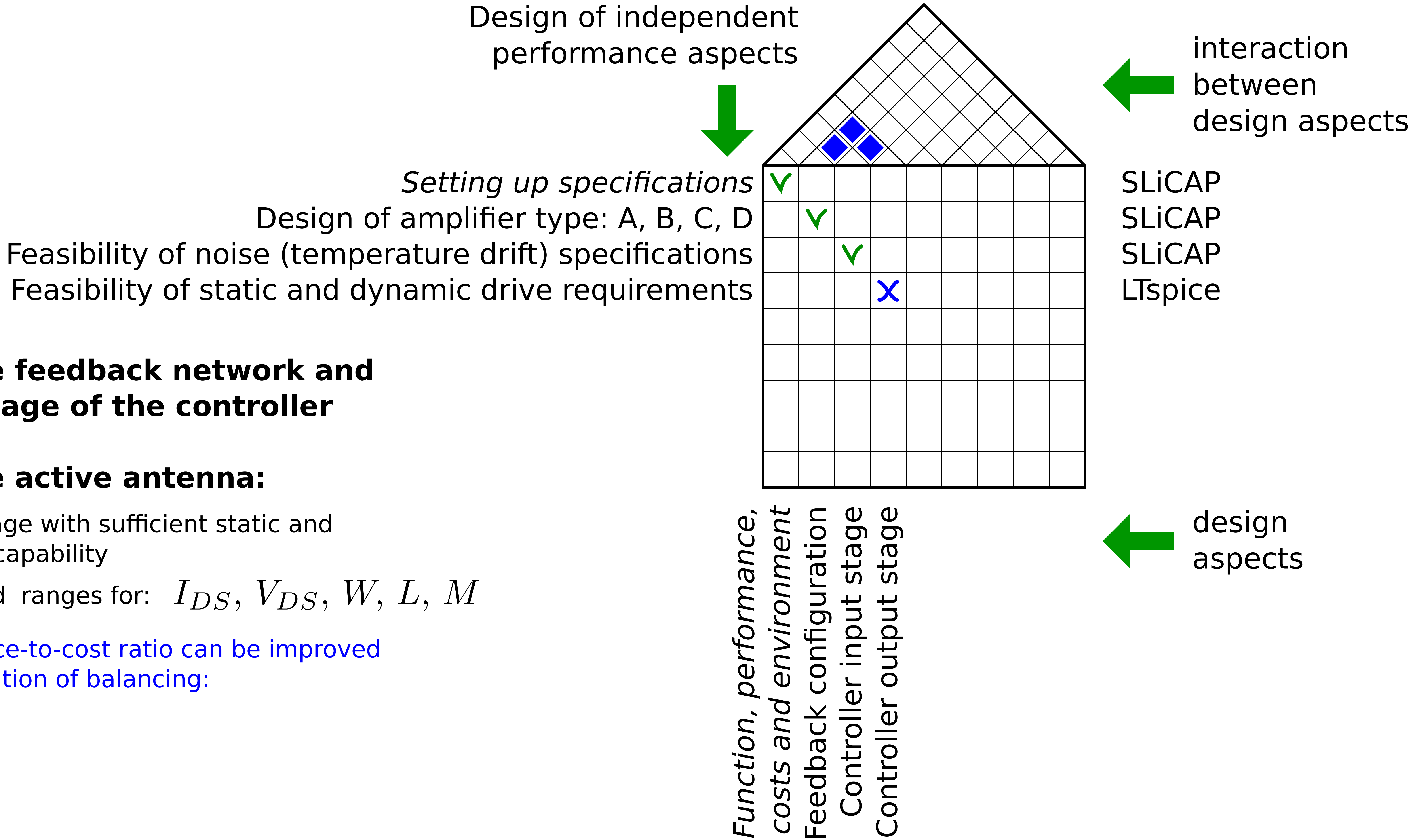
Design of the feedback network and the output stage of the controller

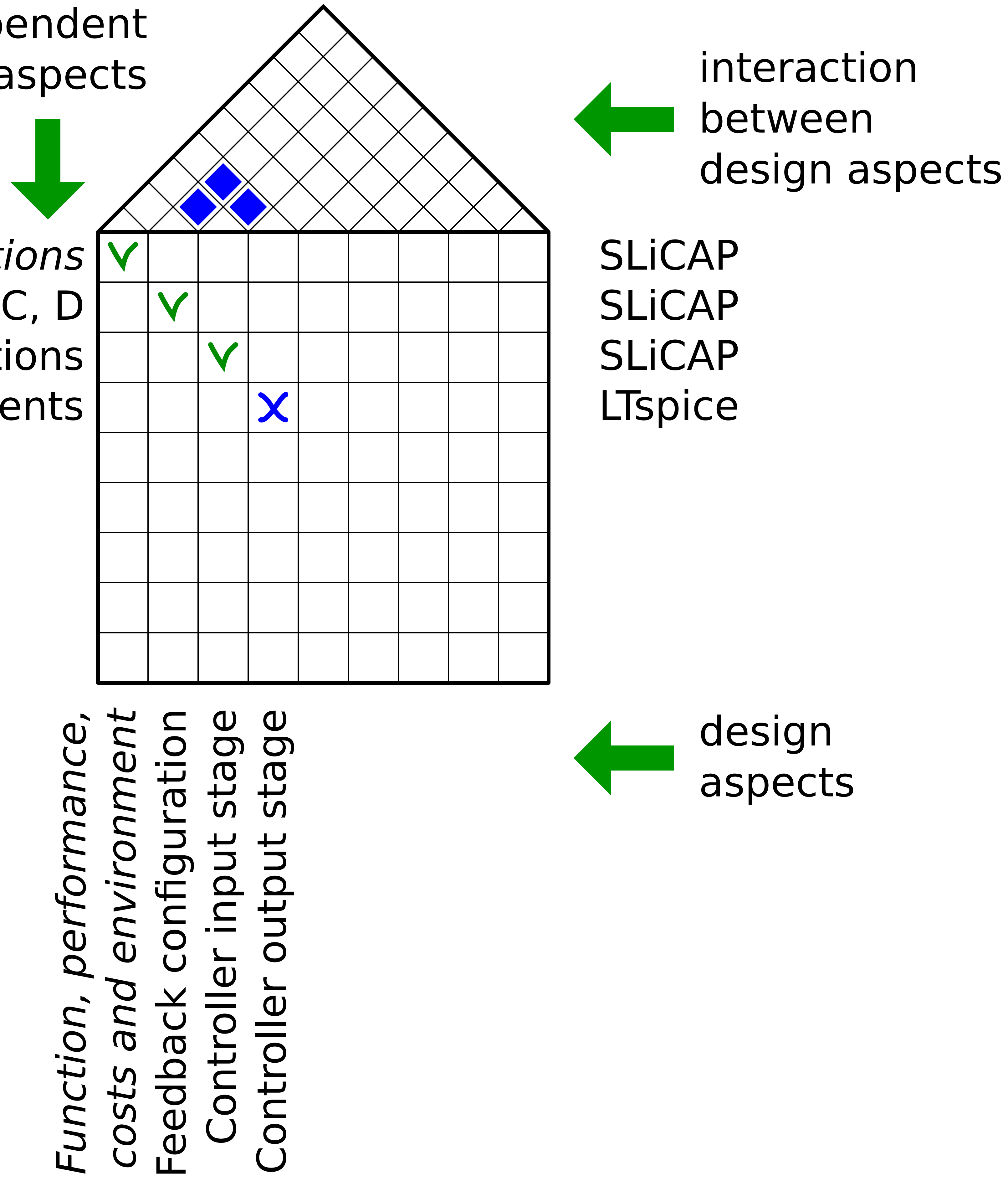
Design of the active antenna:

Design a CS stage with sufficient static and dynamic drive capability

Determine valid ranges for: I_{DS}, V_{DS}, W, L, M

The performance-to-cost ratio can be improved through application of balancing:





Design of the feedback network and the output stage of the controller

Design of the active antenna:

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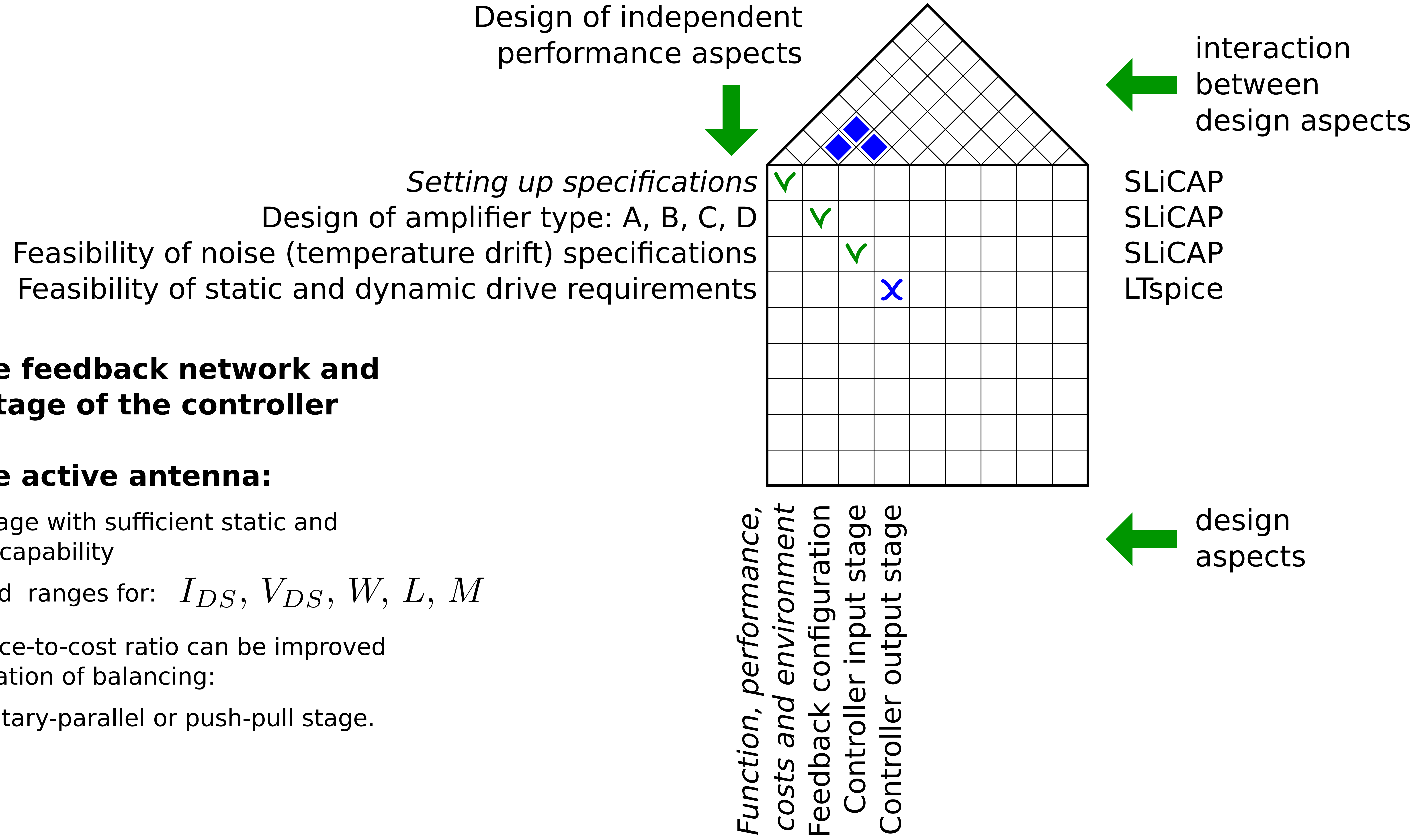
Determine valid ranges for: I_{DS}, V_{DS}, W, L, M

The performance-to-cost ratio can be improved through application of balancing:

Complementary-parallel or push-pull stage.



Design of the feedback network and the output stage of the controller

Design of the active antenna:

Design a CS stage with sufficient static and dynamic drive capability

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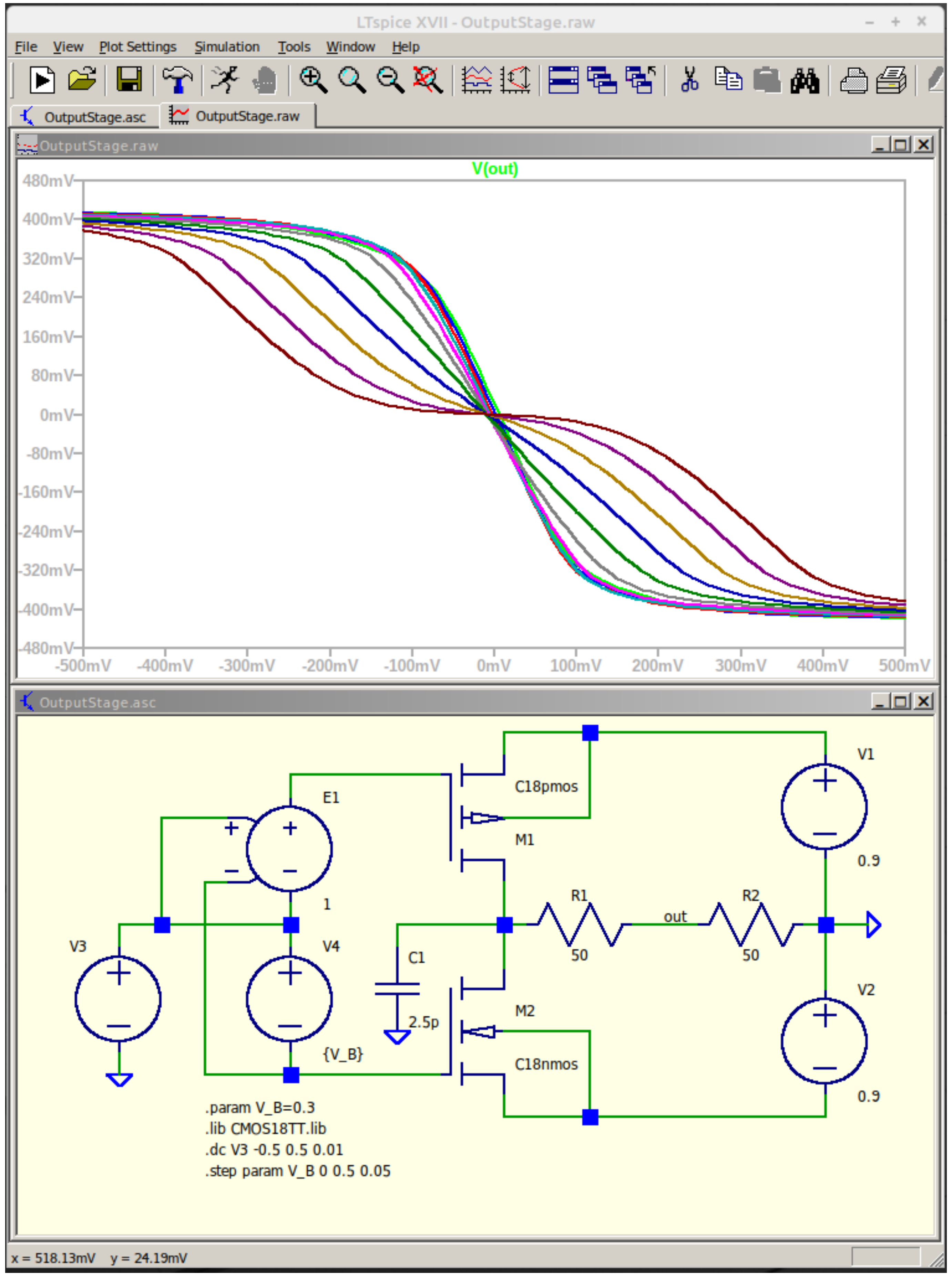
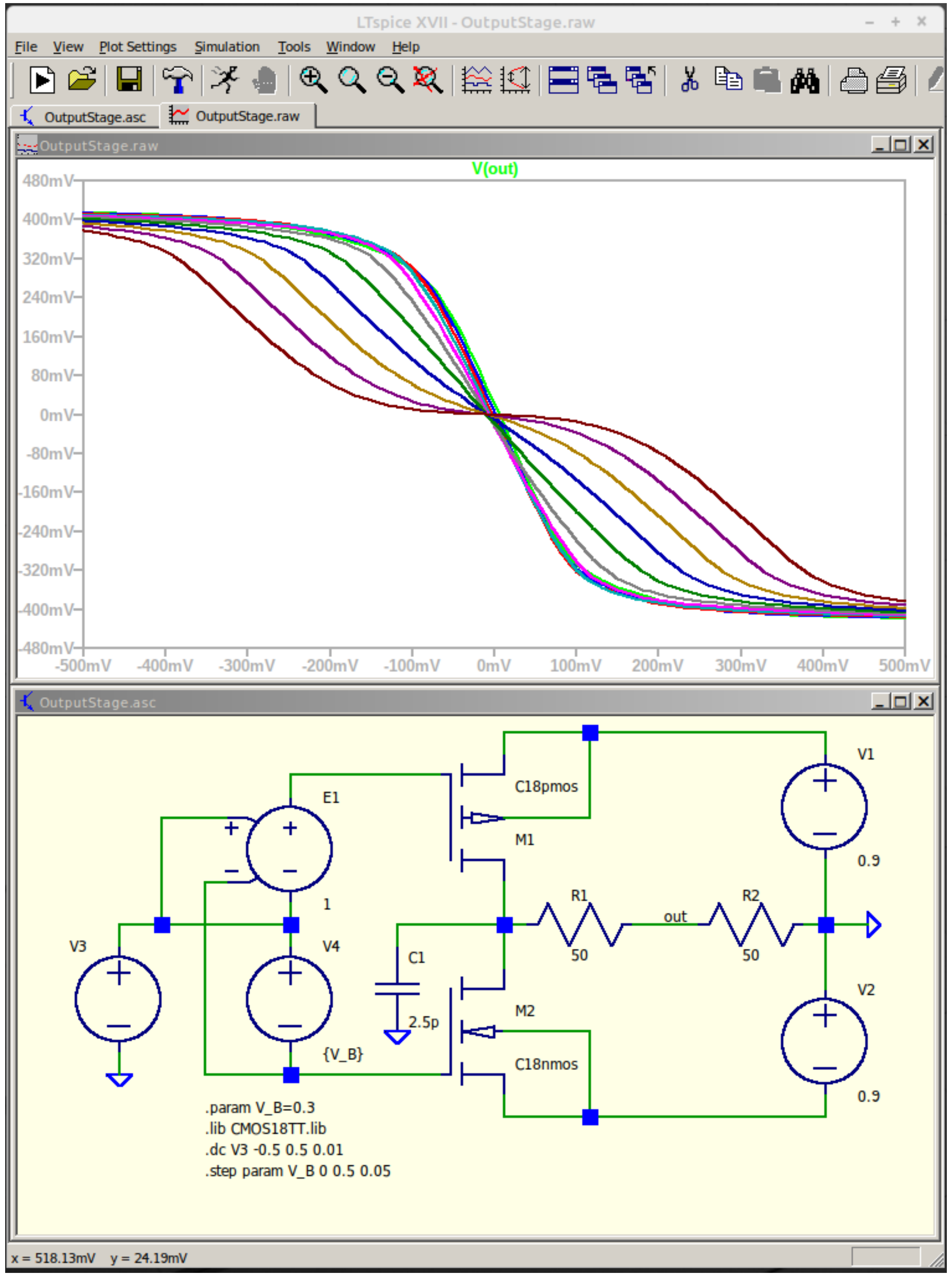
CS output stage design

CS output stage design

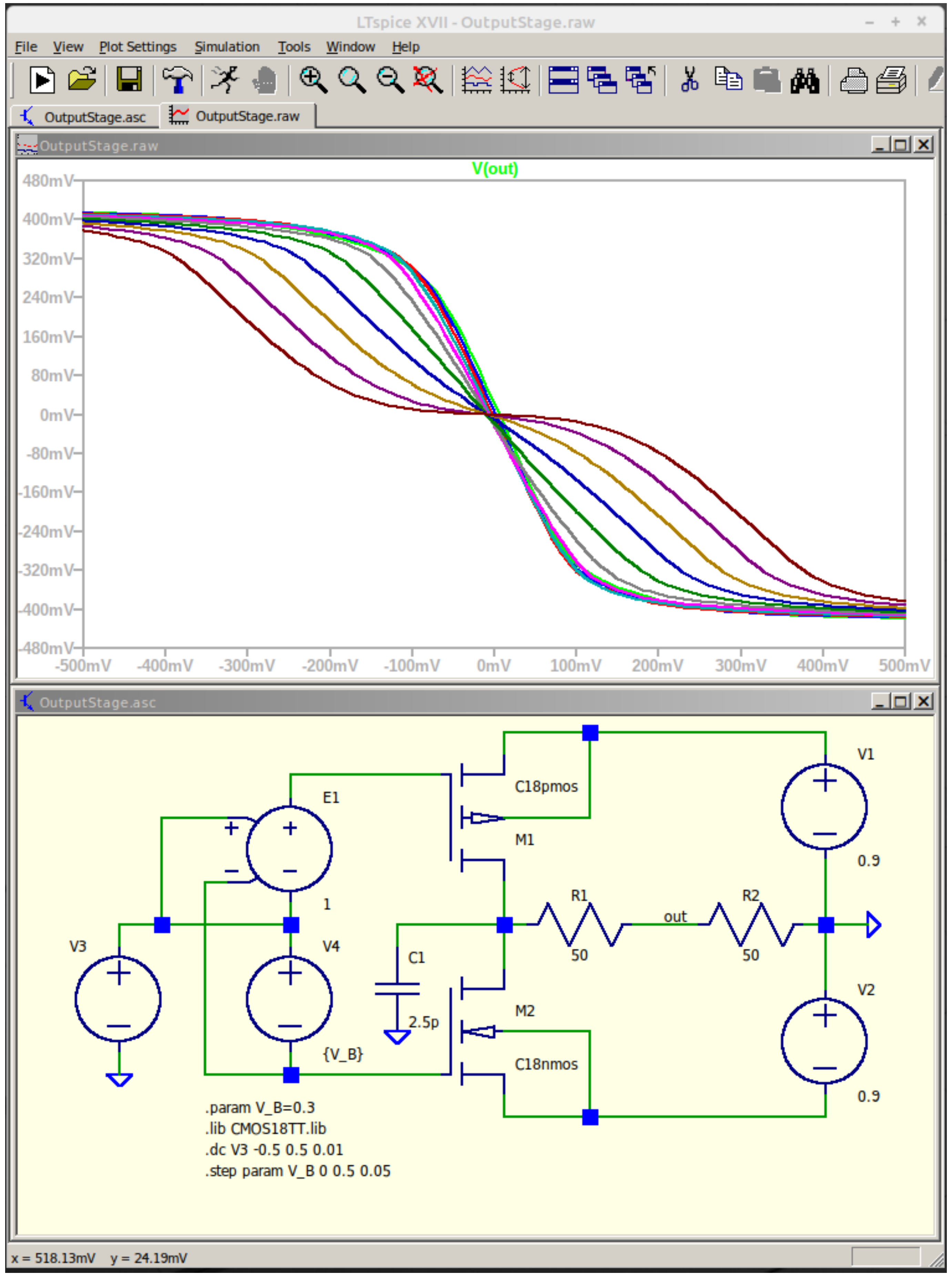


CS output stage design



Smallest value for L: 180nm

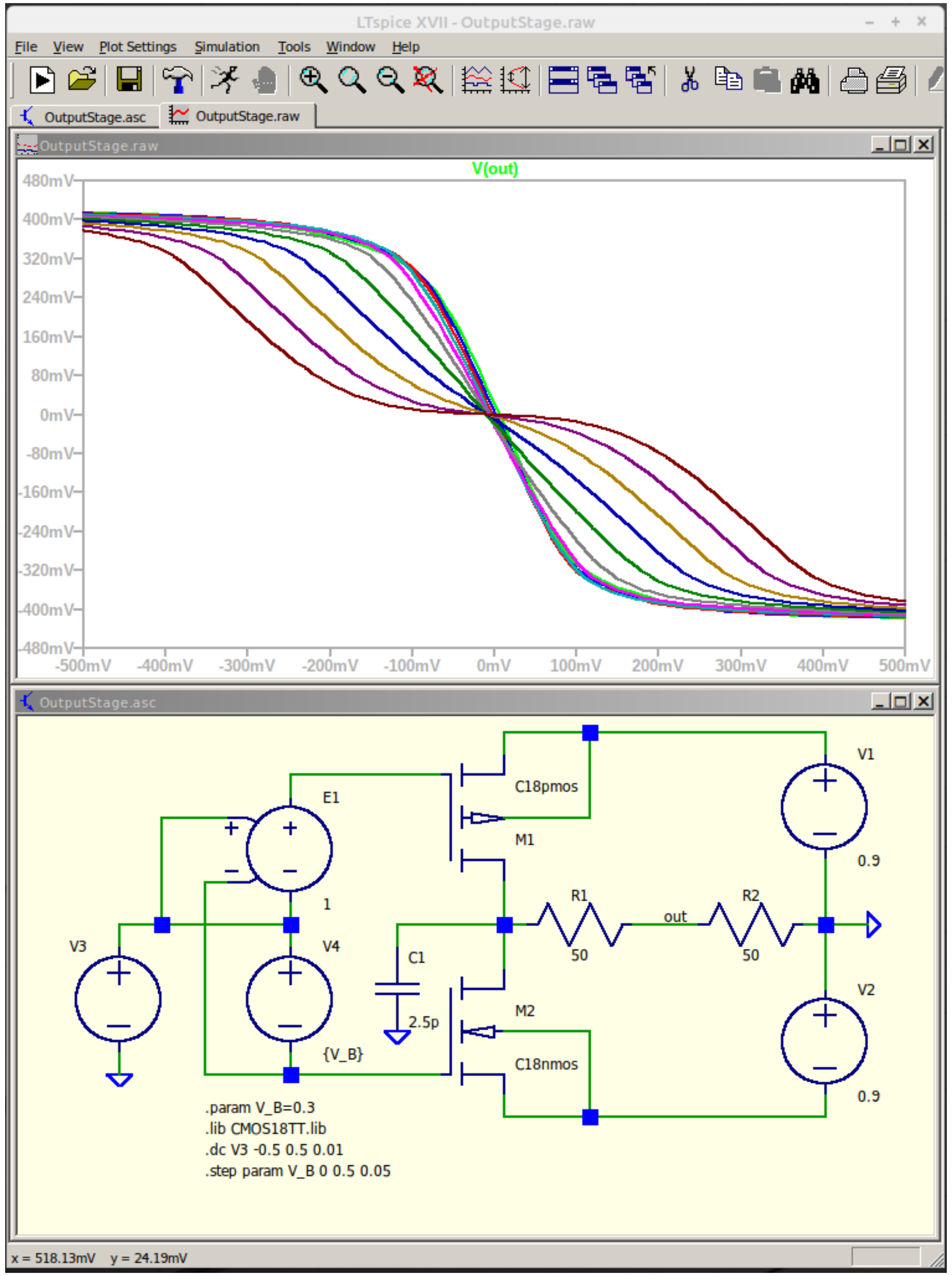
CS output stage design



Smallest value for L: 180nm

Wpmos/Wnmos = 1/mobility_ratio

CS output stage design

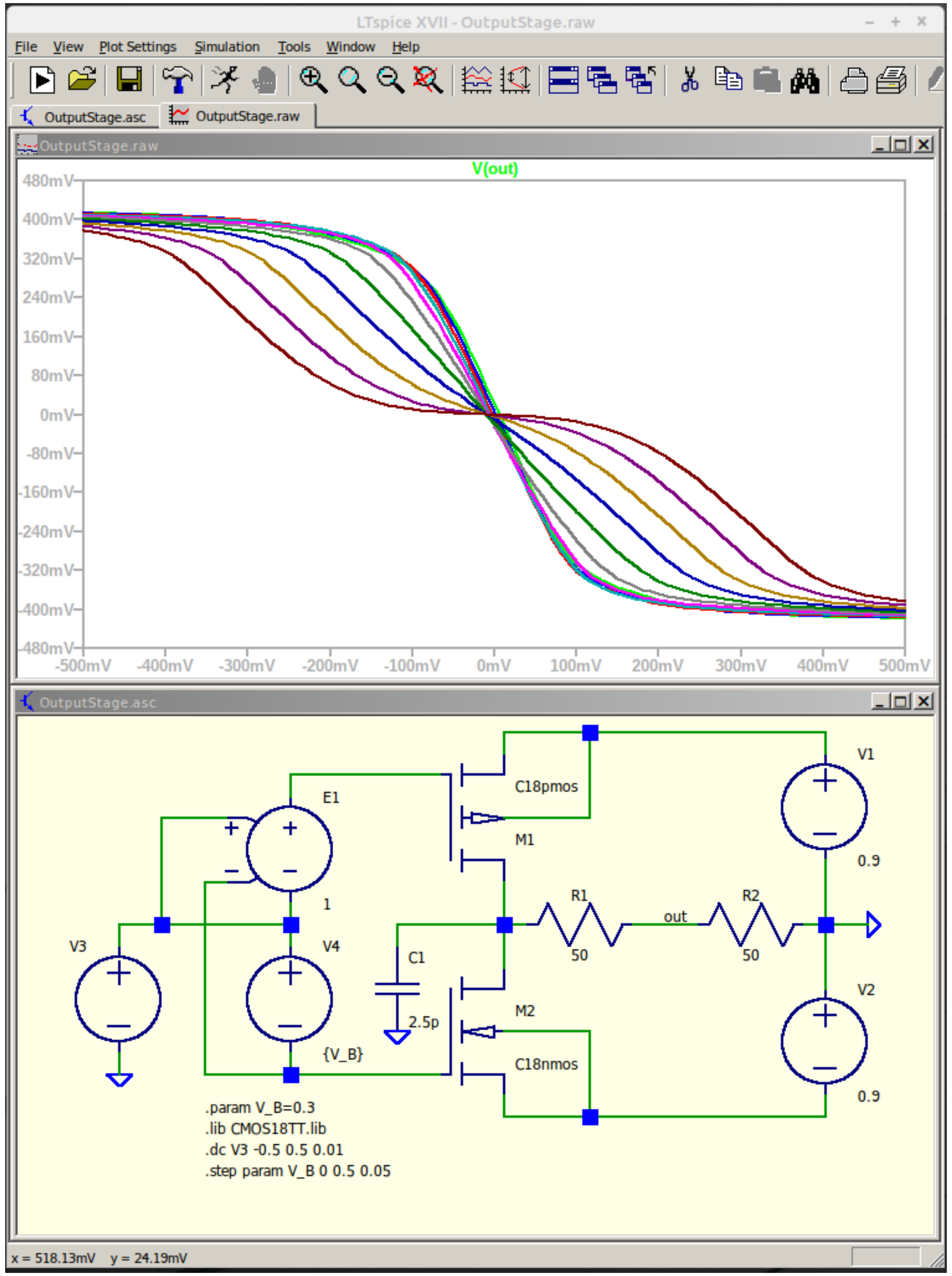


Smallest value for L: 180nm

Wpmos/Wnmos = 1/mobility_ratio

Determine W and M such that the load can be driven with a sufficiently small drive (V3)

CS output stage design



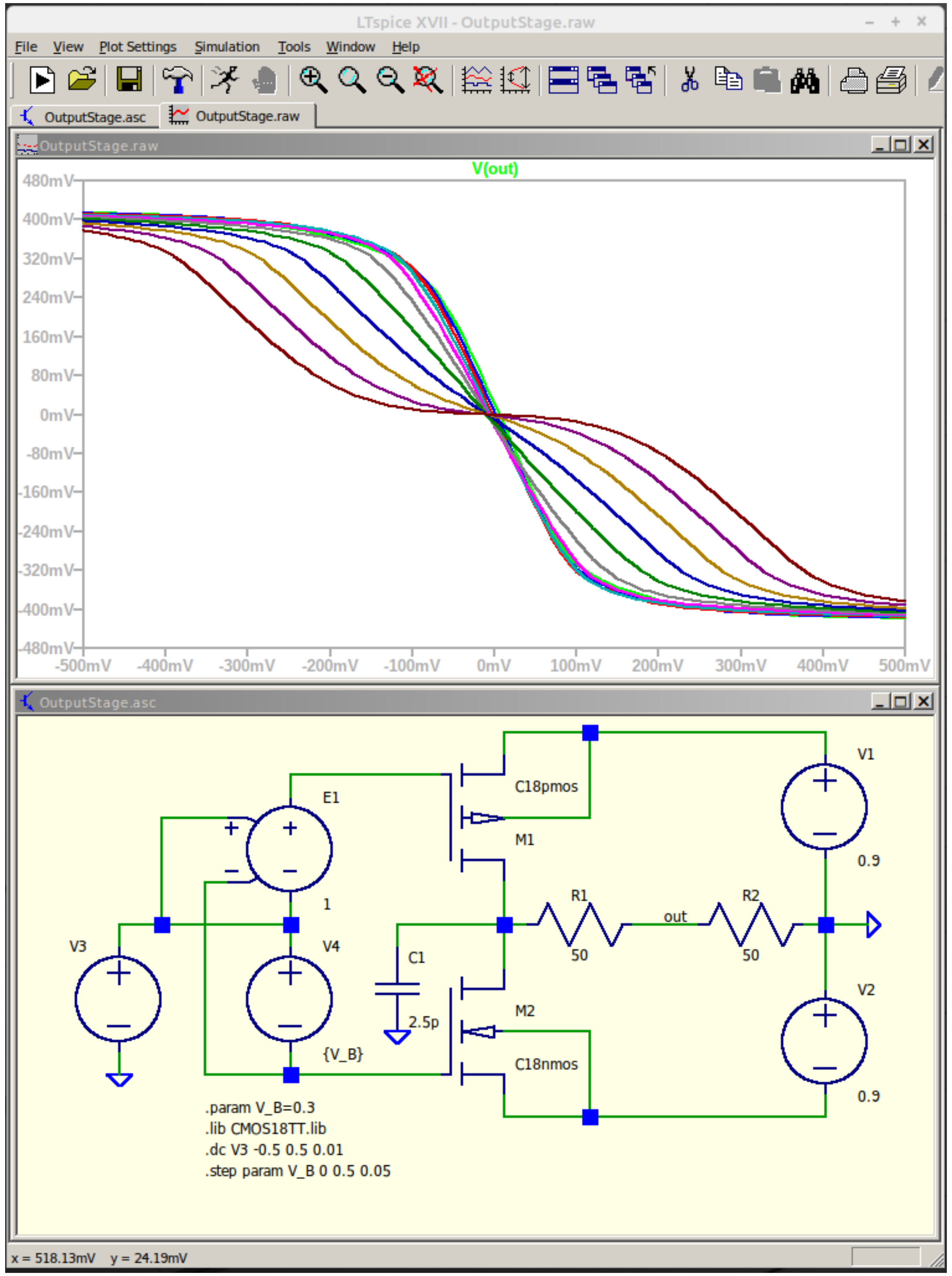
Smallest value for L: 180nm

Wpmos/Wnmos = 1/mobility_ratio

Determine W and M such that the load can be driven with a sufficiently small drive (V3)

PMOS: W=40u, M=10

CS output stage design



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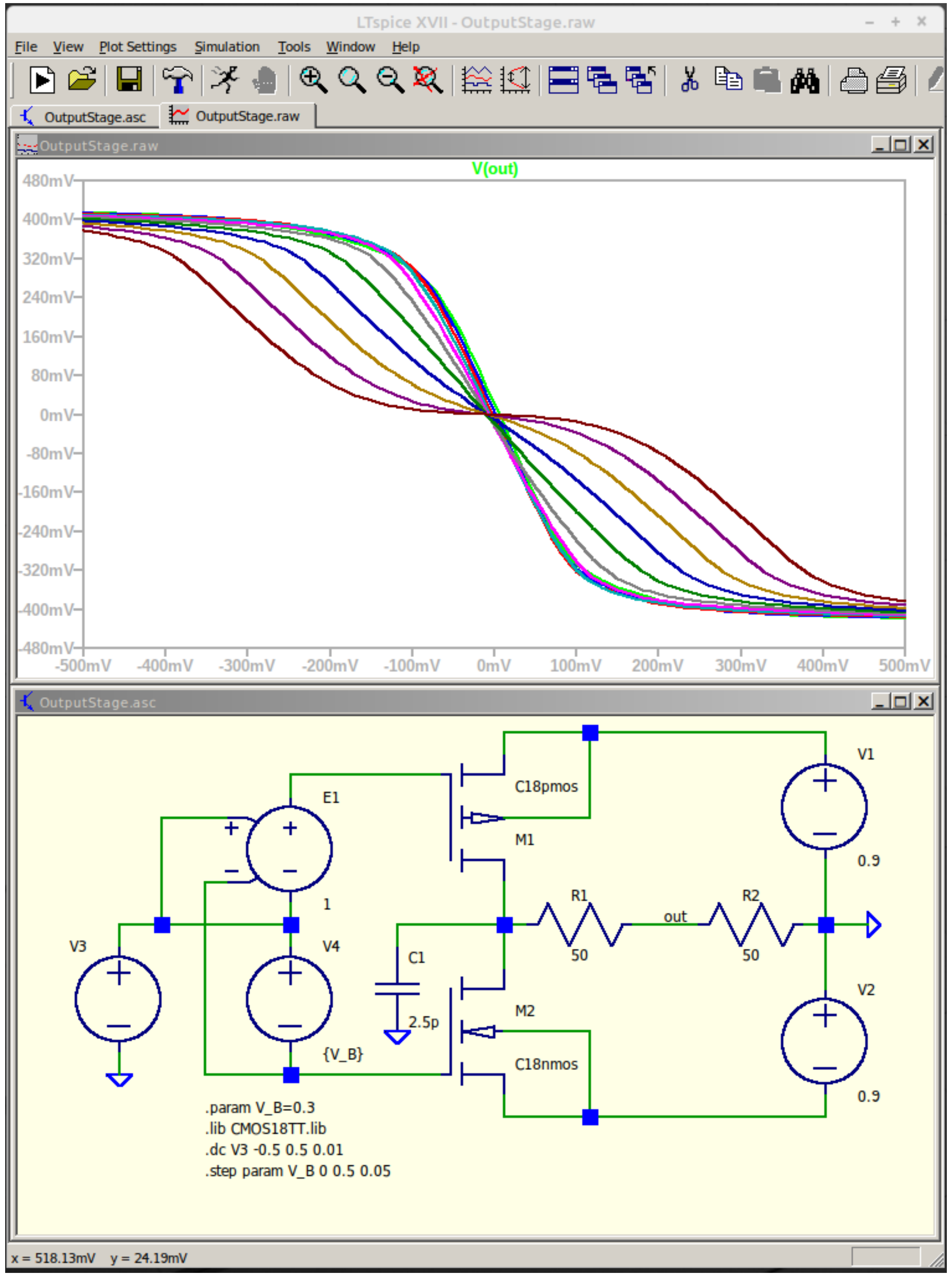
Determine W and M such that the load can be driven with a sufficiently small drive (V3)

PMOS: W=40u, M=10
NMOS: W=40u, M=3

CS output stage design



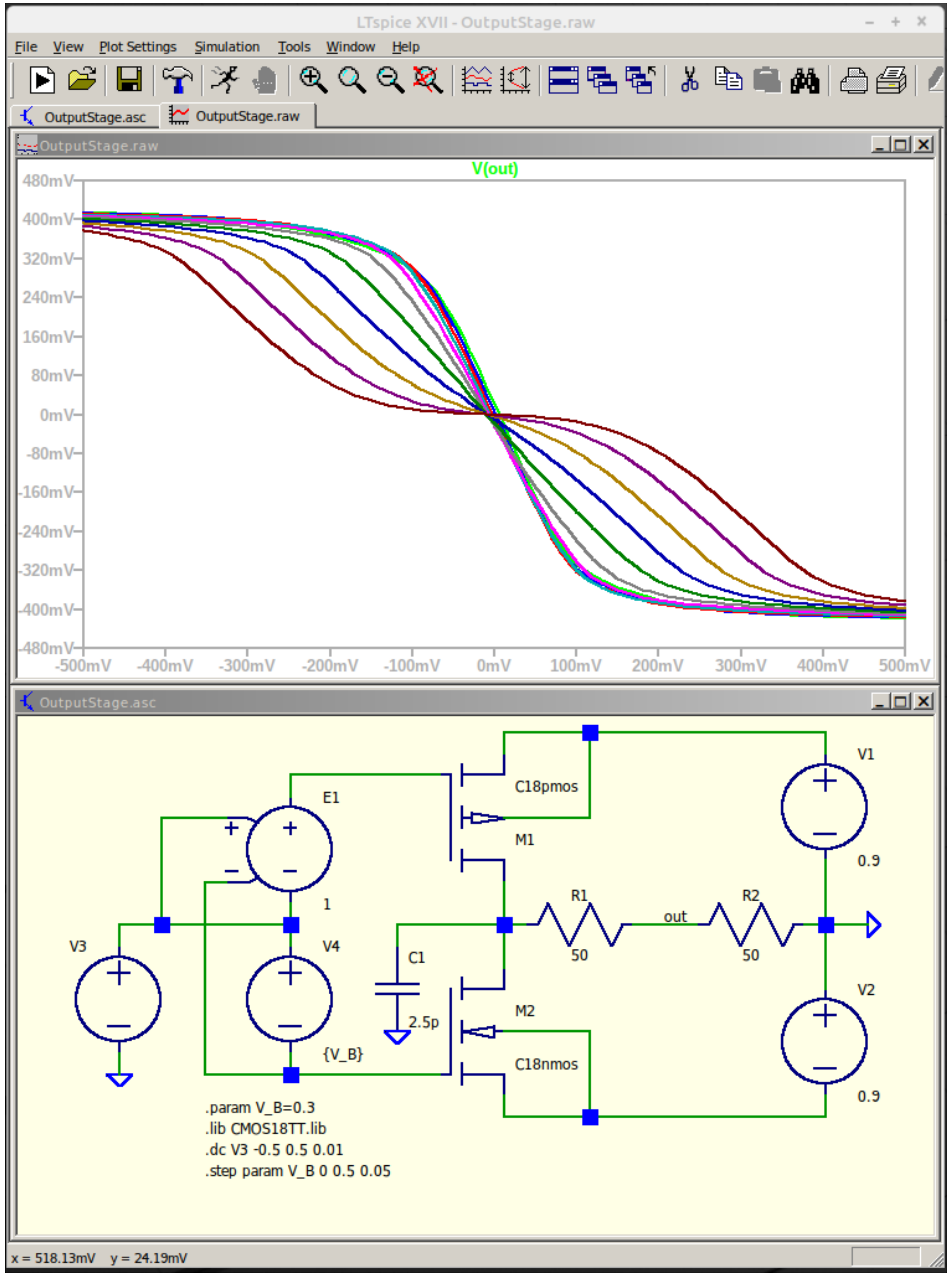
Smallest value for L: 180nm

Wpmos/Wnmos = 1/mobility_ratio

Determine W and M such that the load can be driven with a sufficiently small drive (V3)

PMOS: W=40u, M=10
NMOS: W=40u, M=3
Bias voltage 0.2V

CS output stage design



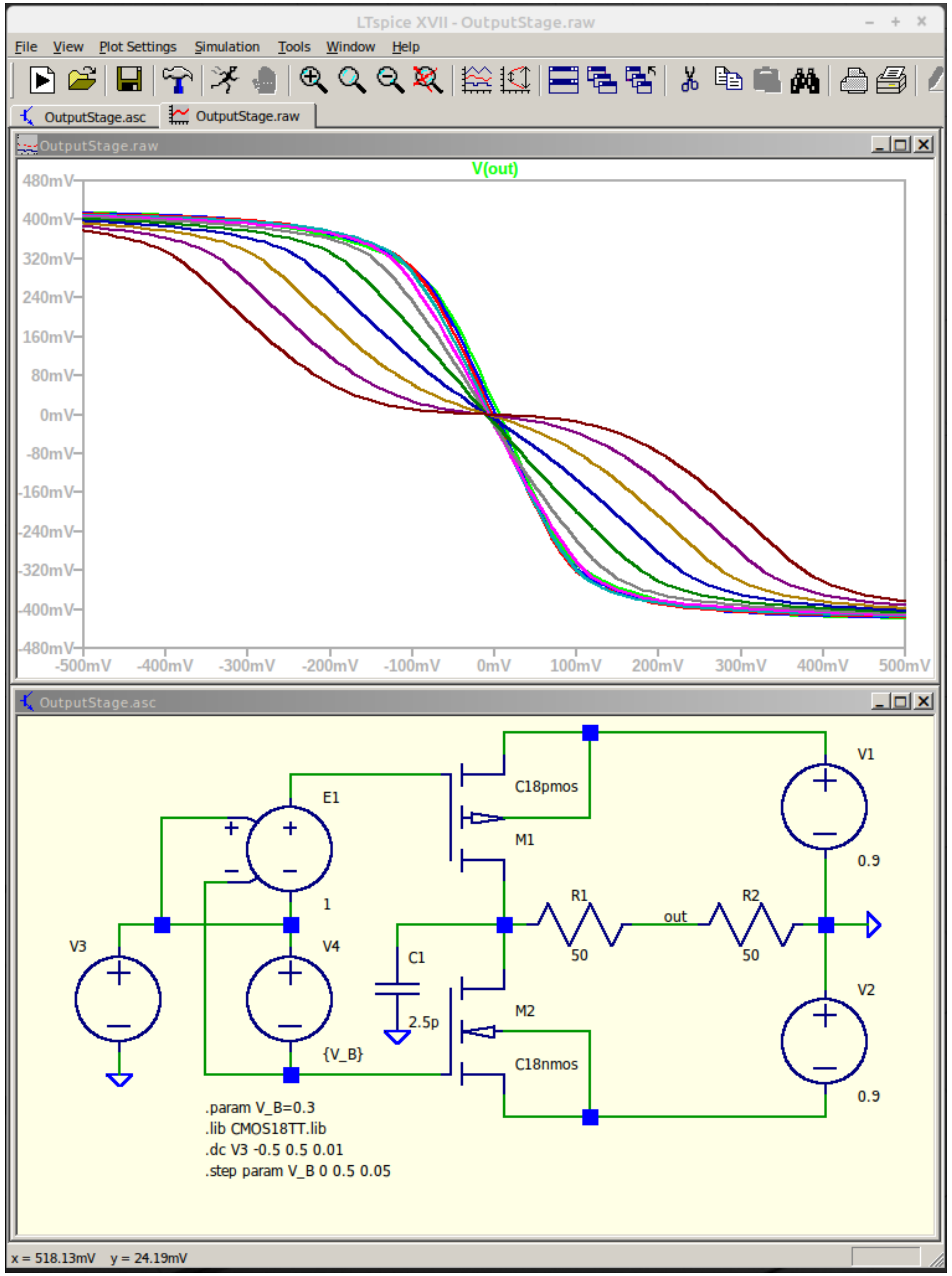
Smallest value for L: 180nm

Wpmos/Wnmos = 1/mobility_ratio

Determine W and M such that the load can be driven with a sufficiently small drive (V3)

PMOS: W=40u, M=10
NMOS: W=40u, M=3
Bias voltage 0.2V
Quiescent current 1mA

CS output stage design



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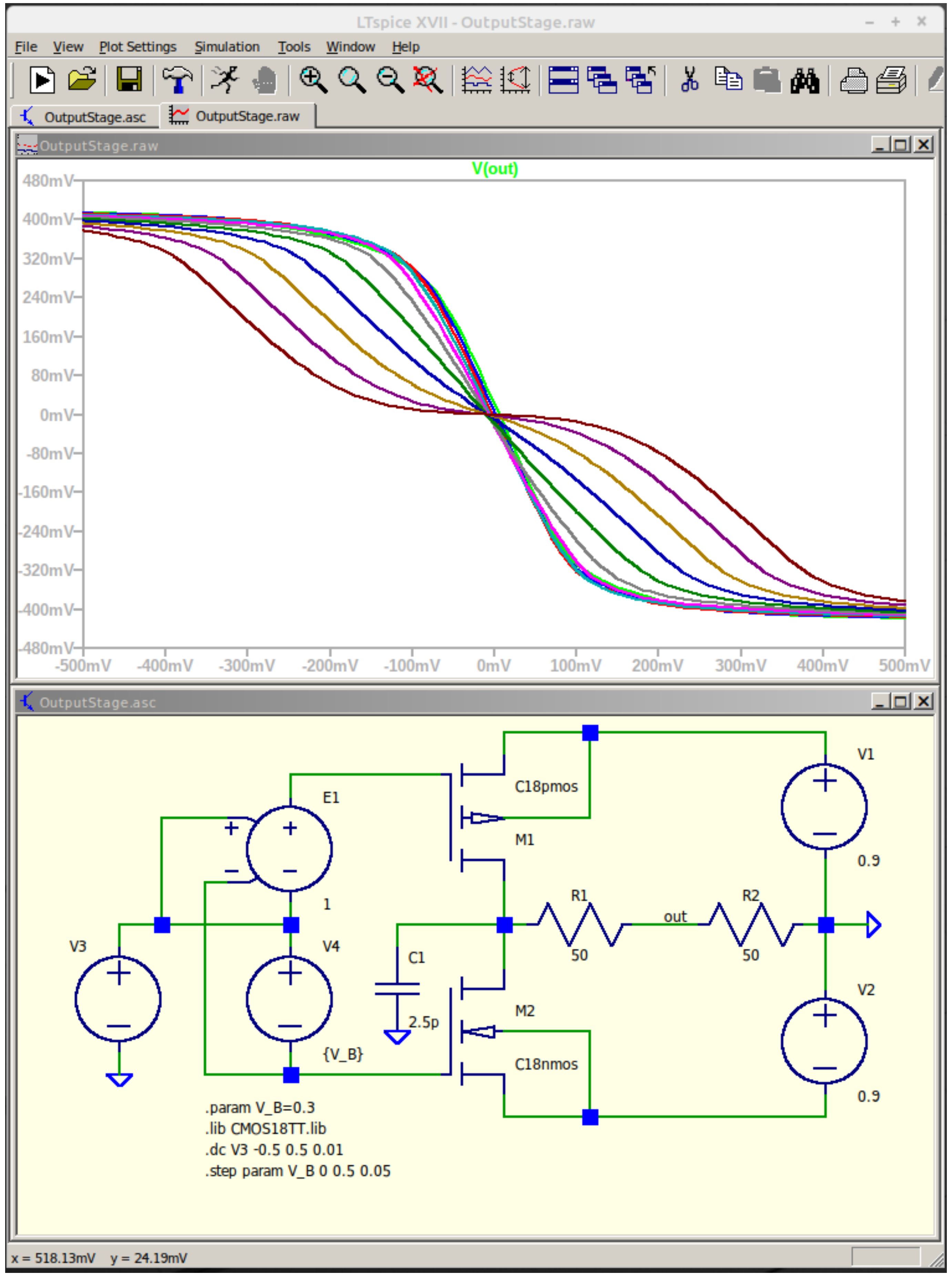
Quiescent current 1mA
Drive requirement +/- 0.2V

CS output stage design



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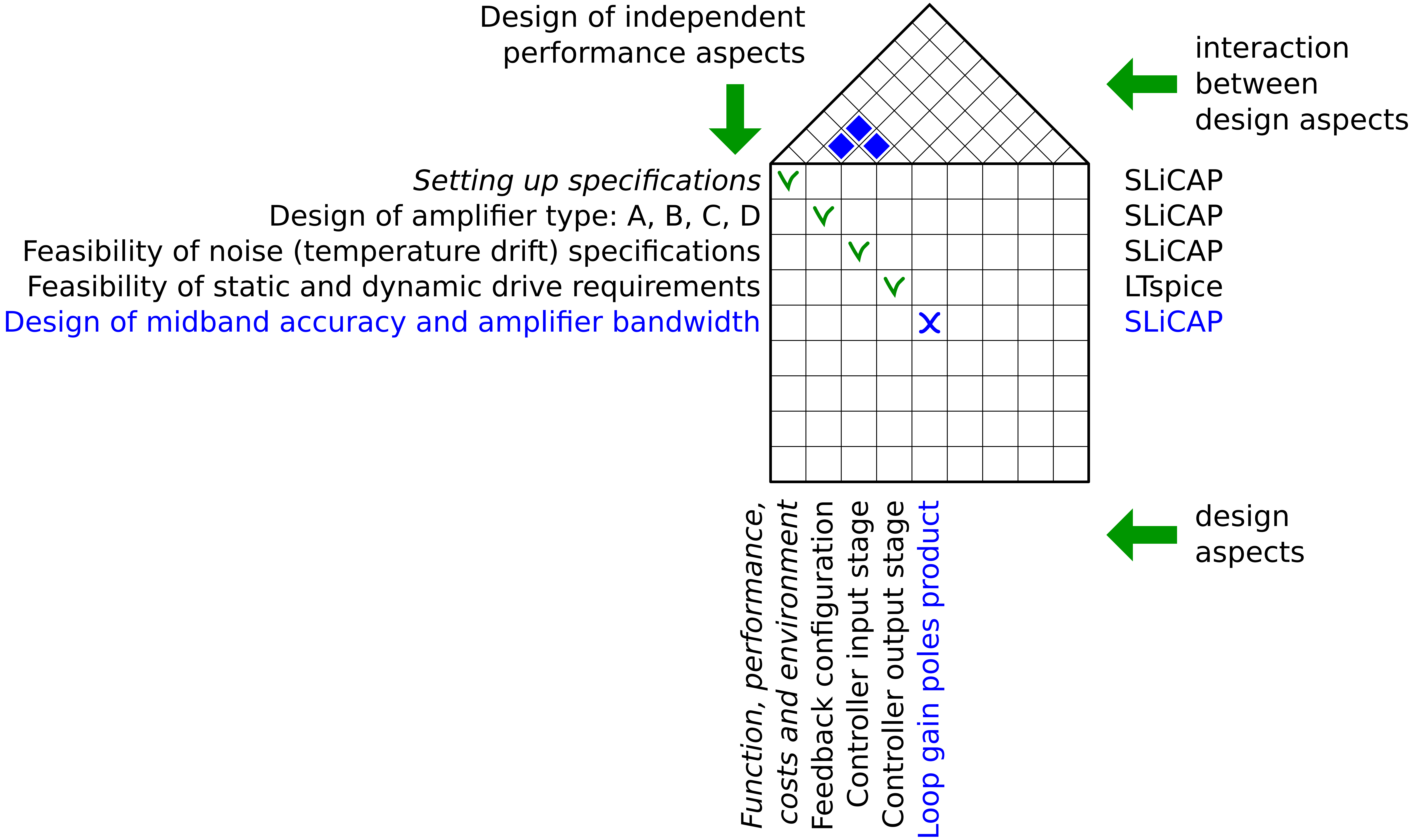
Bias voltage 0.2V
Quiescent current 1mA
Drive requirement +/- 0.2V

Structured Electronic Design

Step 5
Design of mid-band accuracy and bandwidth

Anton J.M. Montagne



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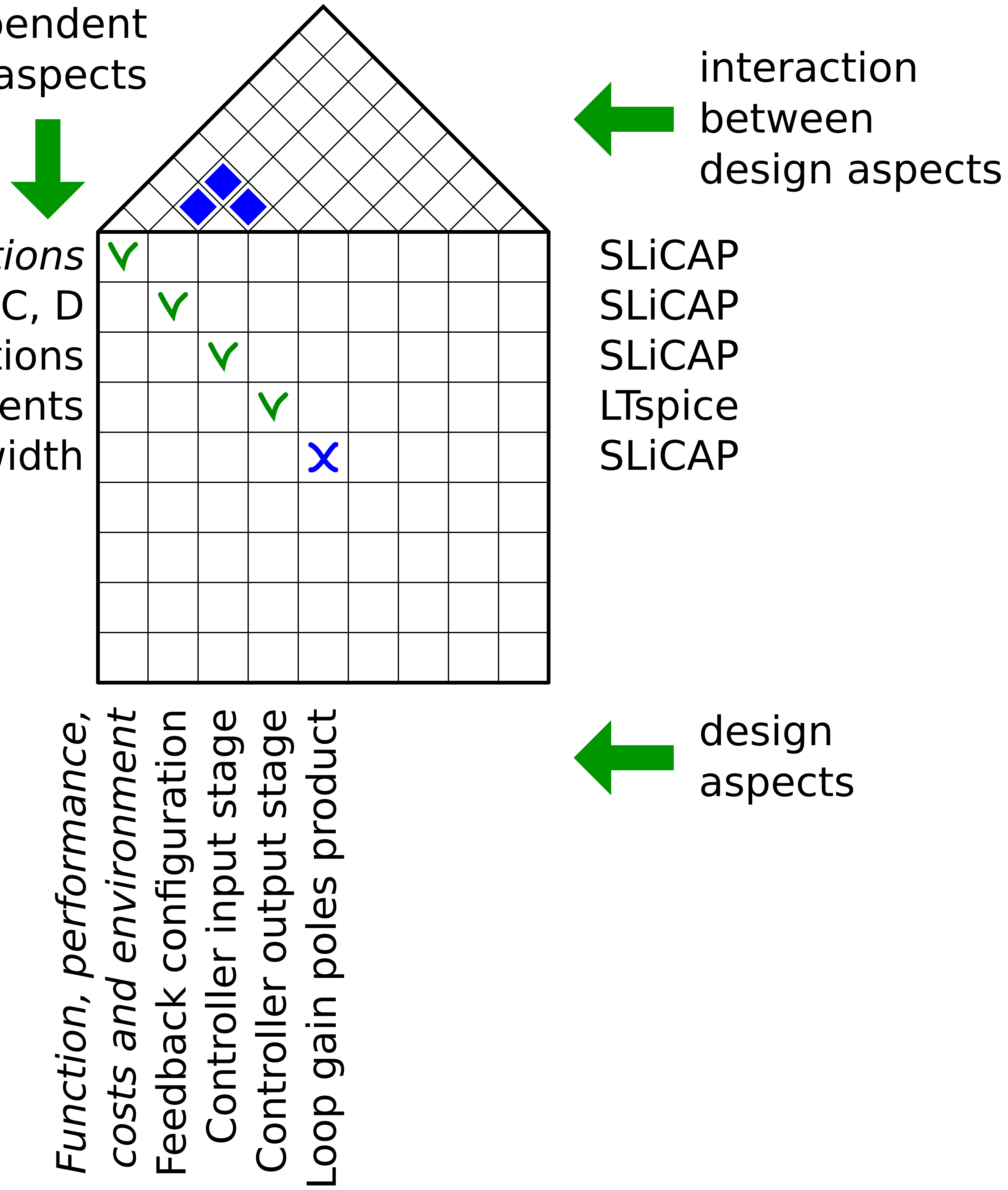
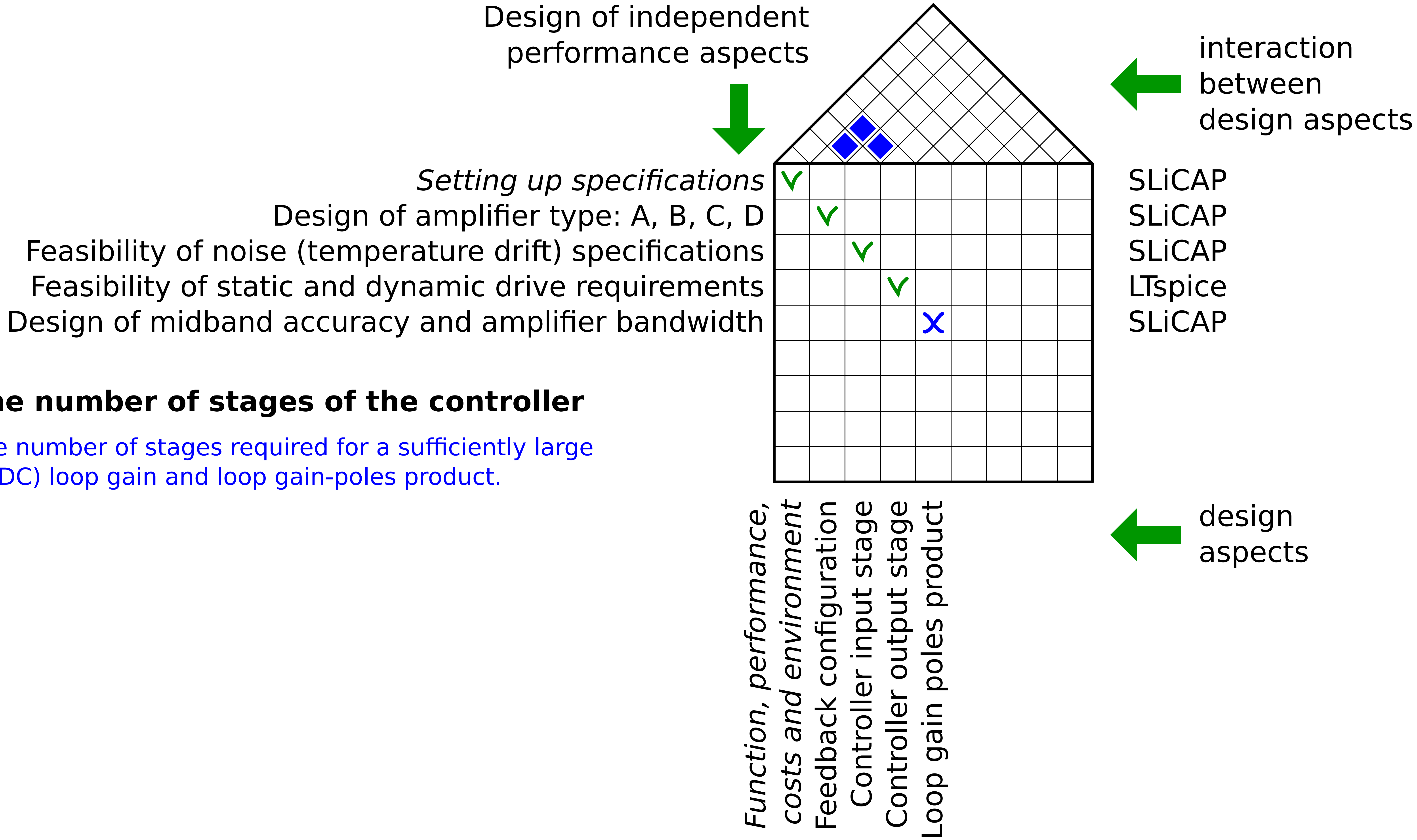
Loop gain poles product
design
aspects

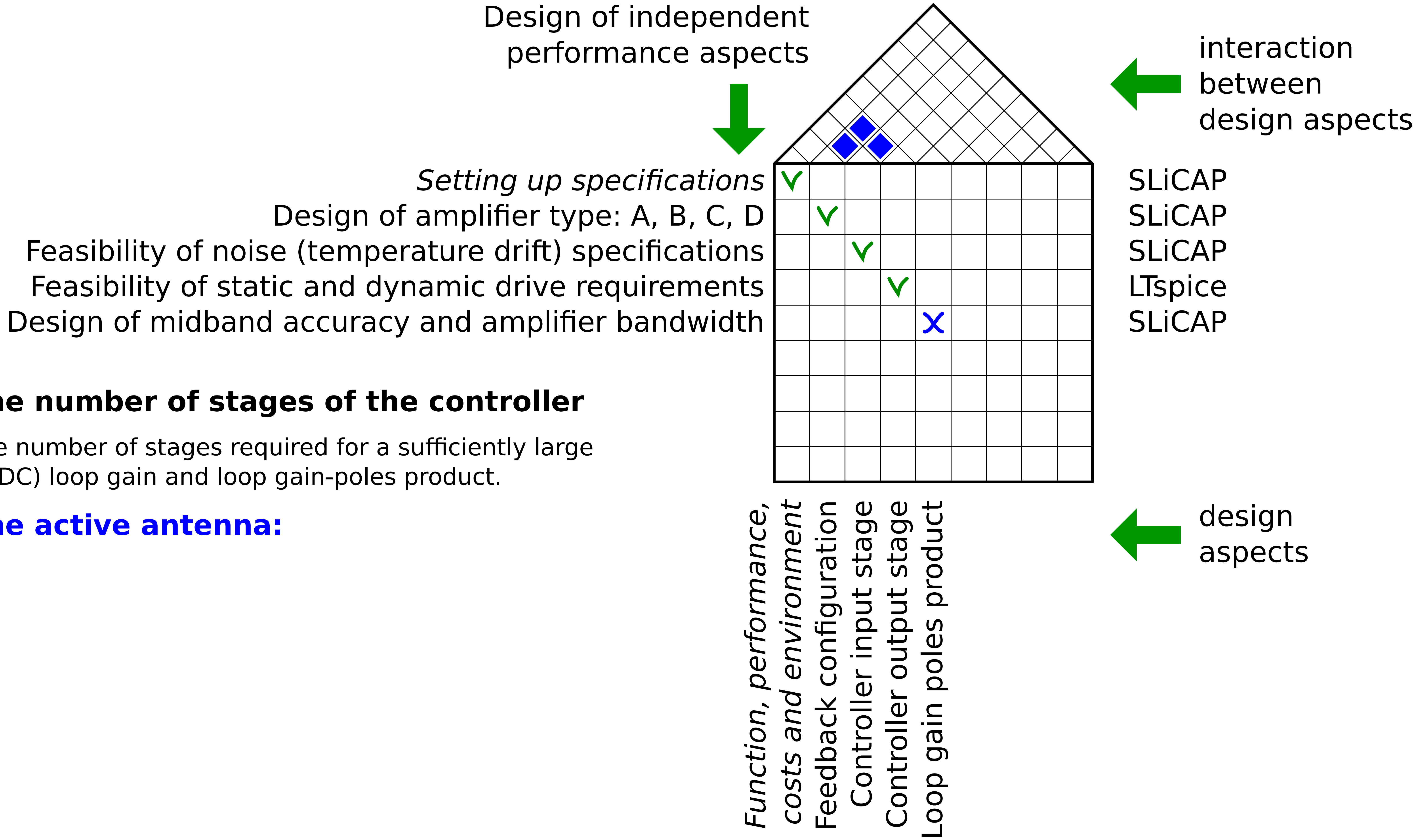
Design of the number of stages of the controller



Design of the number of stages of the controller

Determine the number of stages required for a sufficiently large mid-band (or DC) loop gain and loop gain-poles product.

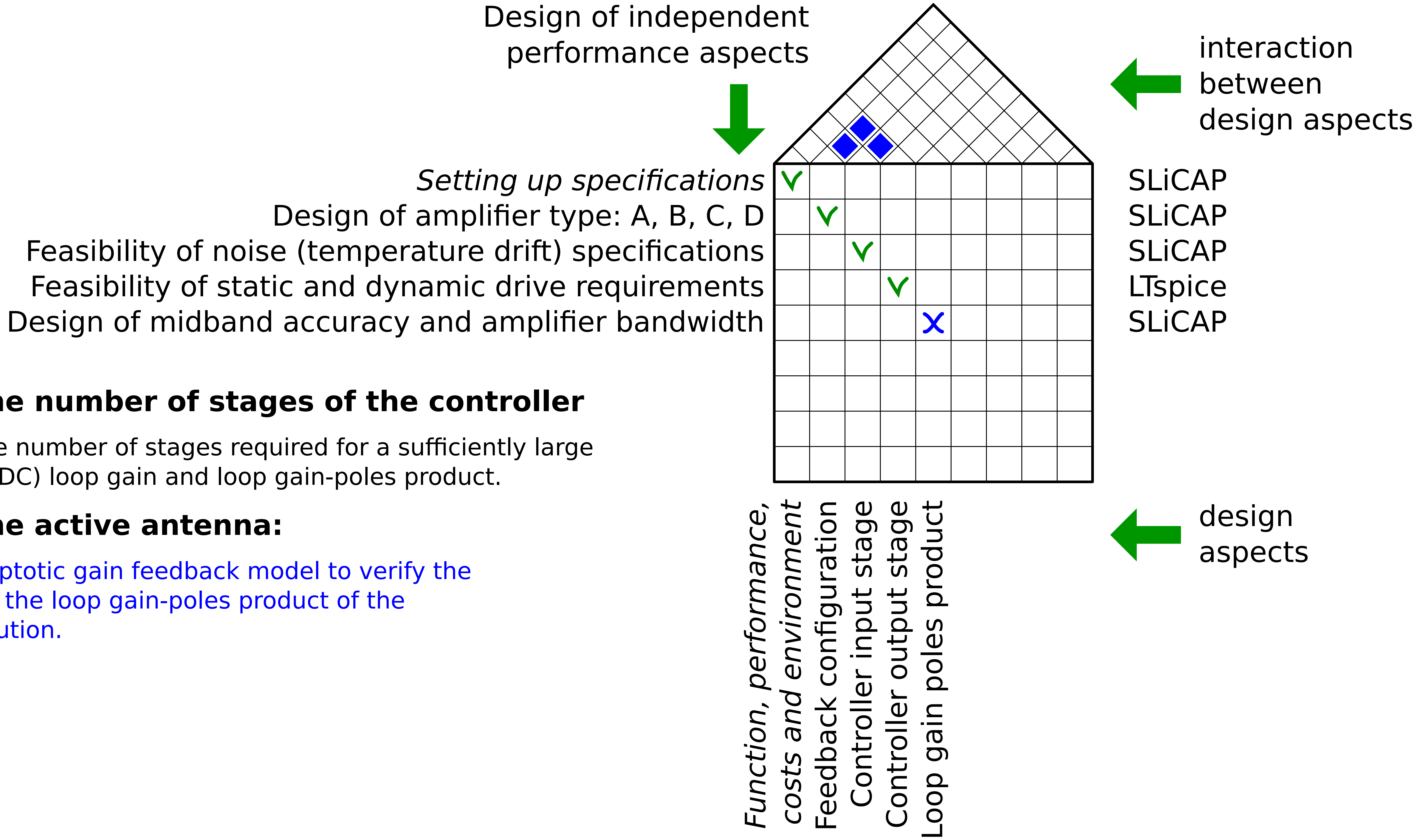




Design of the number of stages of the controller

Determine the number of stages required for a sufficiently large mid-band (or DC) loop gain and loop gain-poles product.

Design of the active antenna:

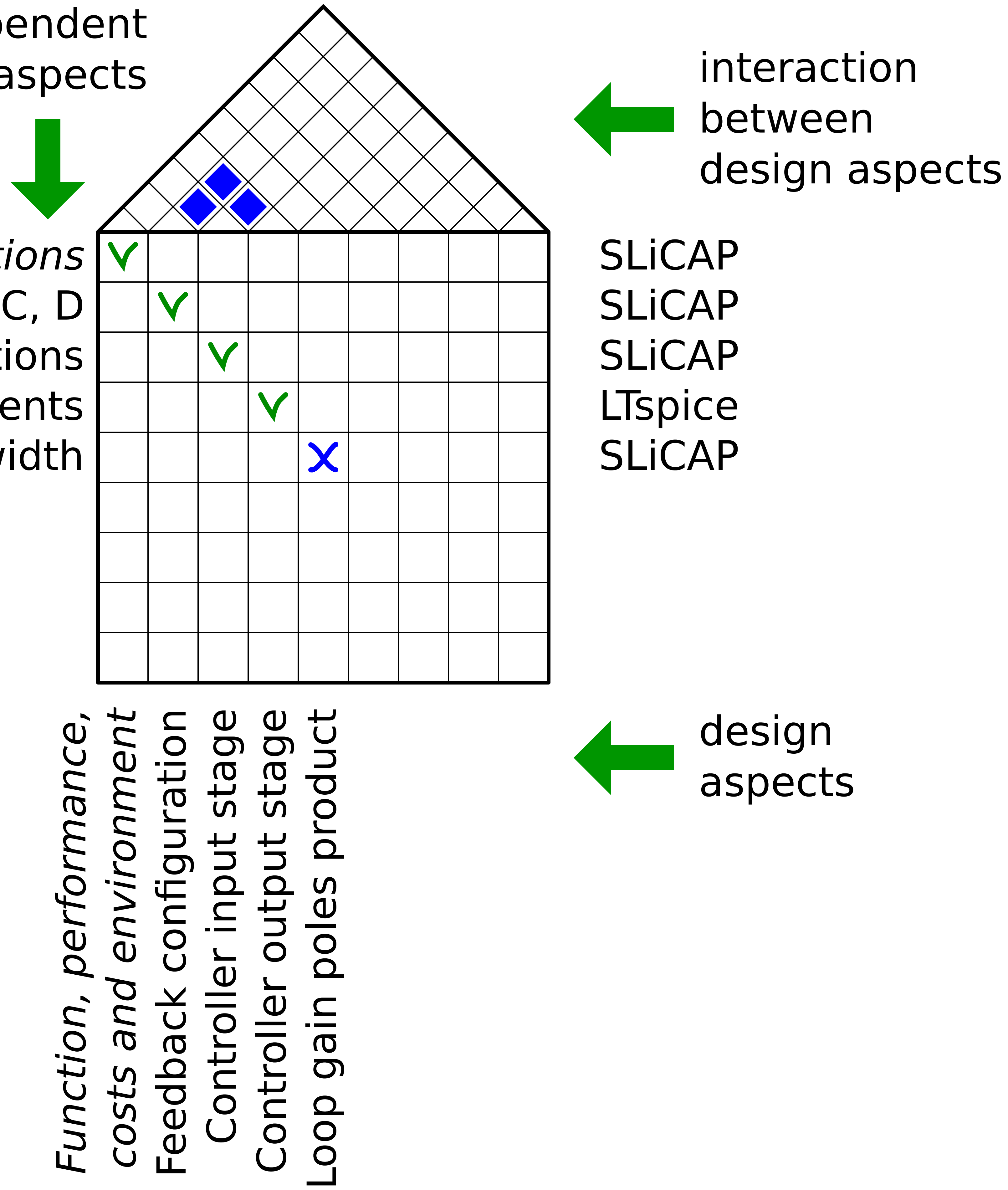


Design of the number of stages of the controller

Determine the number of stages required for a sufficiently large mid-band (or DC) loop gain and loop gain-poles product.

Design of the active antenna:

Use the asymptotic gain feedback model to verify the loop gain and the loop gain-poles product of the two-stage solution.



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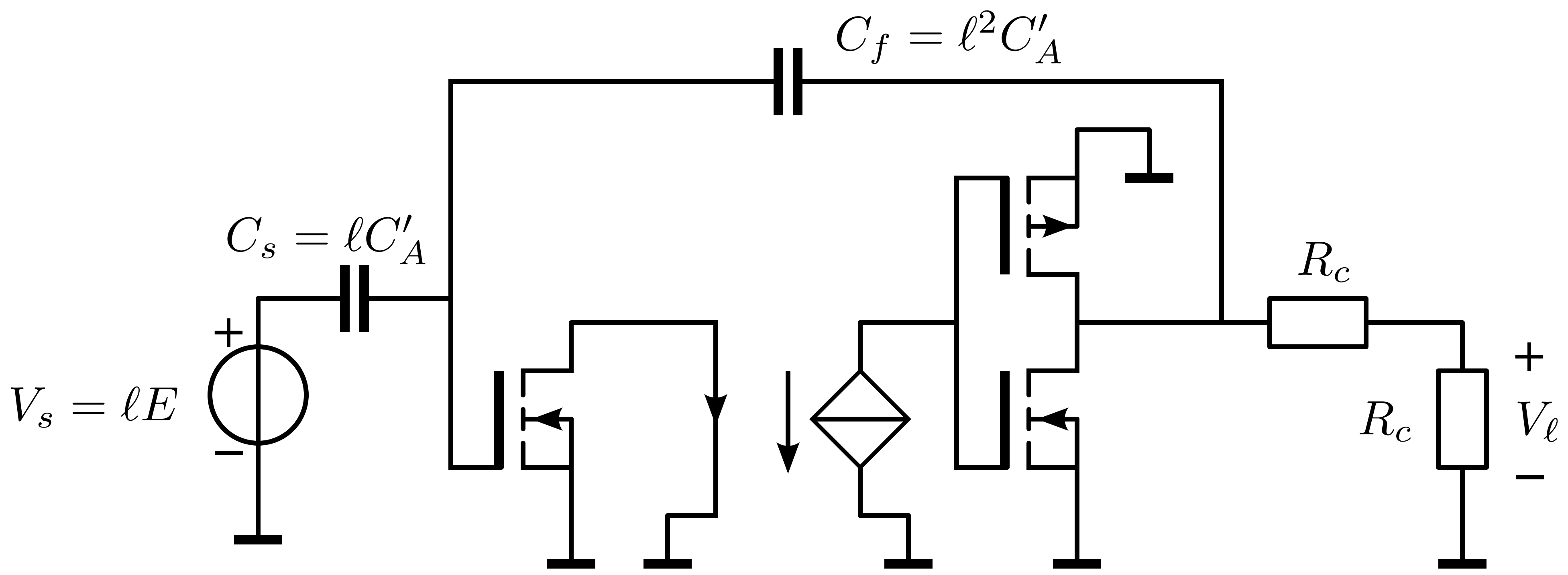
Bandwidth design

Bandwidth design



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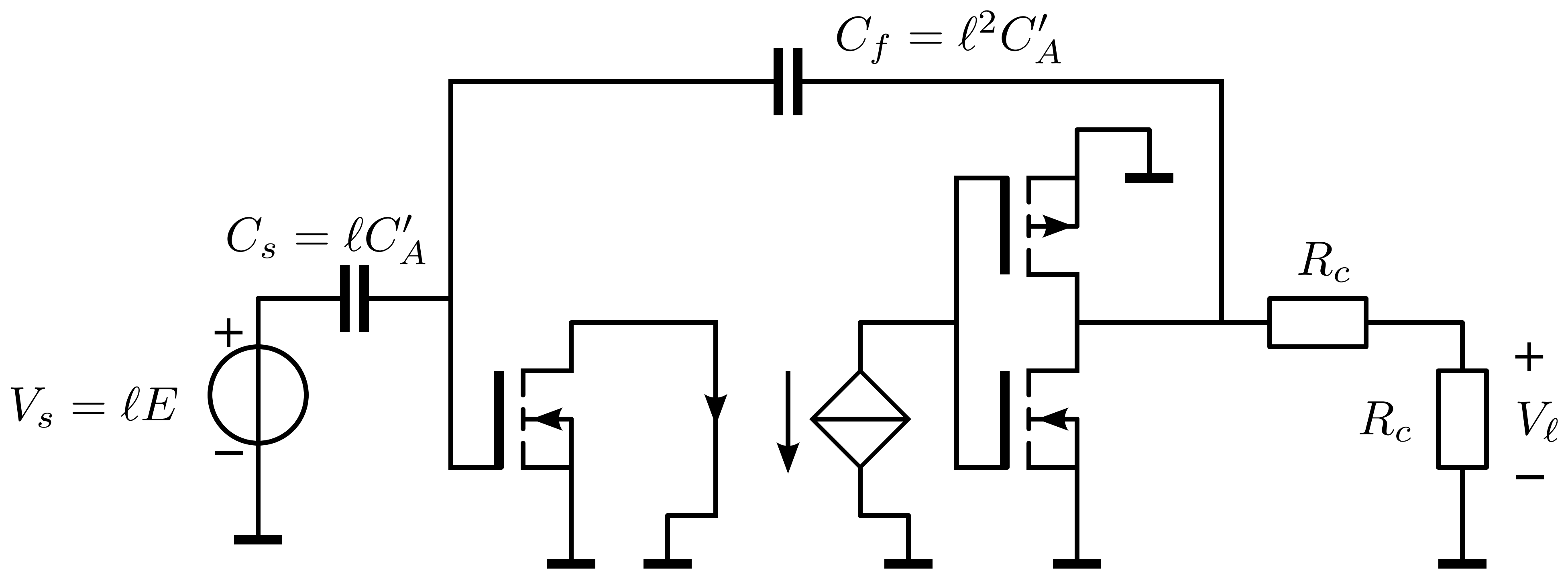

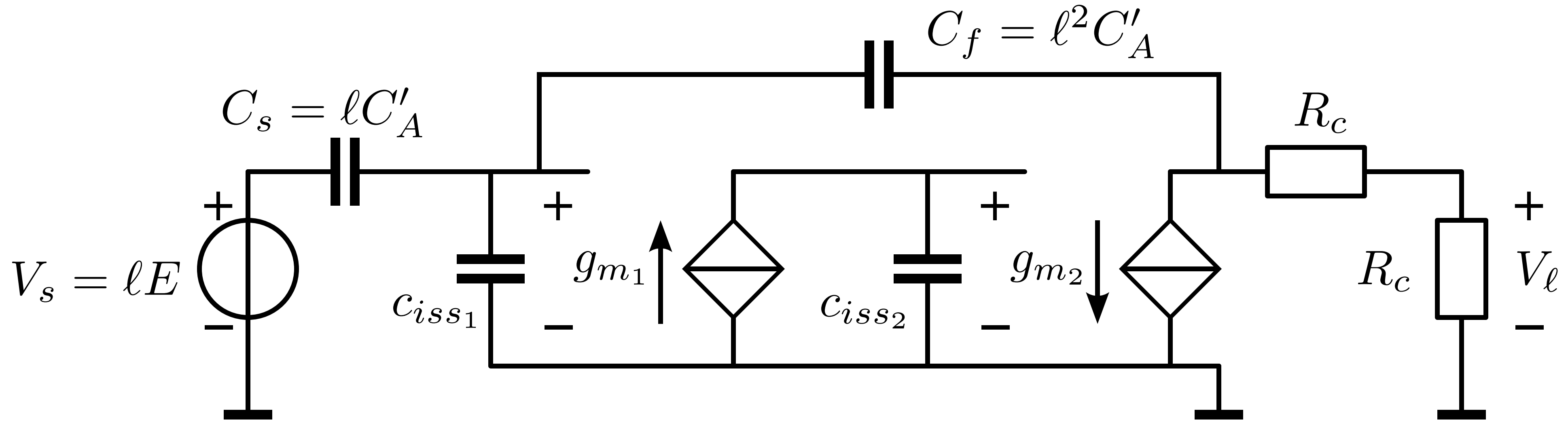

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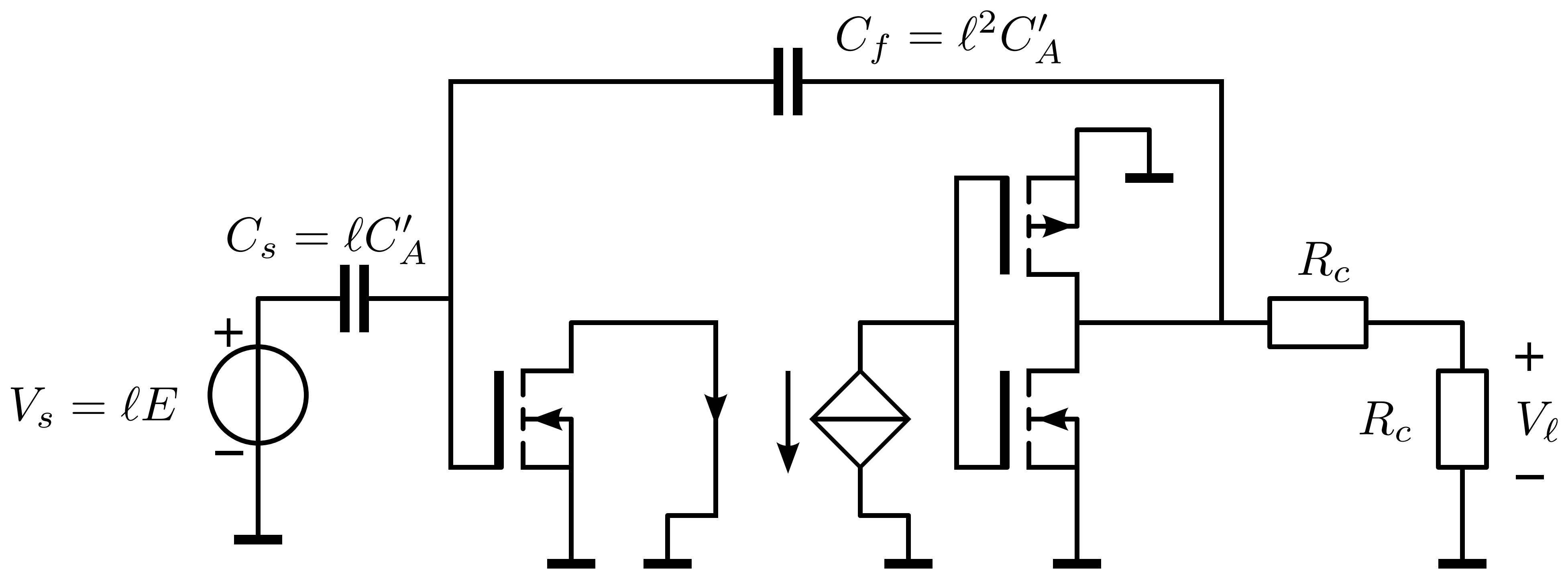
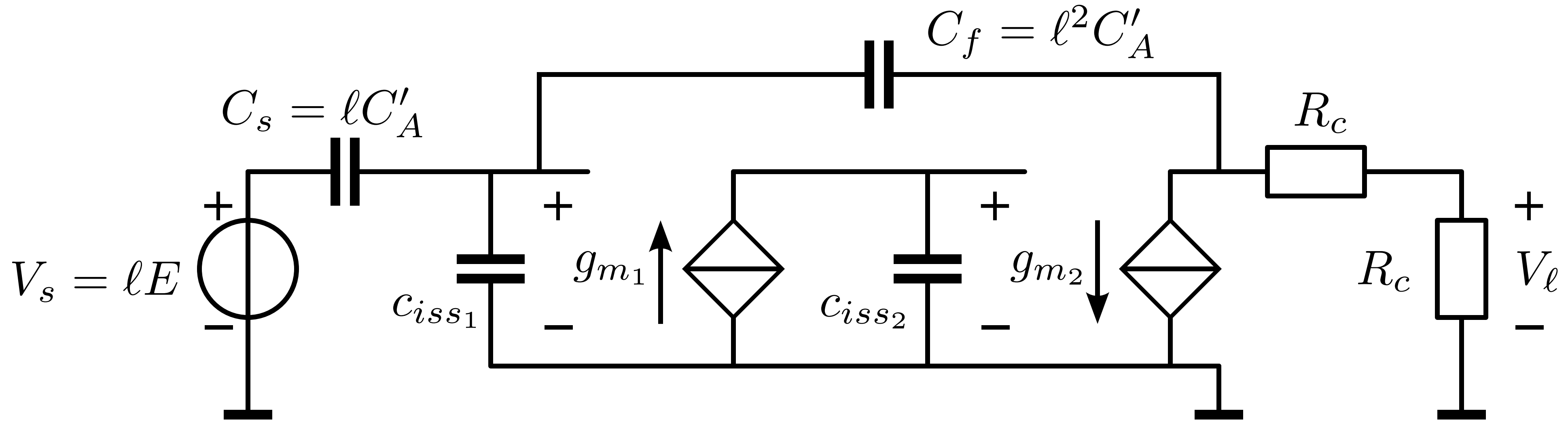
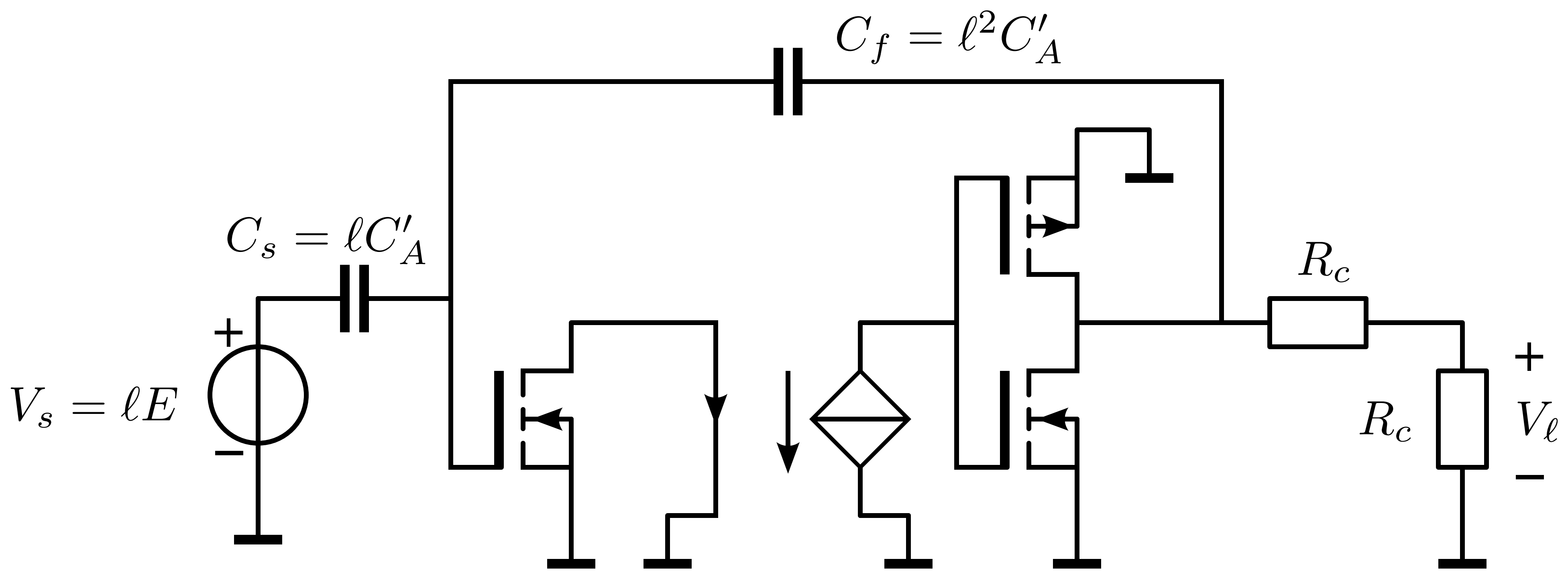
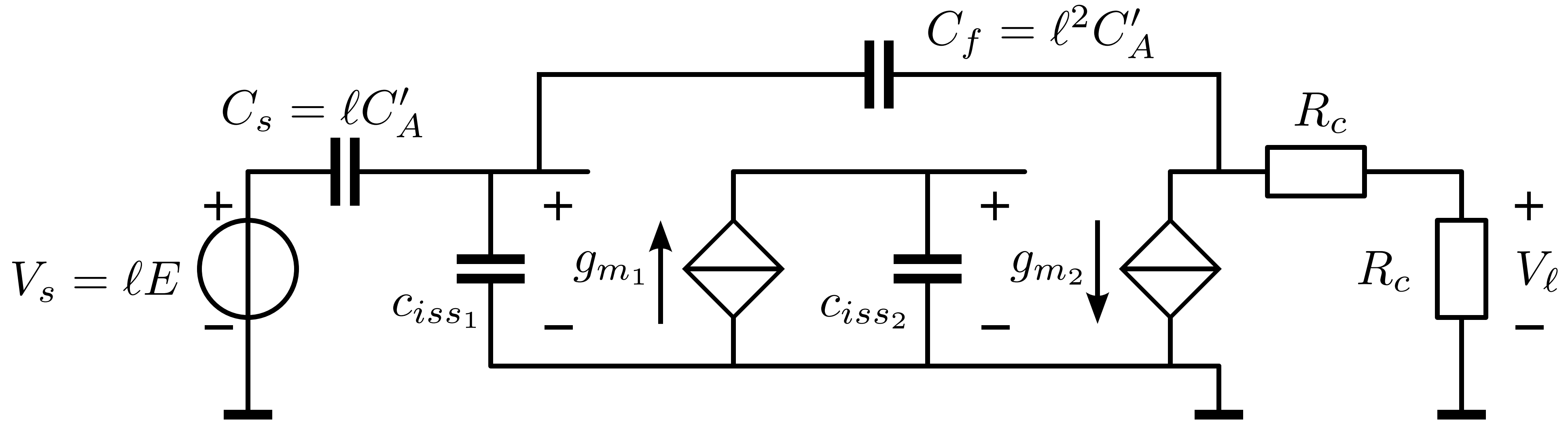




Loop gain, ref: g_{m_1}

Bandwidth design

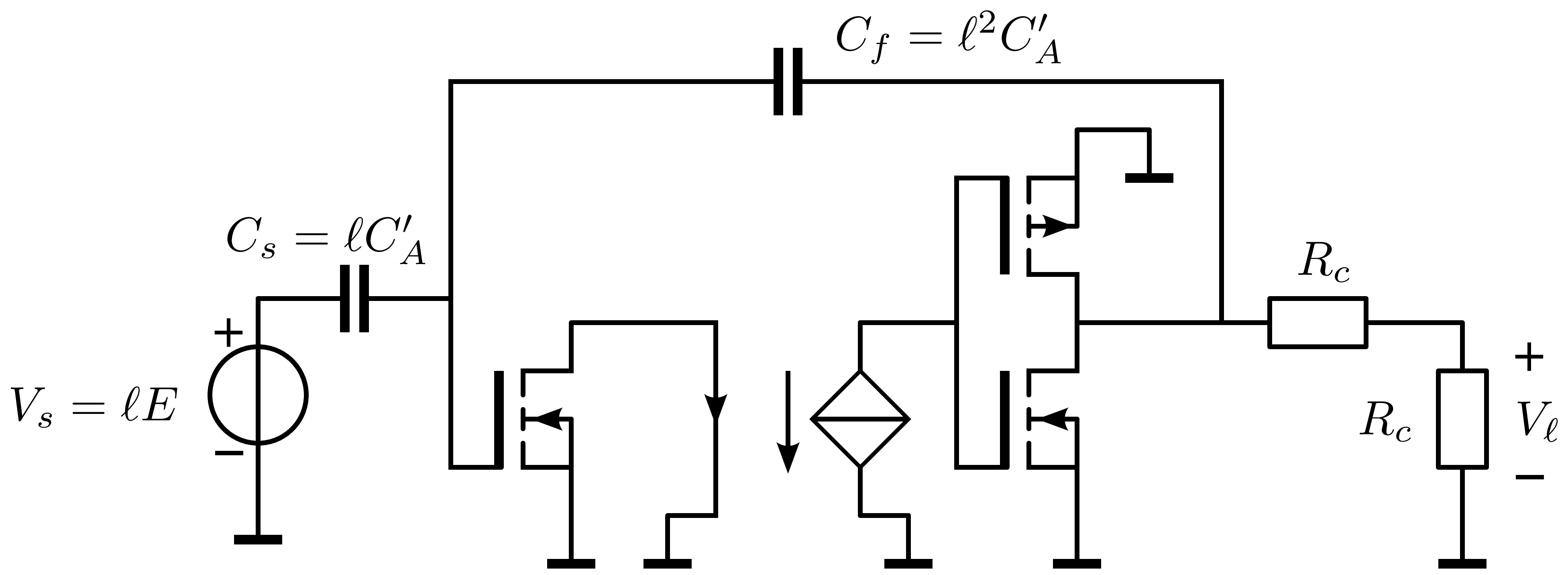


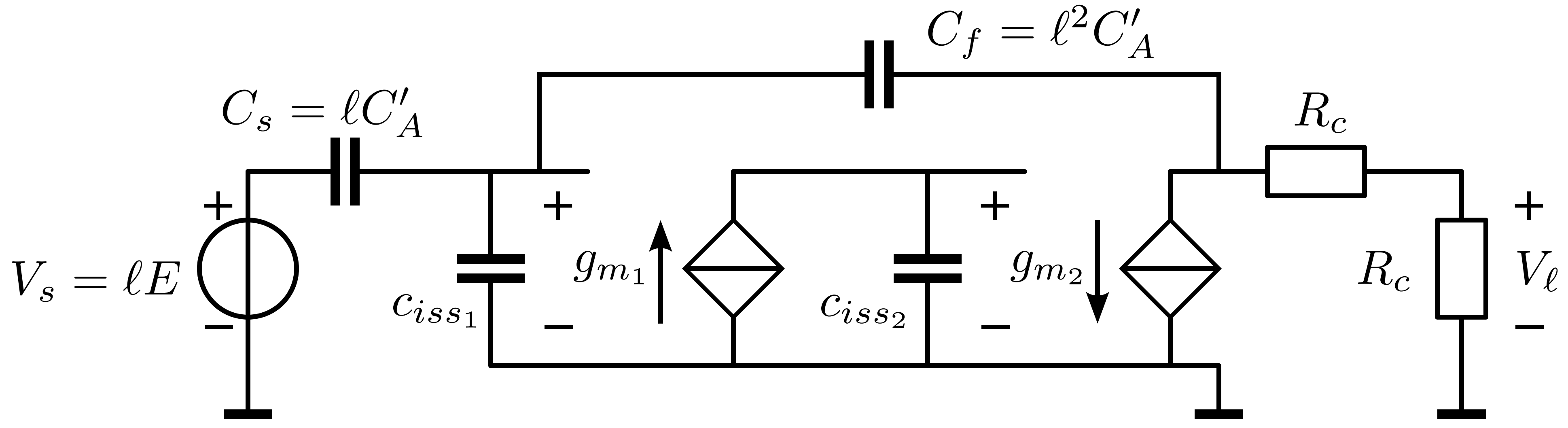


Loop gain, ref: g_{m_1}

$$L = -\frac{2 g_{m_1} g_{m_2} R_c \frac{C_f}{C_f + C_s + c_{iss_1}}}{s c_{iss_2} \left(1 + s 2 R_c \frac{C_f \left(C_s + c_{iss_1}\right)}{C_f + C_s + c_{iss_1}}\right)}$$

Bandwidth design





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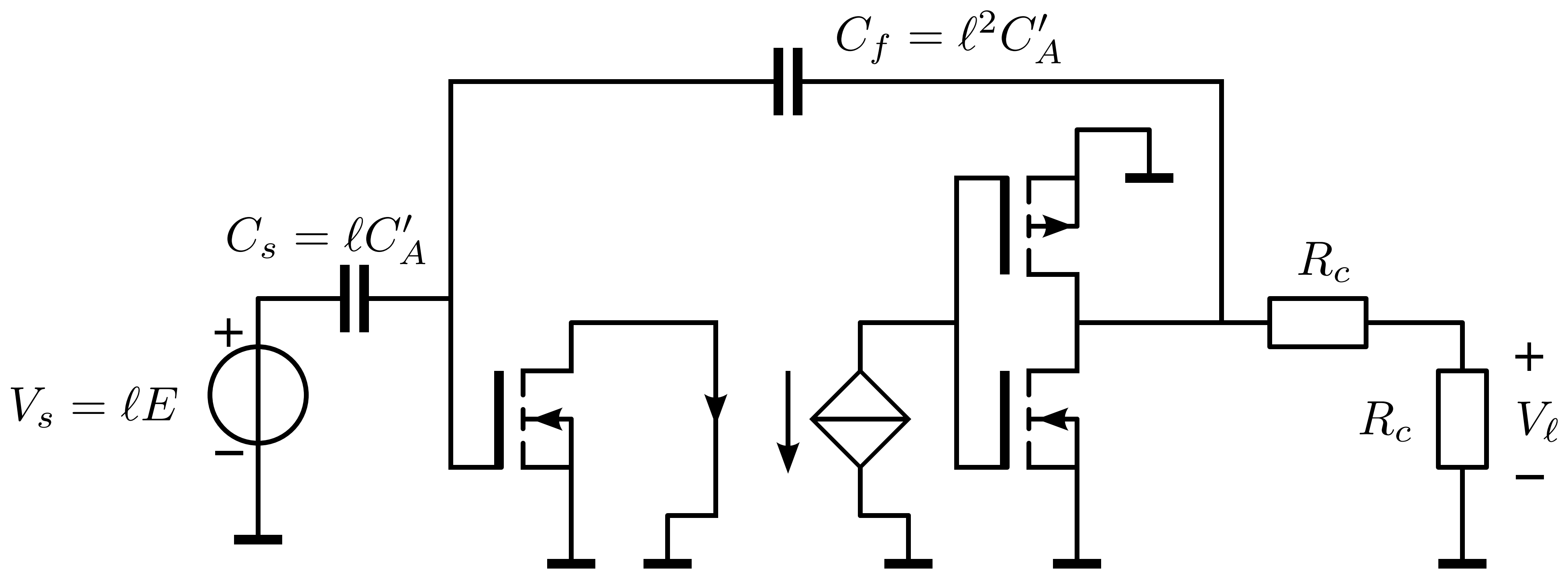
Second-order loop gain-poles product:

Bandwidth design



Loop gain, ref: g_{m_1}

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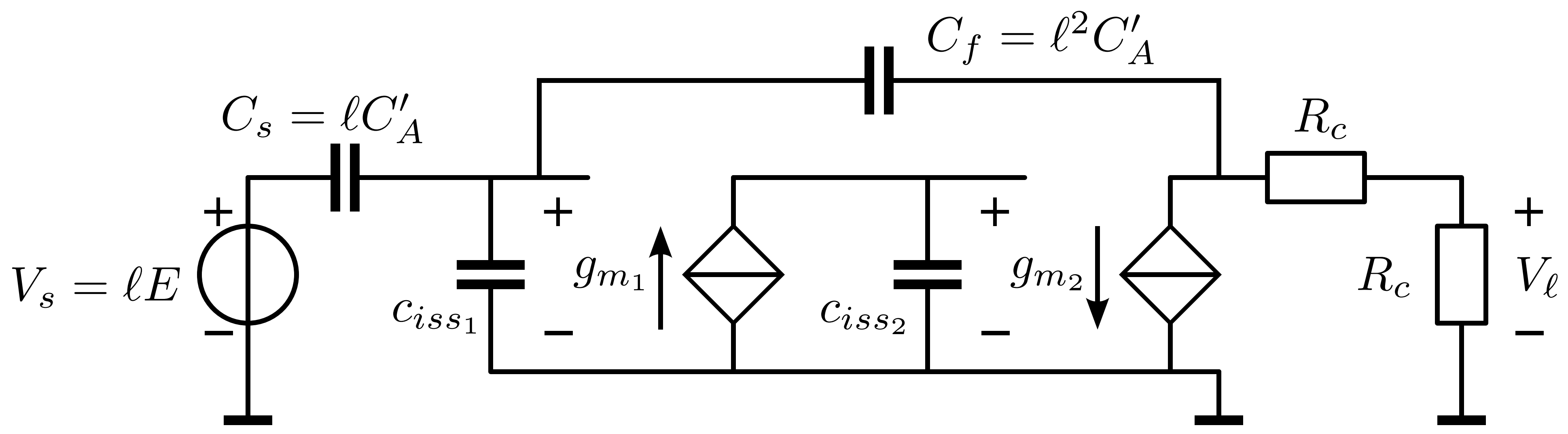
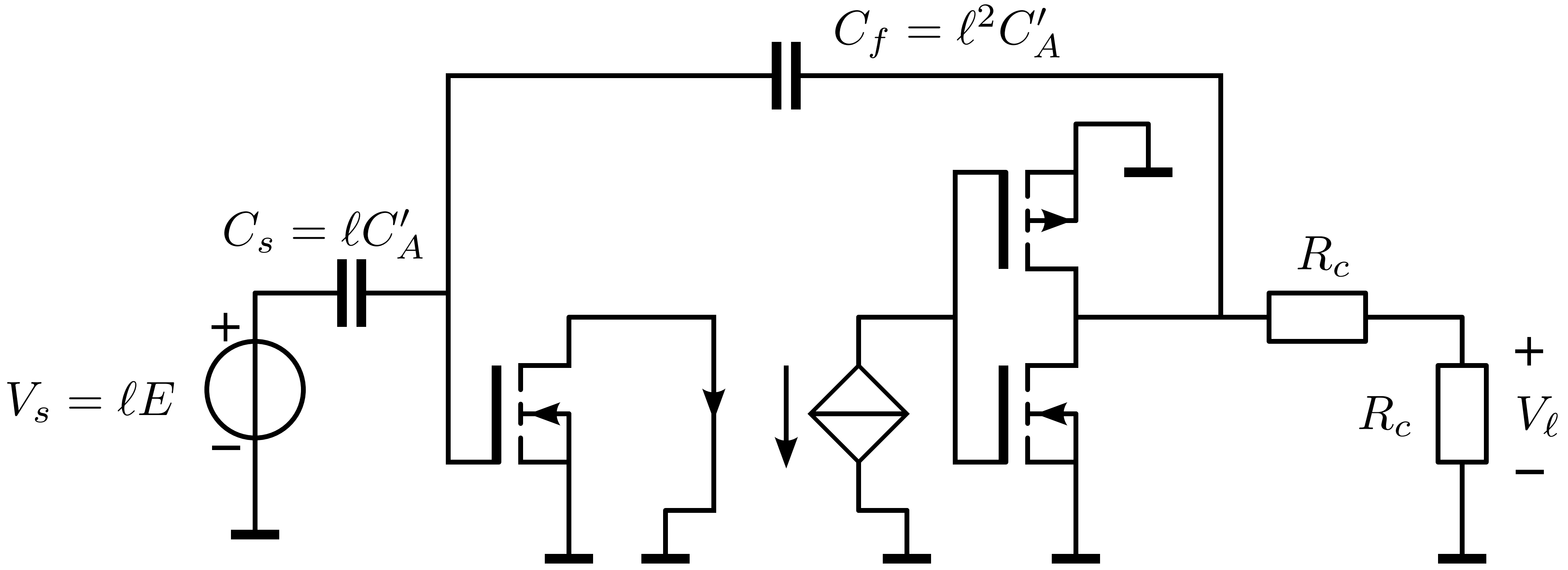
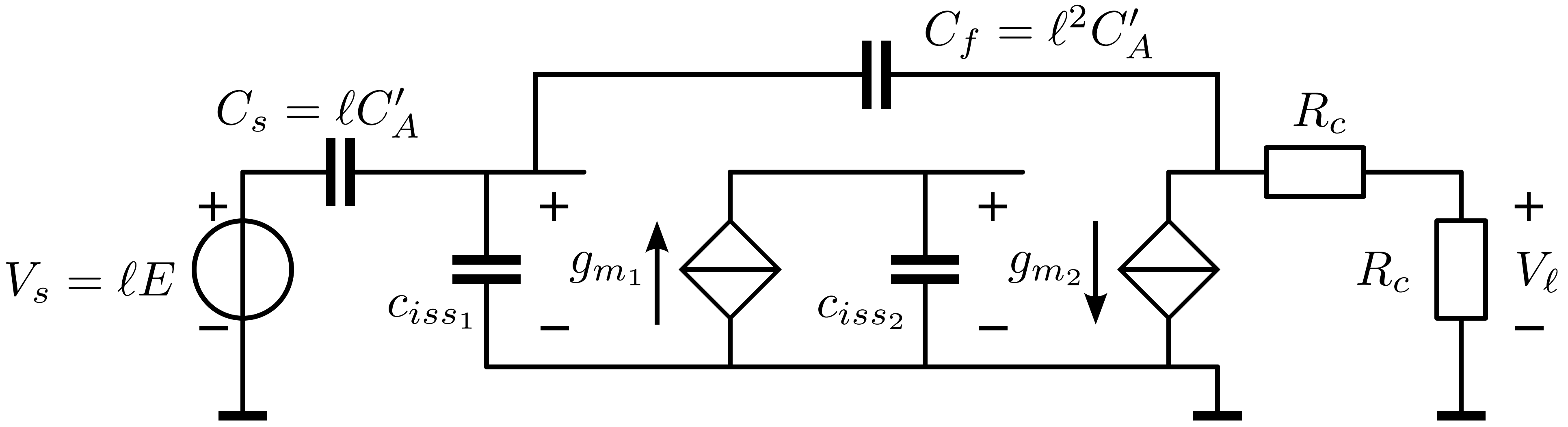
Second-order loop gain-poles product:

$$LP_2 = \frac{g_{m_1} g_{m_2}}{c_{iss_2}\left(C_s + c_{iss_1}\right)}$$



Bandwidth design





Loop gain, ref: g_{m_1}

$$L = -\frac{2 g_{m_1} g_{m_2} R_c \frac{C_f}{C_f + C_s + c_{iss_1}}}{s c_{iss_2}\left(1 + s 2 R_c \frac{C_f\left(C_s + c_{iss_1}\right)}{C_f + C_s + c_{iss_1}}\right)}$$

Second-order loop gain-poles product:

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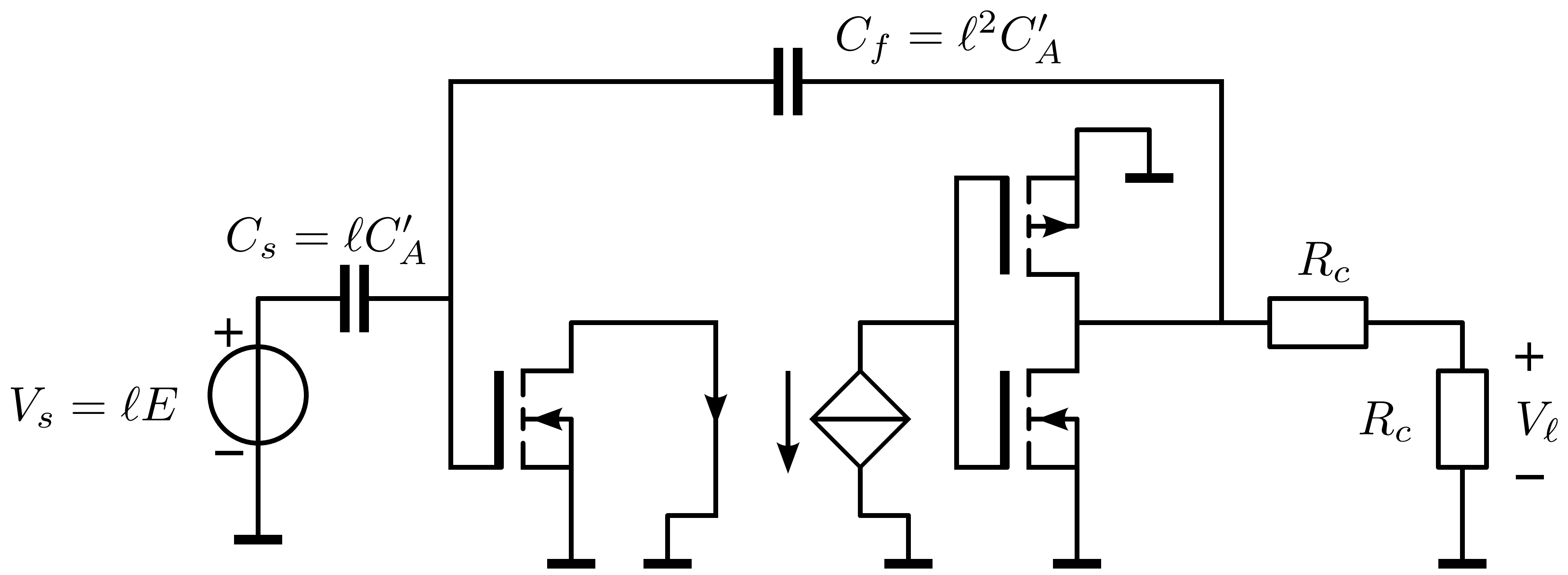
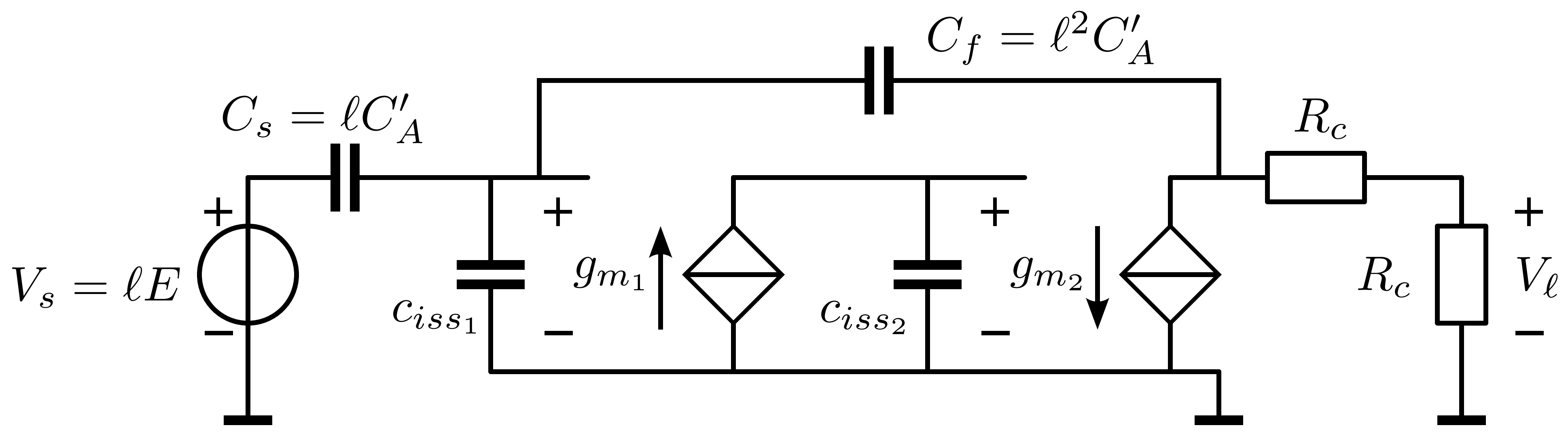
Circuit element values:

Bandwidth design





Loop gain, ref: g_{m_1}

$$L = -\frac{2g_{m_1}g_{m_2}R_c\frac{C_f}{C_f+C_s+c_{iss_1}}}{sc_{iss_2}\left(1+s2R_c\frac{C_f\left(C_s+c_{iss_1}\right)}{C_f+C_s+c_{iss_1}}\right)}$$

Second-order loop gain-poles product:

$$LP_2 = \frac{g_{m_1}g_{m_2}}{c_{iss_2}\left(C_s+c_{iss_1}\right)}$$

Circuit element values:

$g_{m_1} = 23\text{m}$

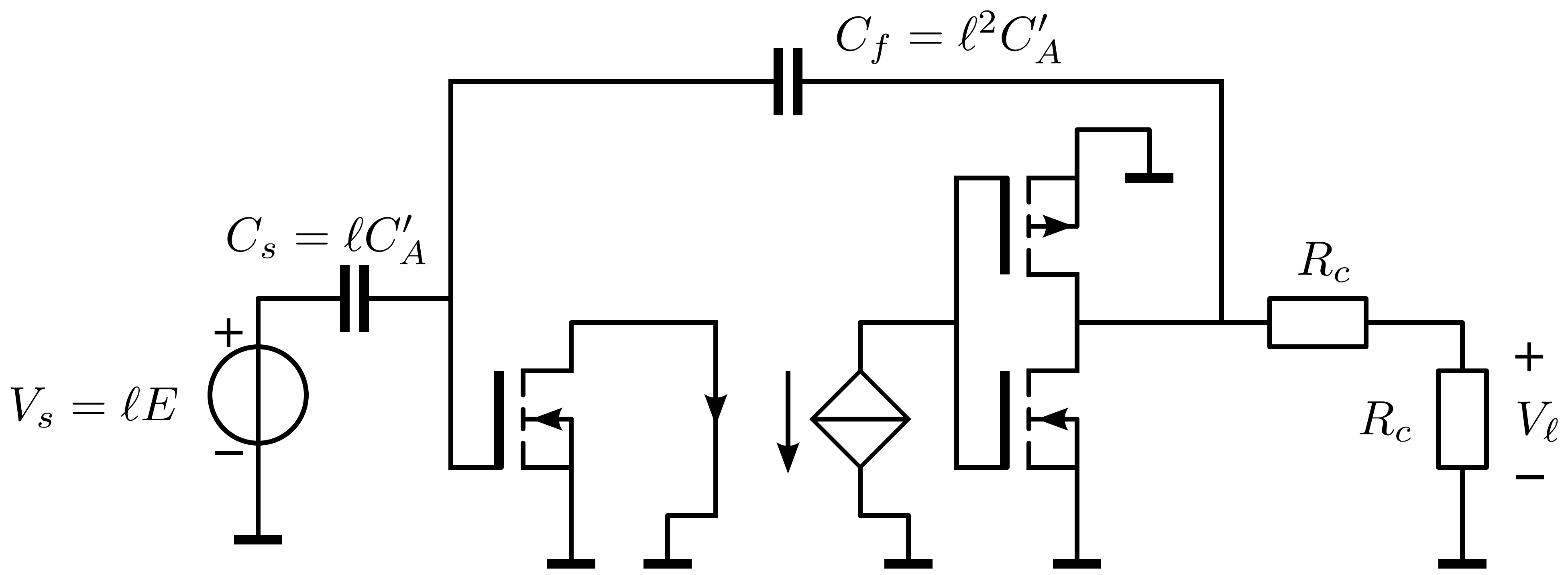
$g_{m_2} = 28\text{m}$

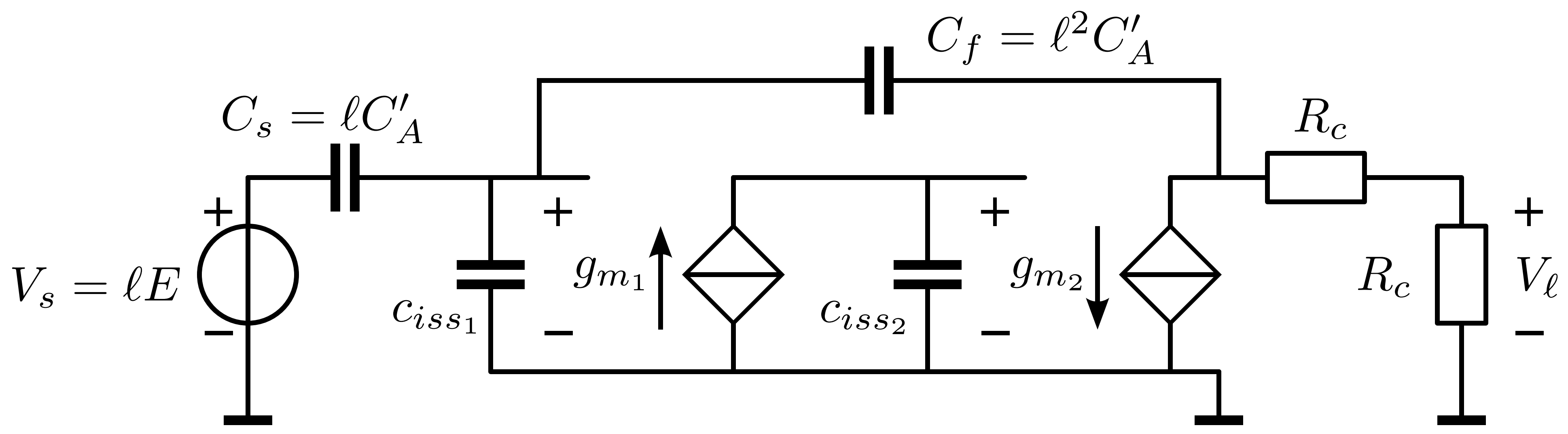
$C_s = 5\text{p}$

$c_{iss_1} = 1\text{p}$

$c_{iss_2} = 1.2\text{p}$

Bandwidth design





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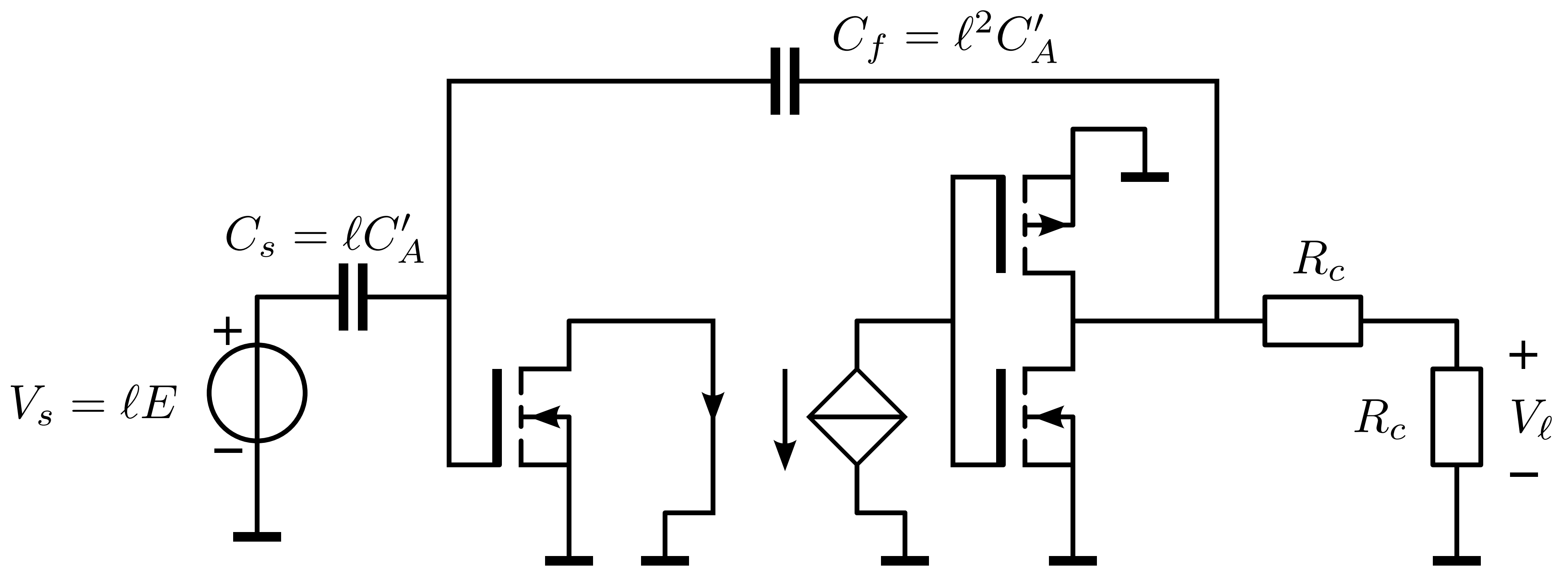
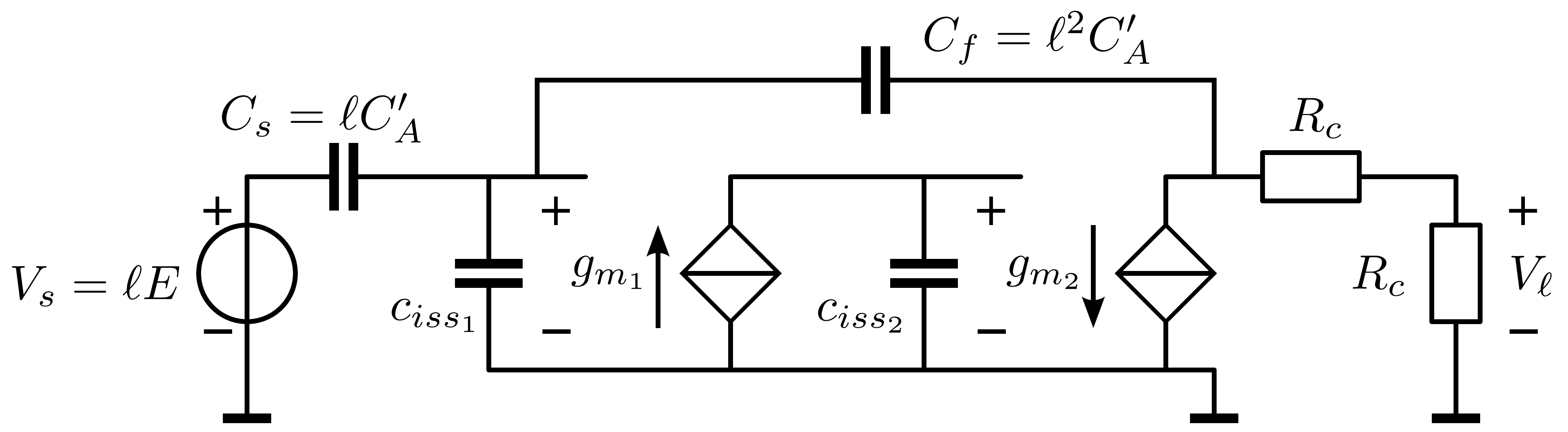
Achievable MFM bandwidth:

Bandwidth design





Loop gain, ref: g_{m_1}

$$L = -\frac{2 g_{m_1} g_{m_2} R_c \frac{C_f}{C_f + C_s + c_{iss_1}}}{s c_{iss_2}\left(1 + s 2 R_c \frac{C_f\left(C_s + c_{iss_1}\right)}{C_f + C_s + c_{iss_1}}\right)}$$

Second-order loop gain-poles product:

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Circuit element values:

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$$C_s = 5\text{p}$$
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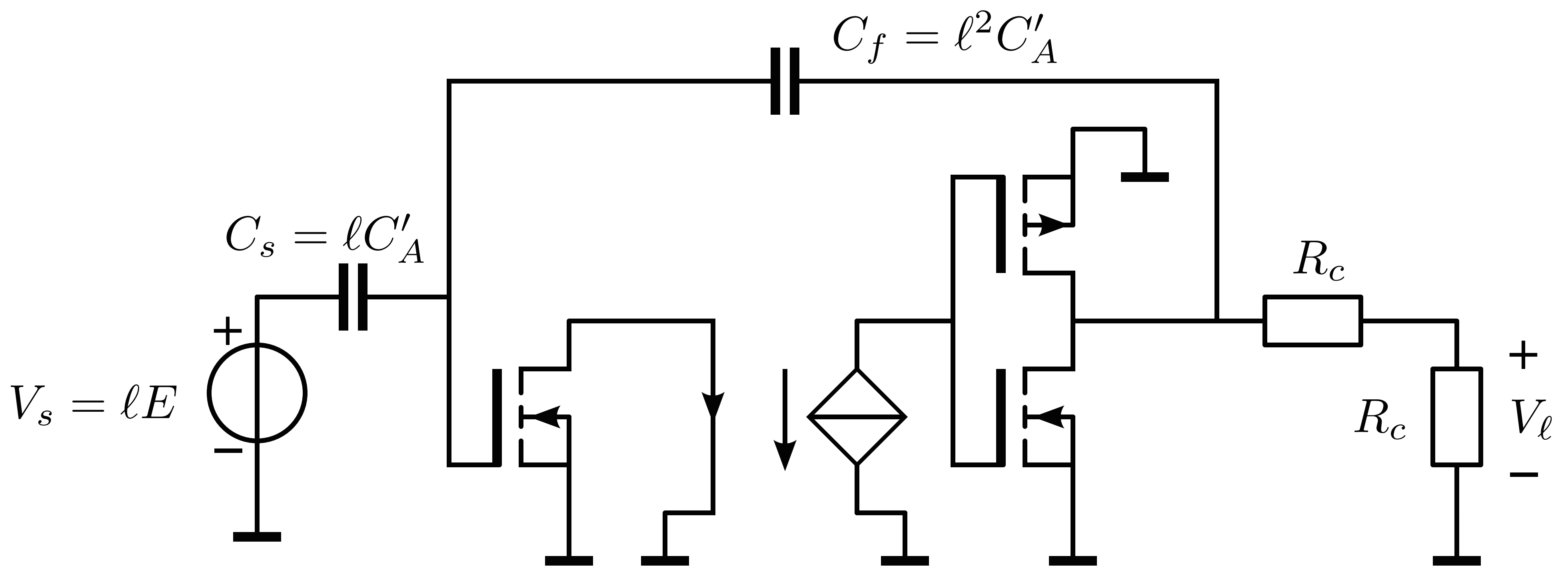
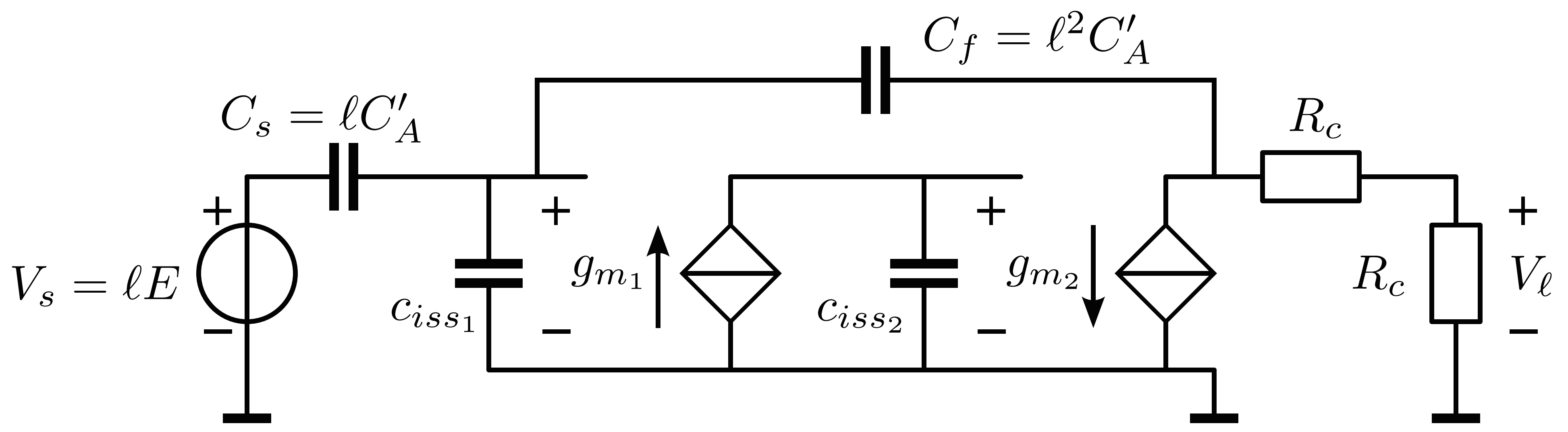
Achievable MFM bandwidth:

$$B_f = \frac{1}{2\pi}\sqrt{LP_2} = 1.5\text{GHz}$$

Bandwidth design





Loop gain, ref: g_{m_1}

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$$C_s = 5\text{p}$$
$$c_{iss_1} = 1\text{p}$$
$$c_{iss_2} = 1.2\text{p}$$

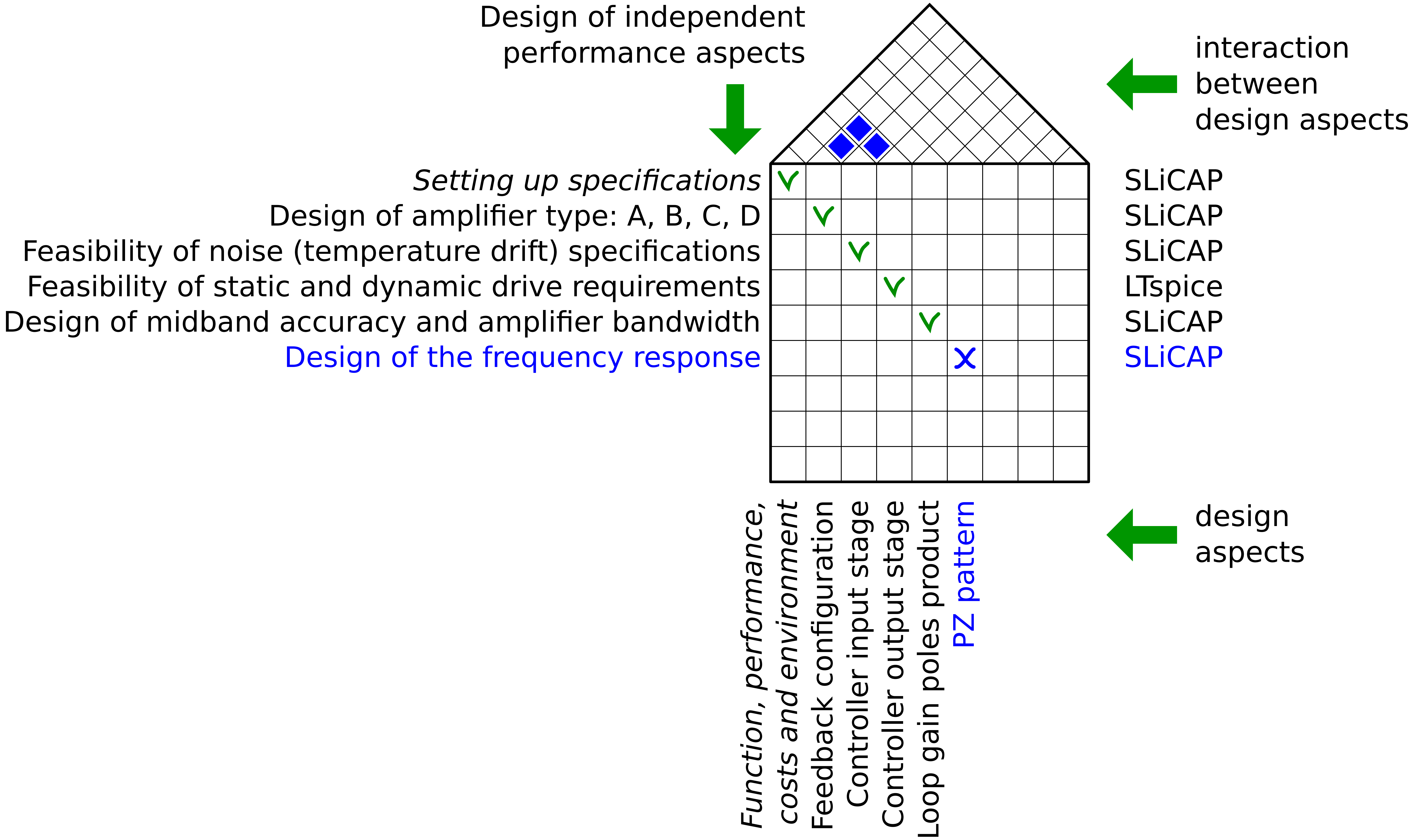
Achievable MFM bandwidth:

$$B_f = \frac{1}{2\pi}\sqrt{LP_2} = 1.5\text{GHz}$$

Structured Electronic Design

Step 6
Design of frequency response
(frequency compensation)

Anton J.M. Montagne


Design of independent
performance aspects
interaction
between
design aspects
Setting up specifications
Design of amplifier type: A, B, C, D
Feasibility of noise (temperature drift) specifications
Feasibility of static and dynamic drive requirements
Design of midband accuracy and amplifier bandwidth
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SLiCAP
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SLiCAP
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SLiCAP
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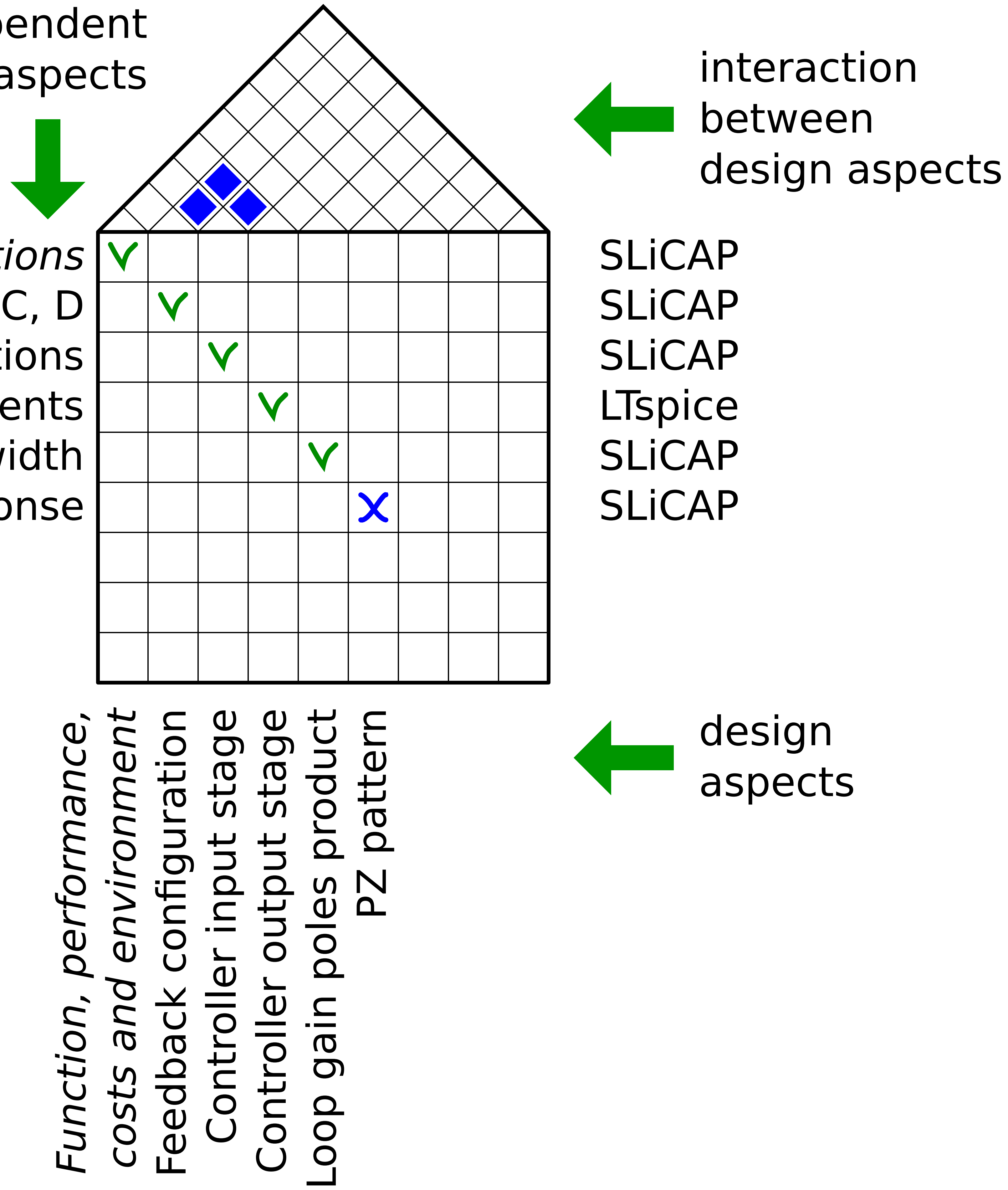
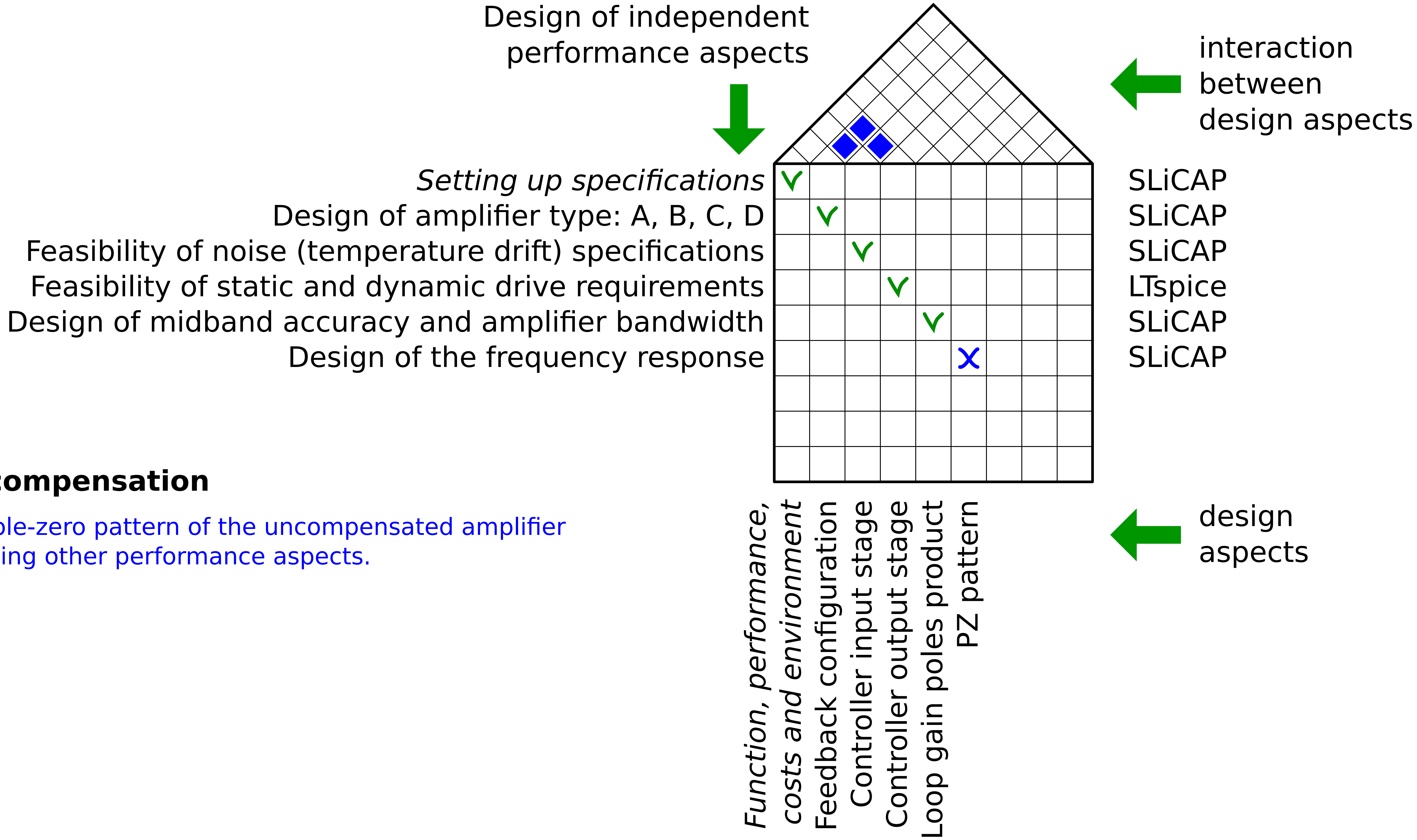
Function, performance, costs and environment
Feedback configuration
Controller input stage
Controller output stage
Loop gain poles product
PZ pattern
design
aspects

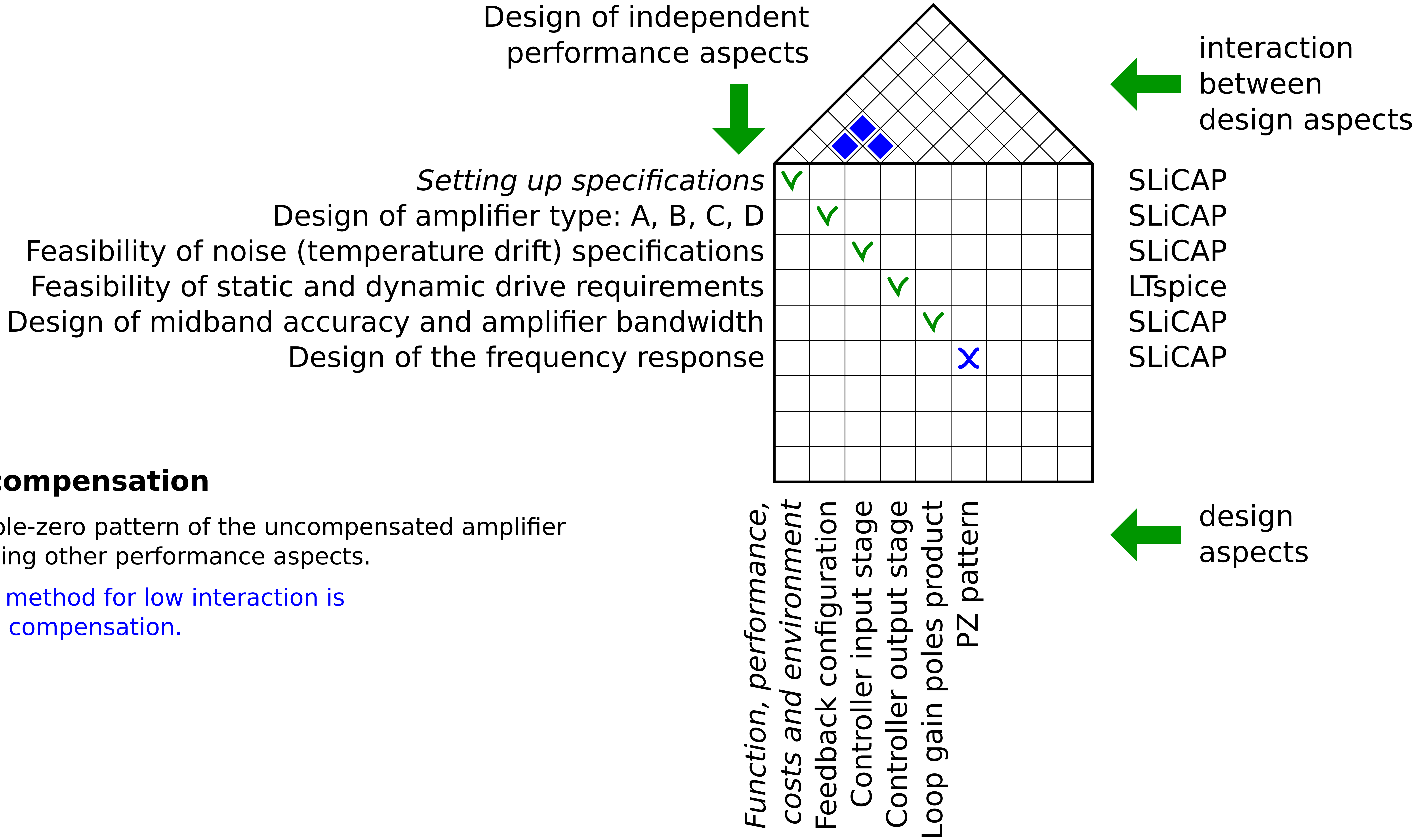
Frequency compensation





Frequency compensation

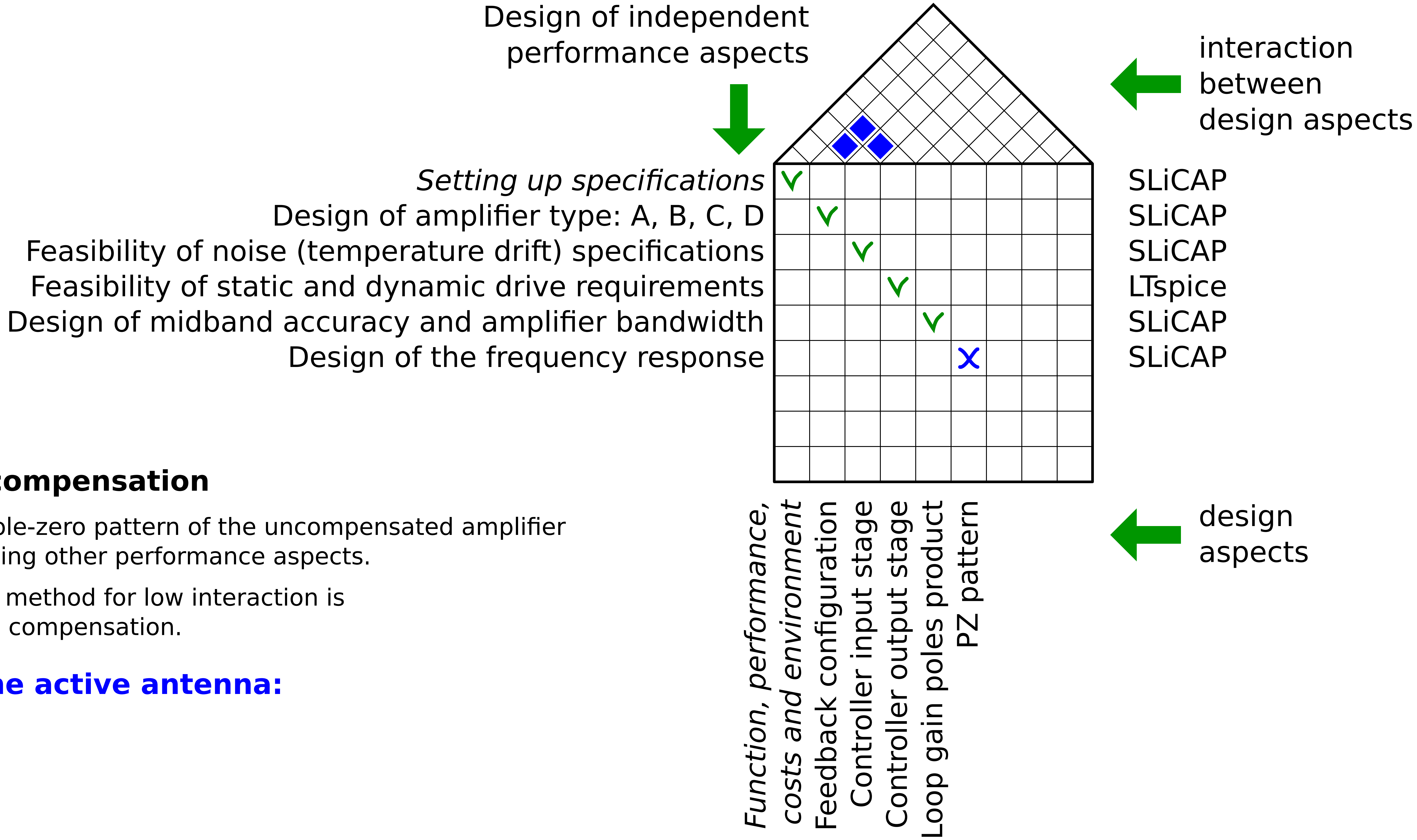
Correct the pole-zero pattern of the uncompensated amplifier without affecting other performance aspects.



Frequency compensation

Correct the pole-zero pattern of the uncompensated amplifier without affecting other performance aspects.

The preferred method for low interaction is phantom zero compensation.

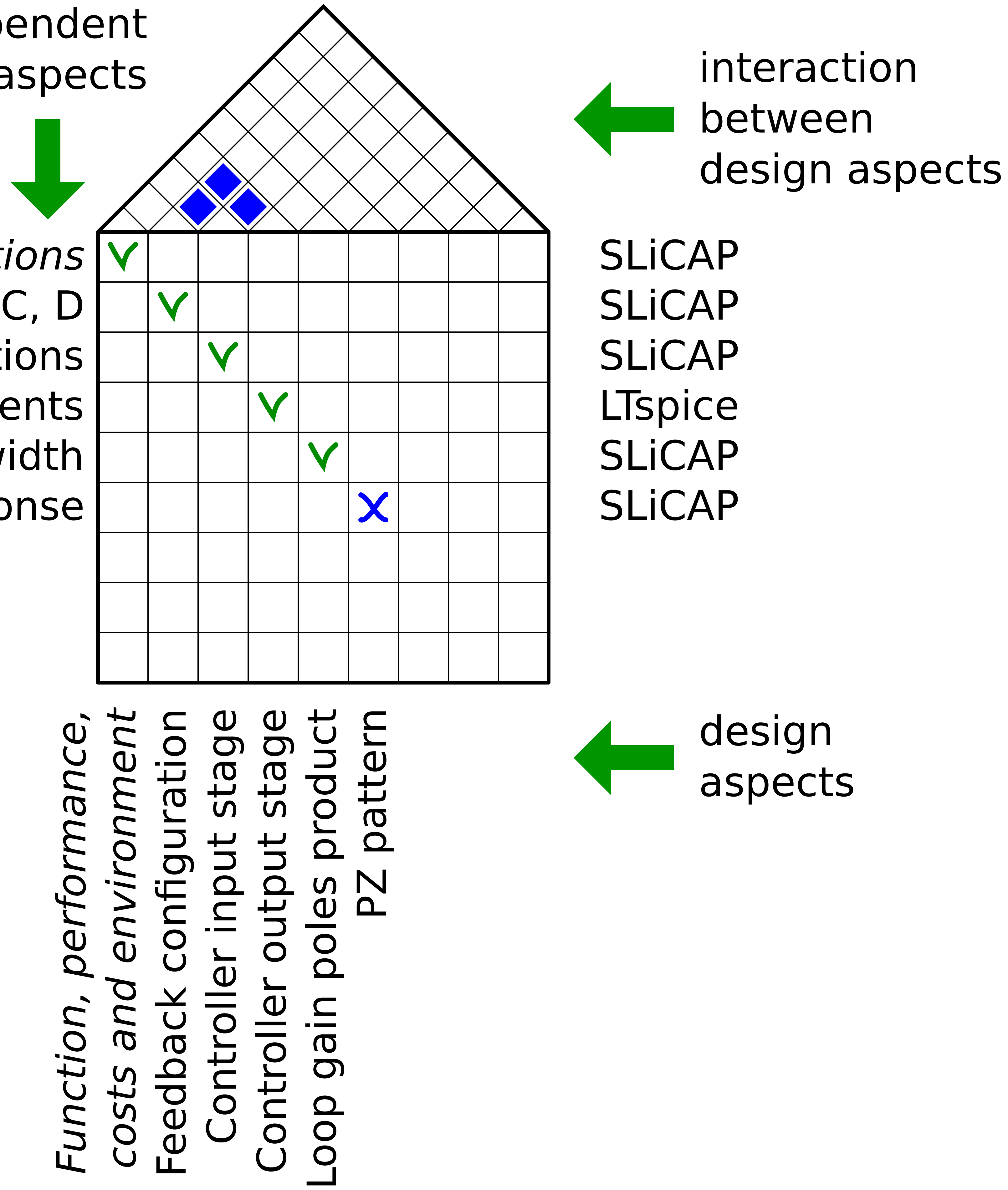


Frequency compensation

Correct the pole-zero pattern of the uncompensated amplifier without affecting other performance aspects.

The preferred method for low interaction is phantom zero compensation.

Design of the active antenna:



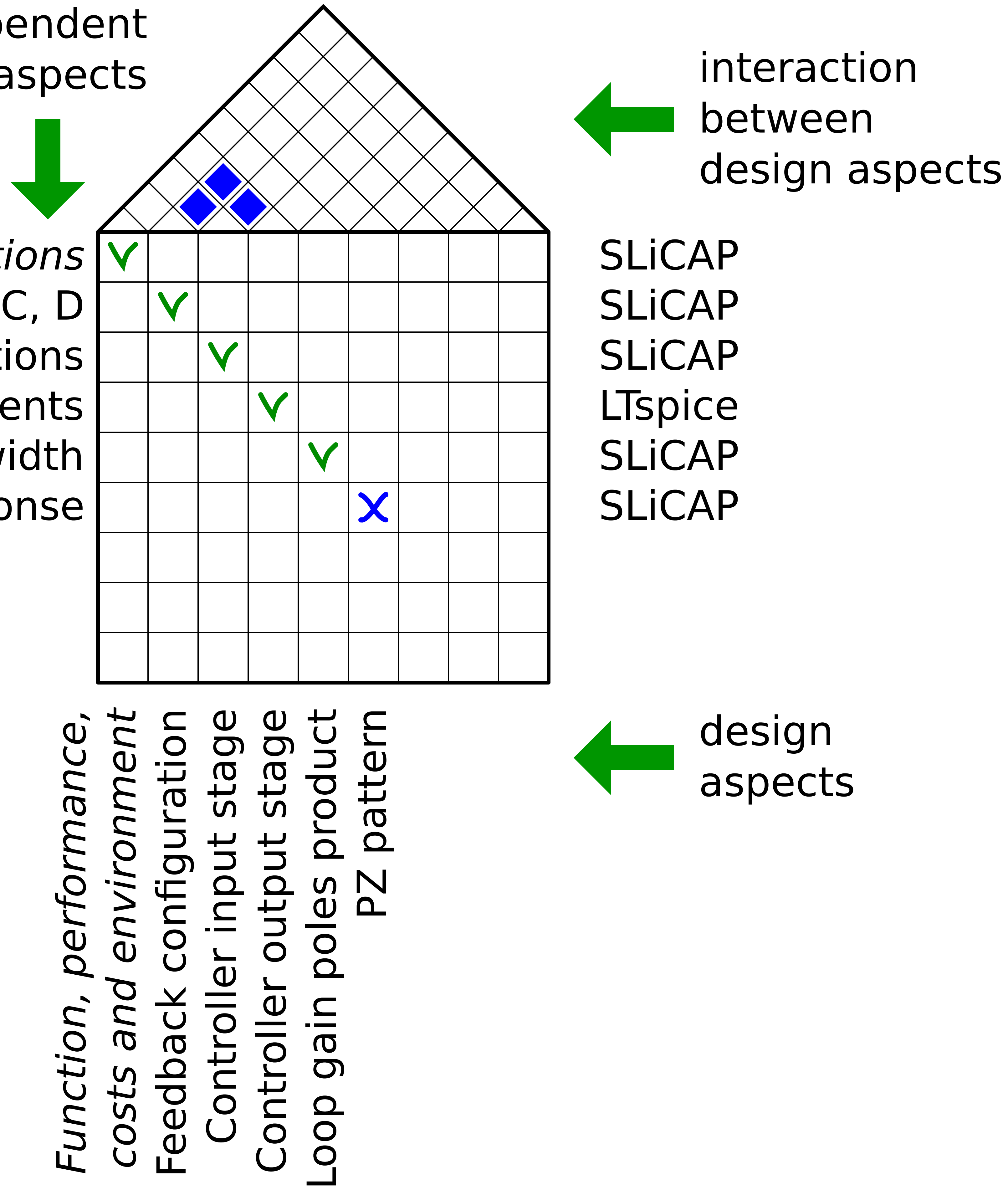
Frequency compensation

Correct the pole-zero pattern of the uncompensated amplifier without affecting other performance aspects.

The preferred method for low interaction is phantom zero compensation.

Design of the active antenna:

Correct the frequency characteristic using a phantom zero at the input of the amplifier.



Frequency compensation

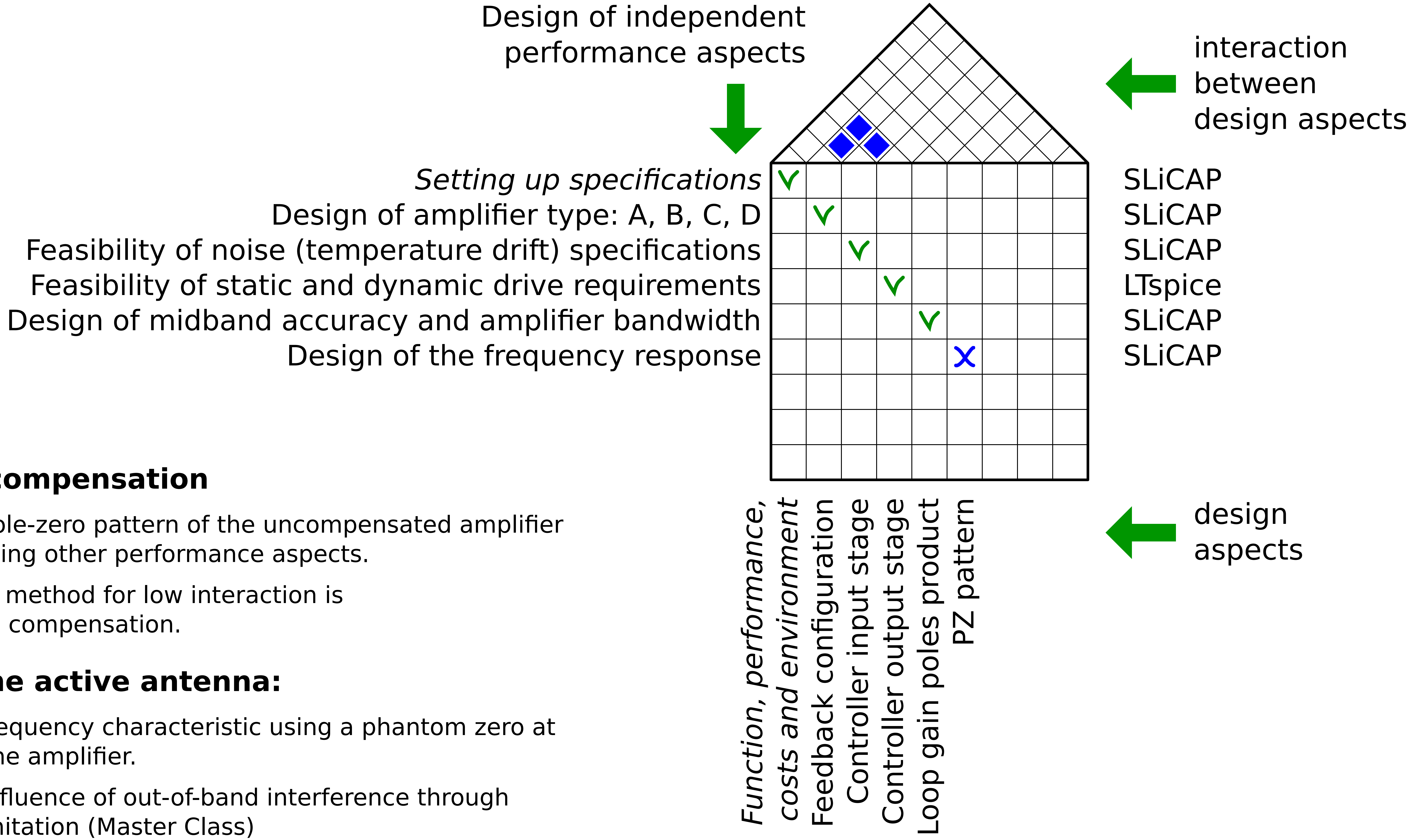
Correct the pole-zero pattern of the uncompensated amplifier without affecting other performance aspects.

The preferred method for low interaction is phantom zero compensation.

Design of the active antenna:

Correct the frequency characteristic using a phantom zero at the input of the amplifier.

Reduce the influence of out-of-band interference through bandwidth limitation (Master Class)



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Design of the active antenna:

Correct the frequency characteristic using a phantom zero at the input of the amplifier.

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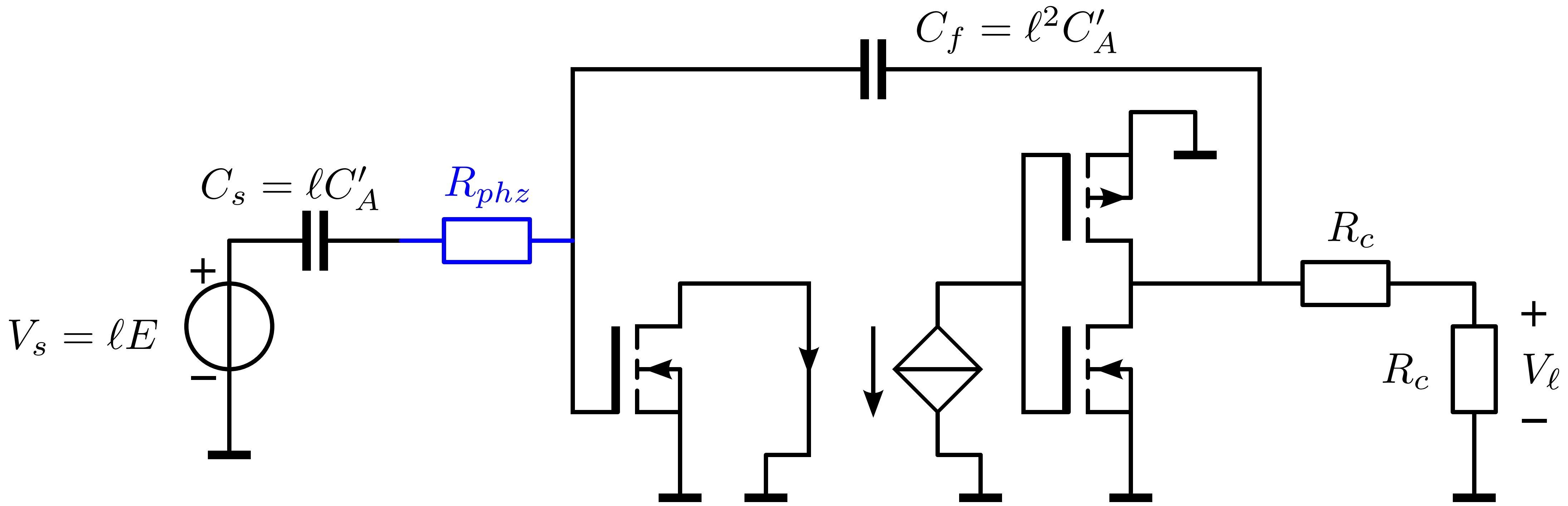
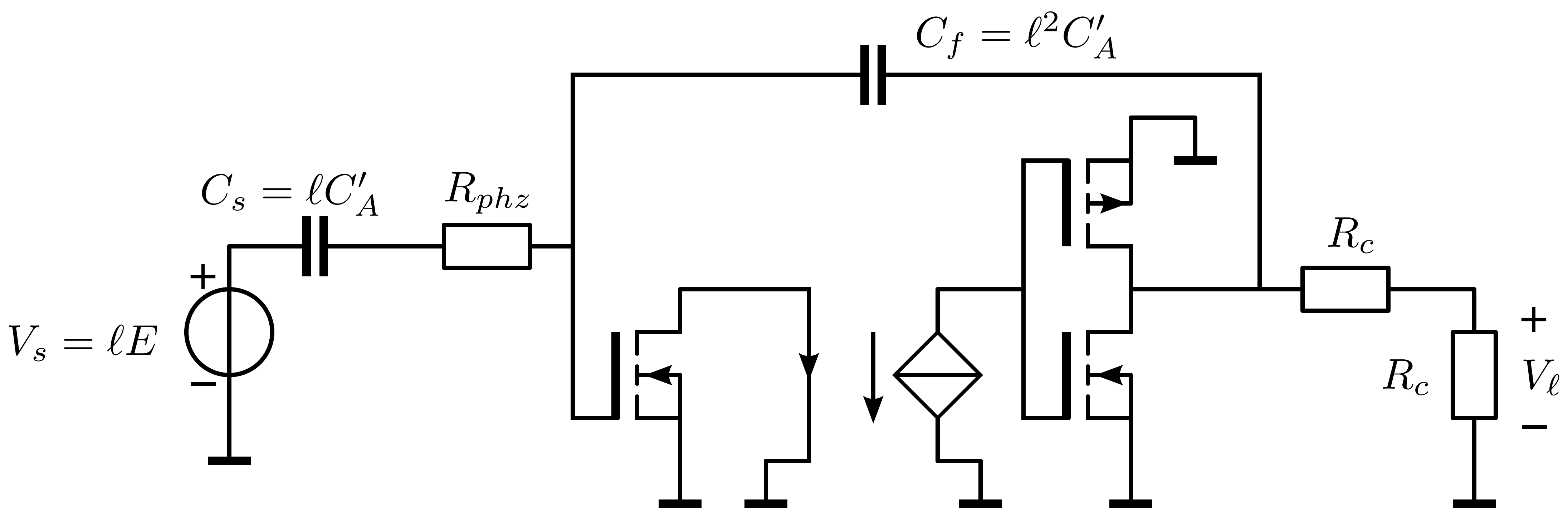
Phantom-zero compensation

Phantom-zero compensation



Phantom-zero compensation

Circuit element values:



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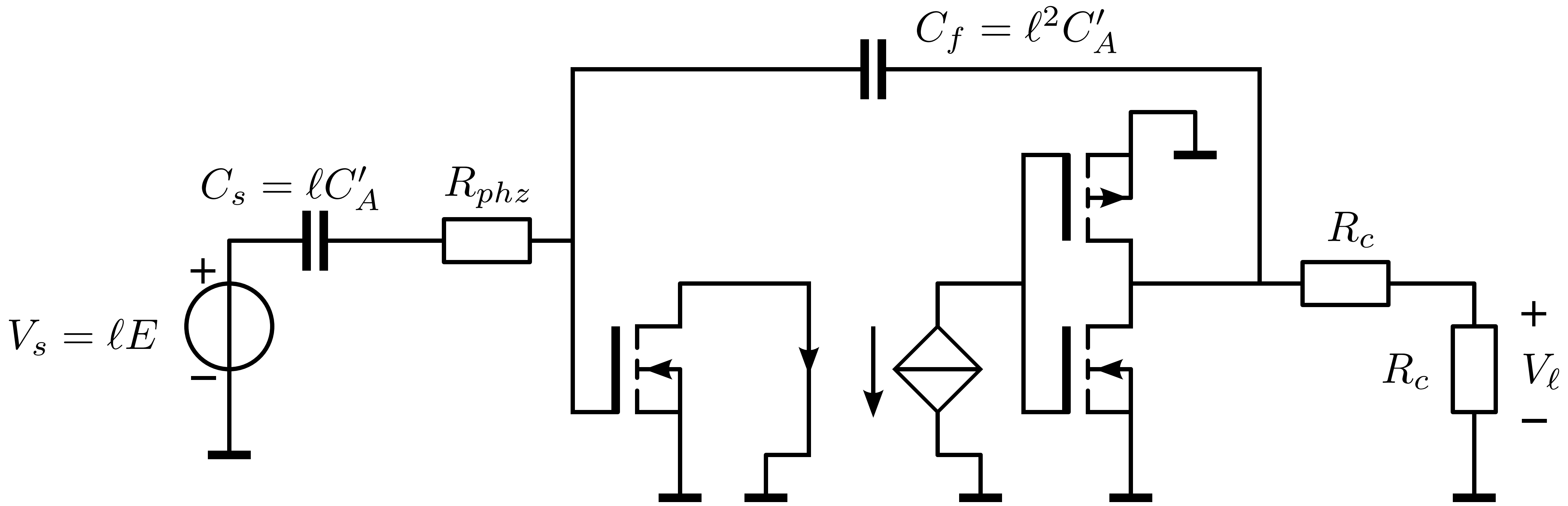

Circuit element values:

$g_{m_1} = 23\text{m}$

$g_{m_2} = 28\text{m}$

$C_s = 5\text{p}$

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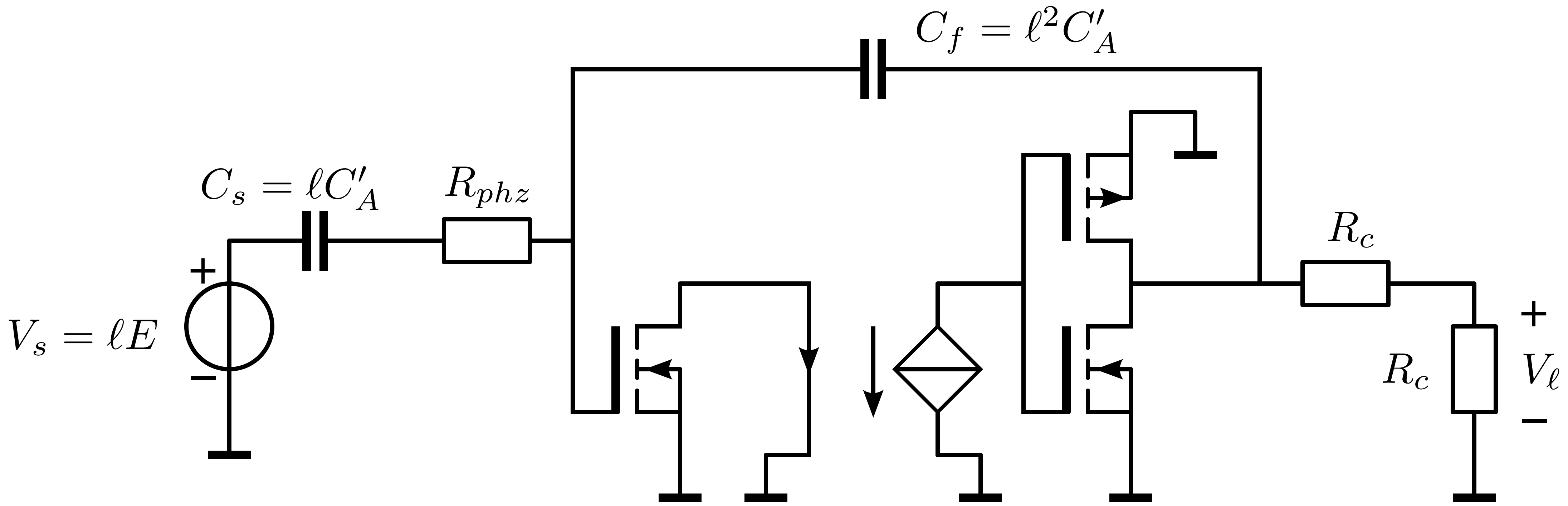
Phantom-zero compensation



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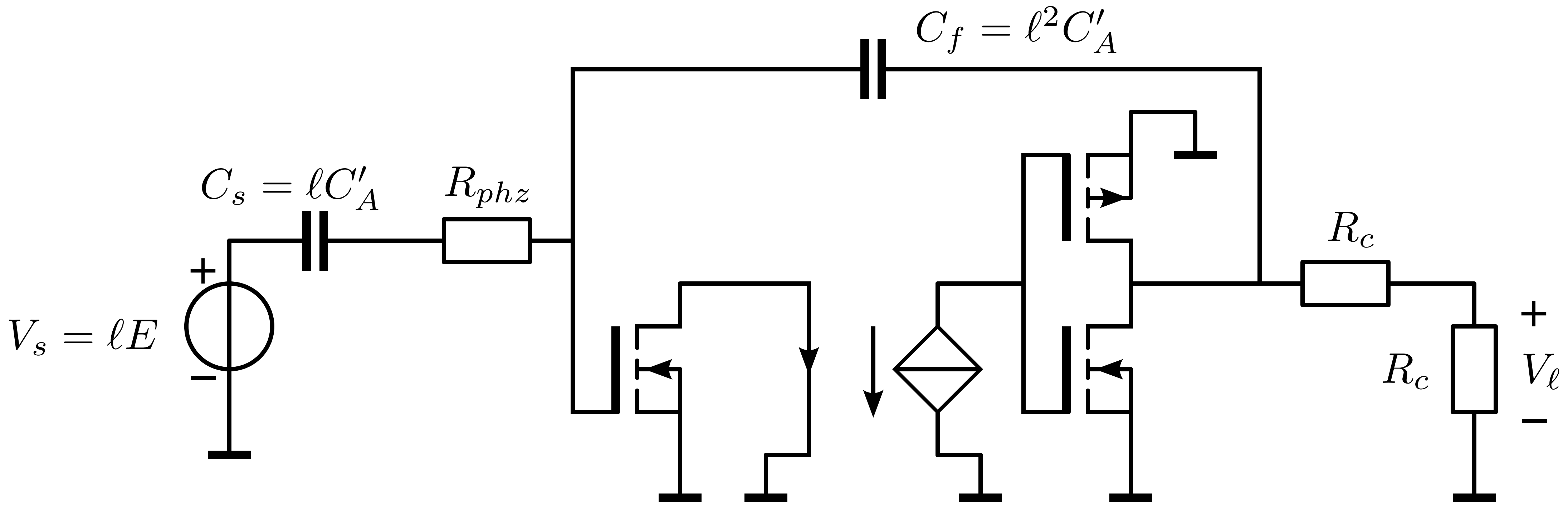
Achievable MFM bandwidth:

Phantom-zero compensation



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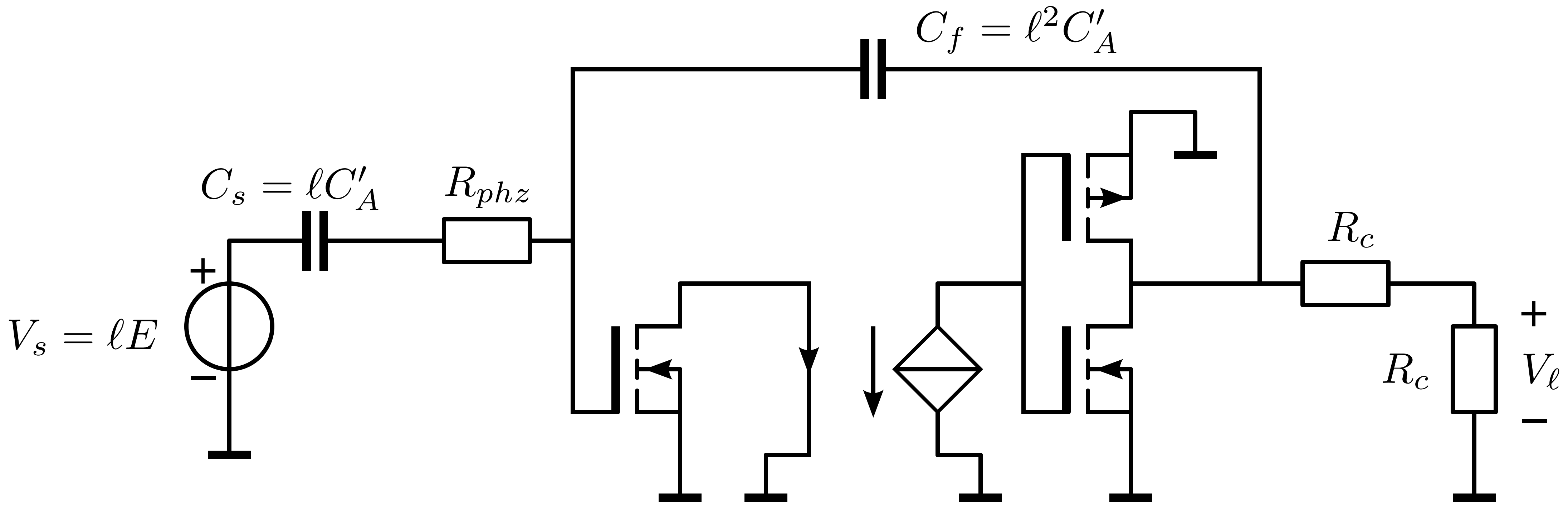
$$B_f = \frac{1}{2\pi}\sqrt{LP_2} = 1.5\text{GHz}$$

Phantom-zero compensation



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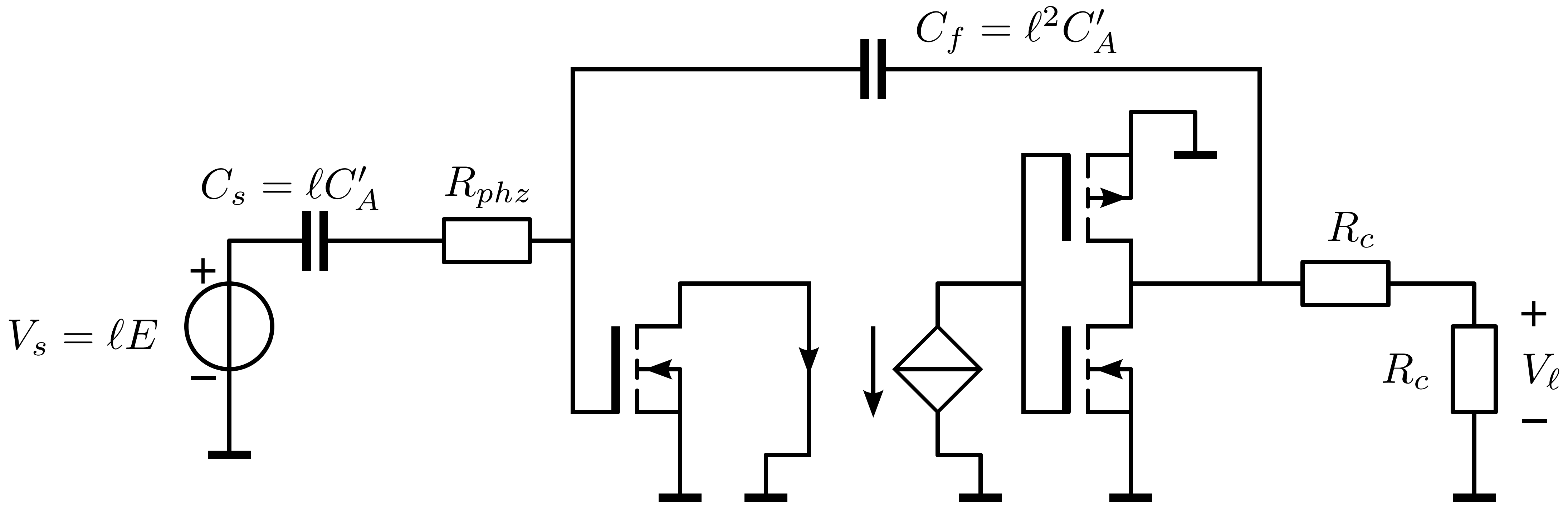
Sum of the poles:

Phantom-zero compensation



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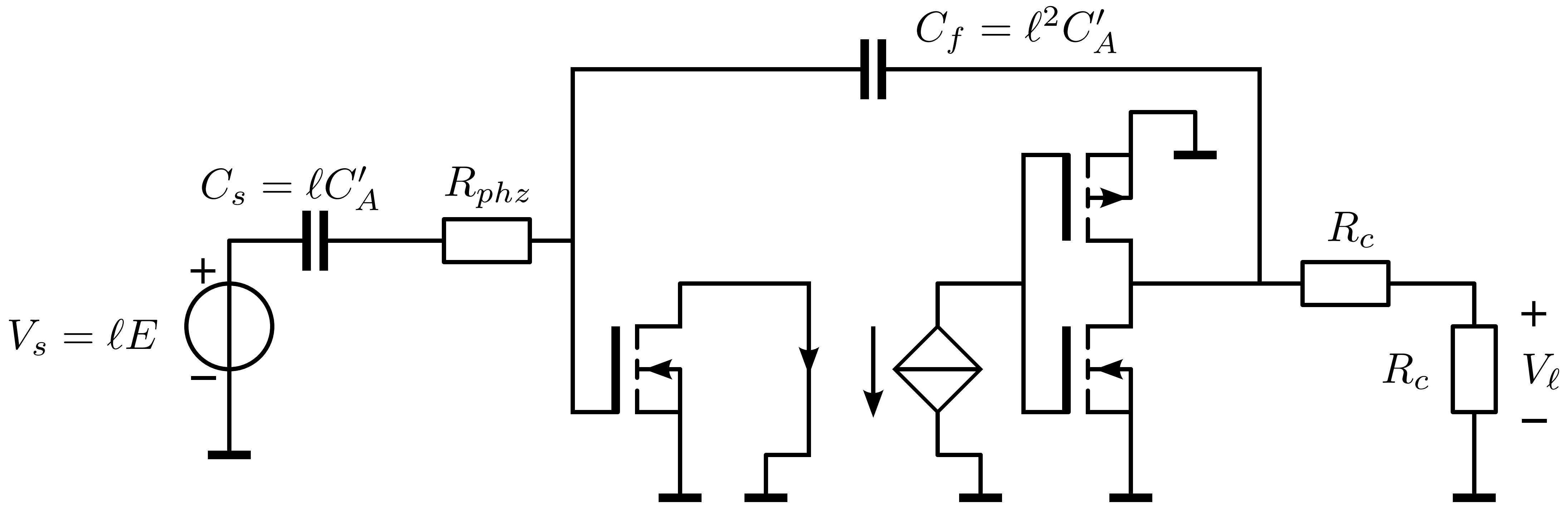
Sum of the poles:

$$p_1 = 0,\ p_2 = -\frac{C_f + C_s + c_{iss_1}}{4\pi R_c C_f \left(C_s + c_{iss_1}\right)} = -450\text{MHz}$$

Phantom-zero compensation



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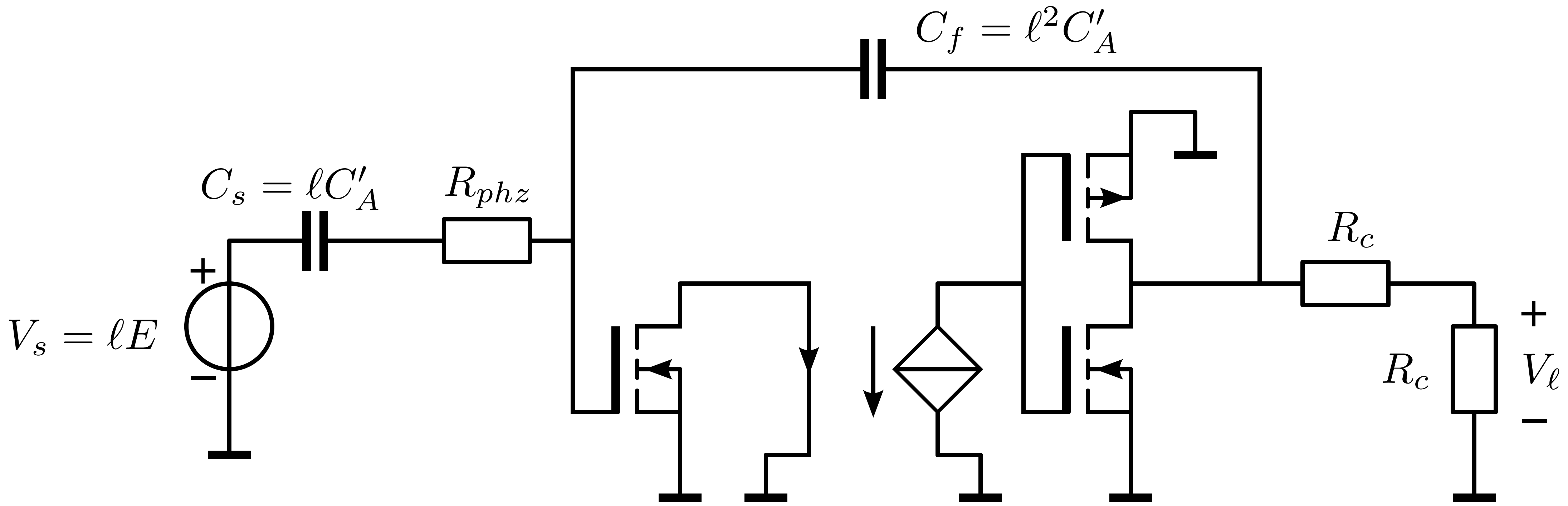
Frequency of the phantom zero

Phantom-zero compensation



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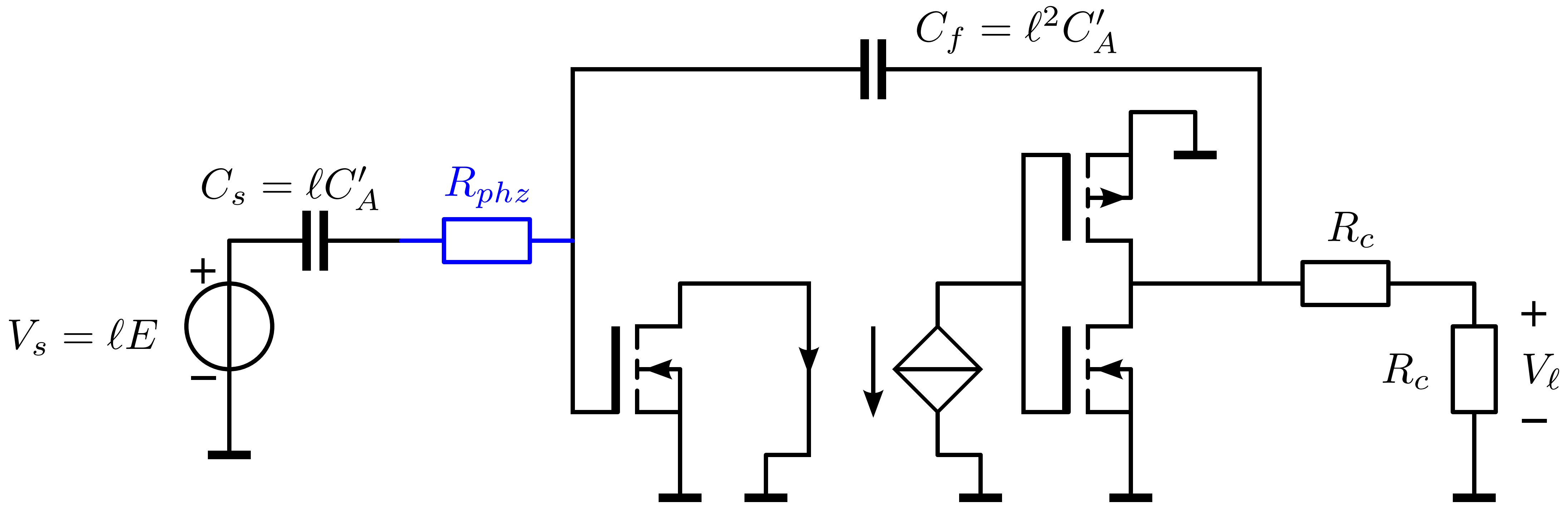
Frequency of the phantom zero

$$z = -\frac{B_f^2}{\sqrt{2}B_f + p_1 + p_2} = -\frac{1}{2\pi R_{phz} C_s} = -1\text{GHz}$$

Phantom-zero compensation



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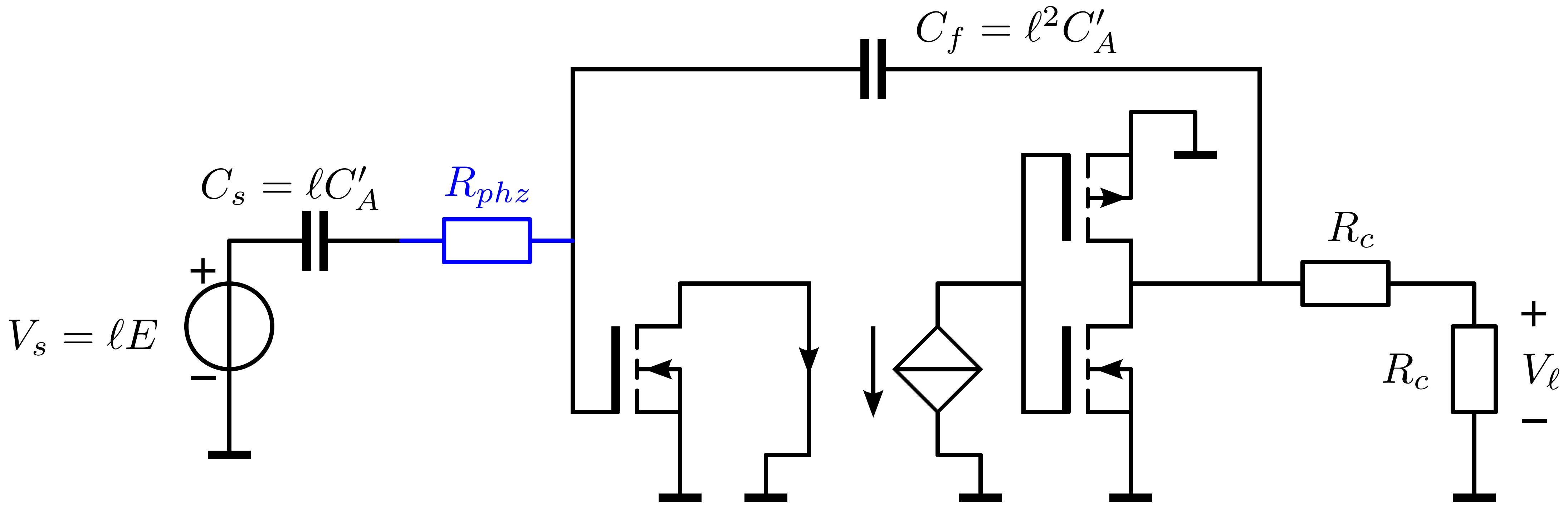
Value of the compensation resistor

Phantom-zero compensation



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Value of the compensation resistor

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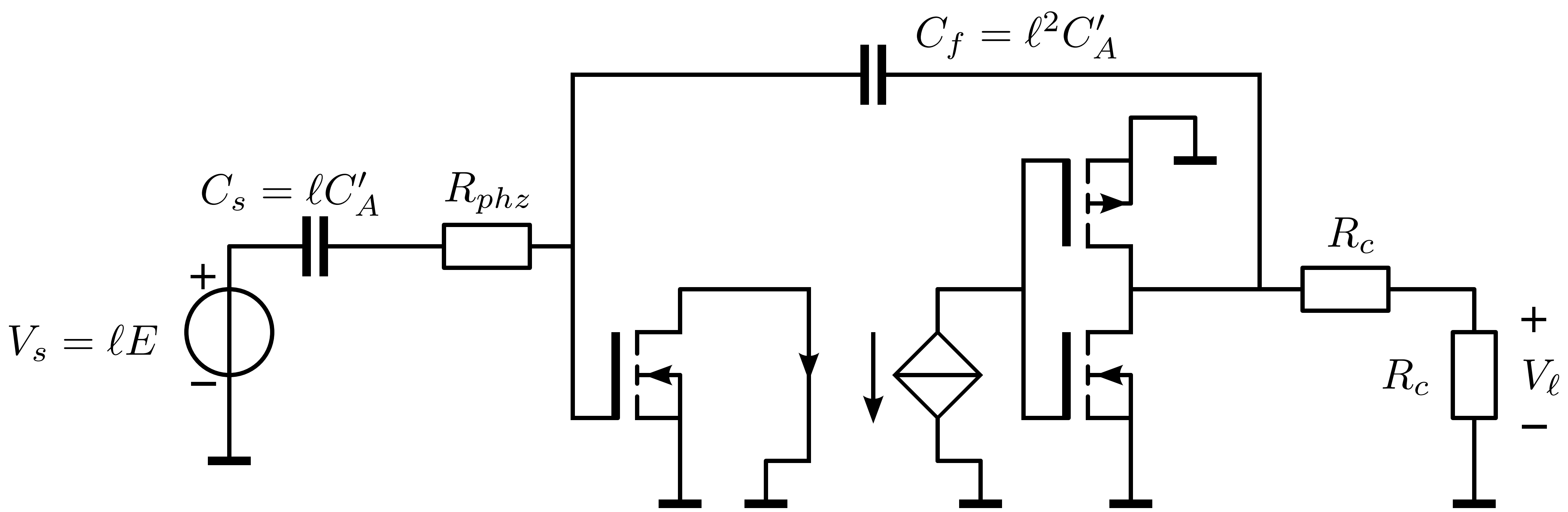
Phantom-zero compensation



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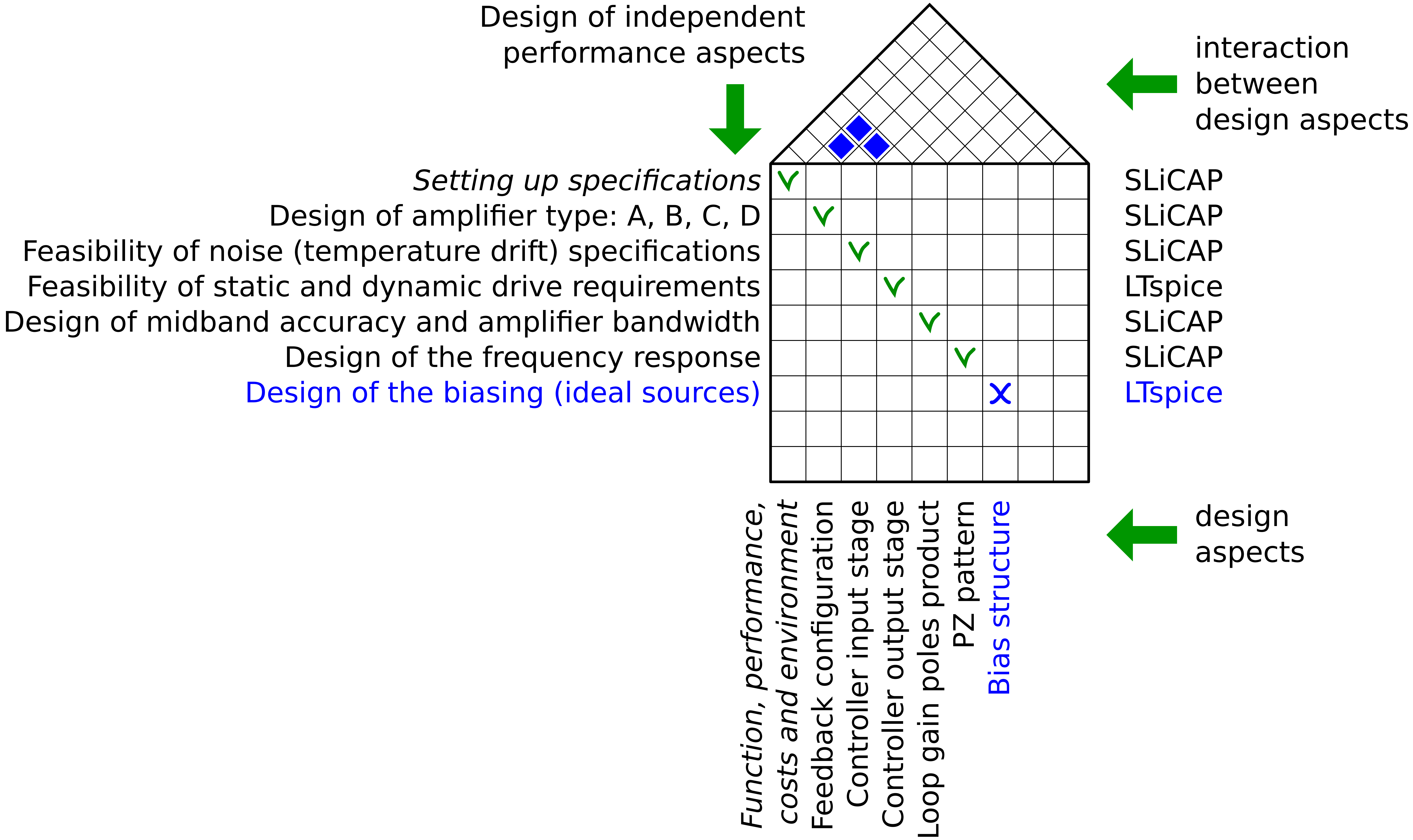
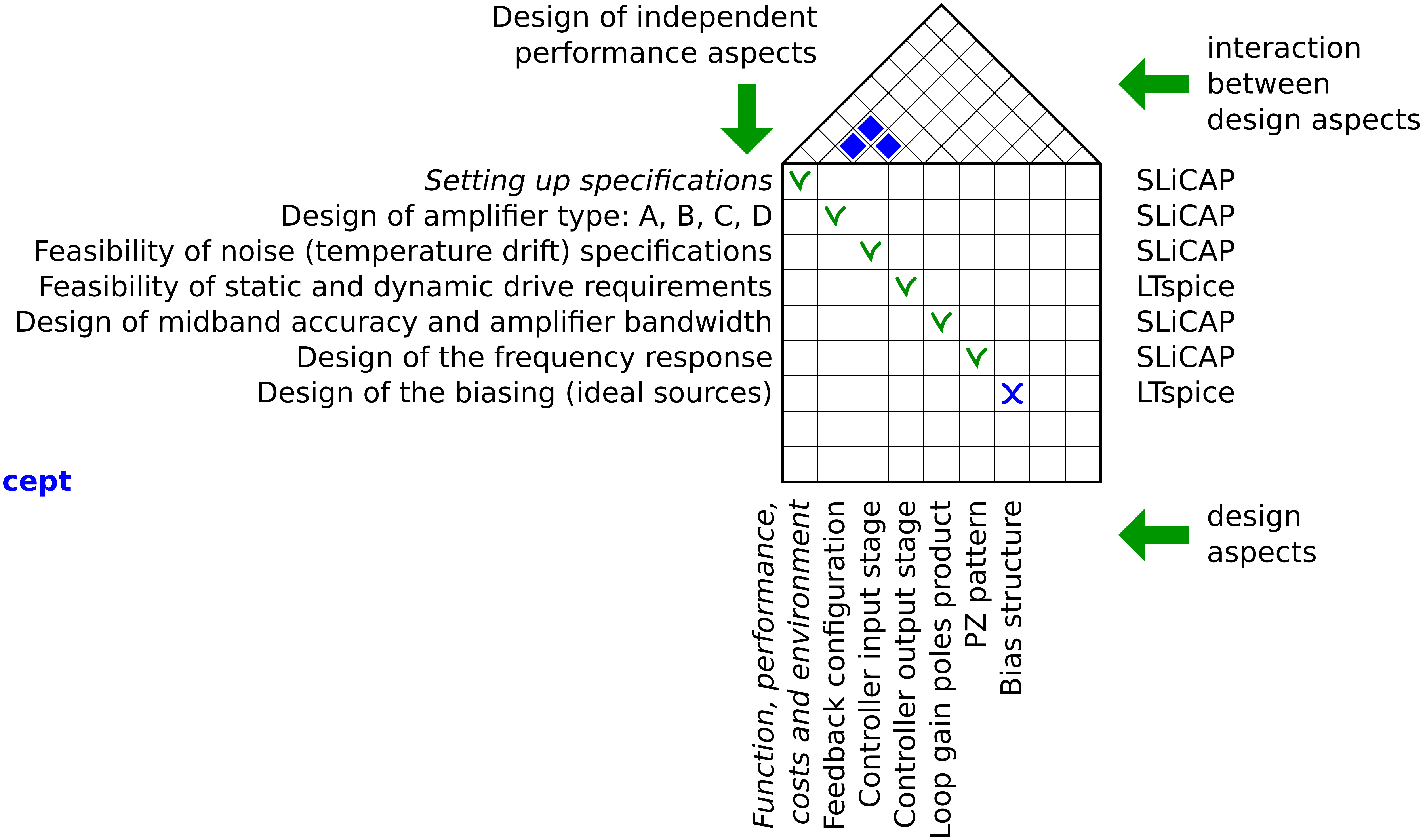
Structured Electronic Design

Step 7
Design of the biasing concept
(ideal bias sources)

Anton J.M. Montagne



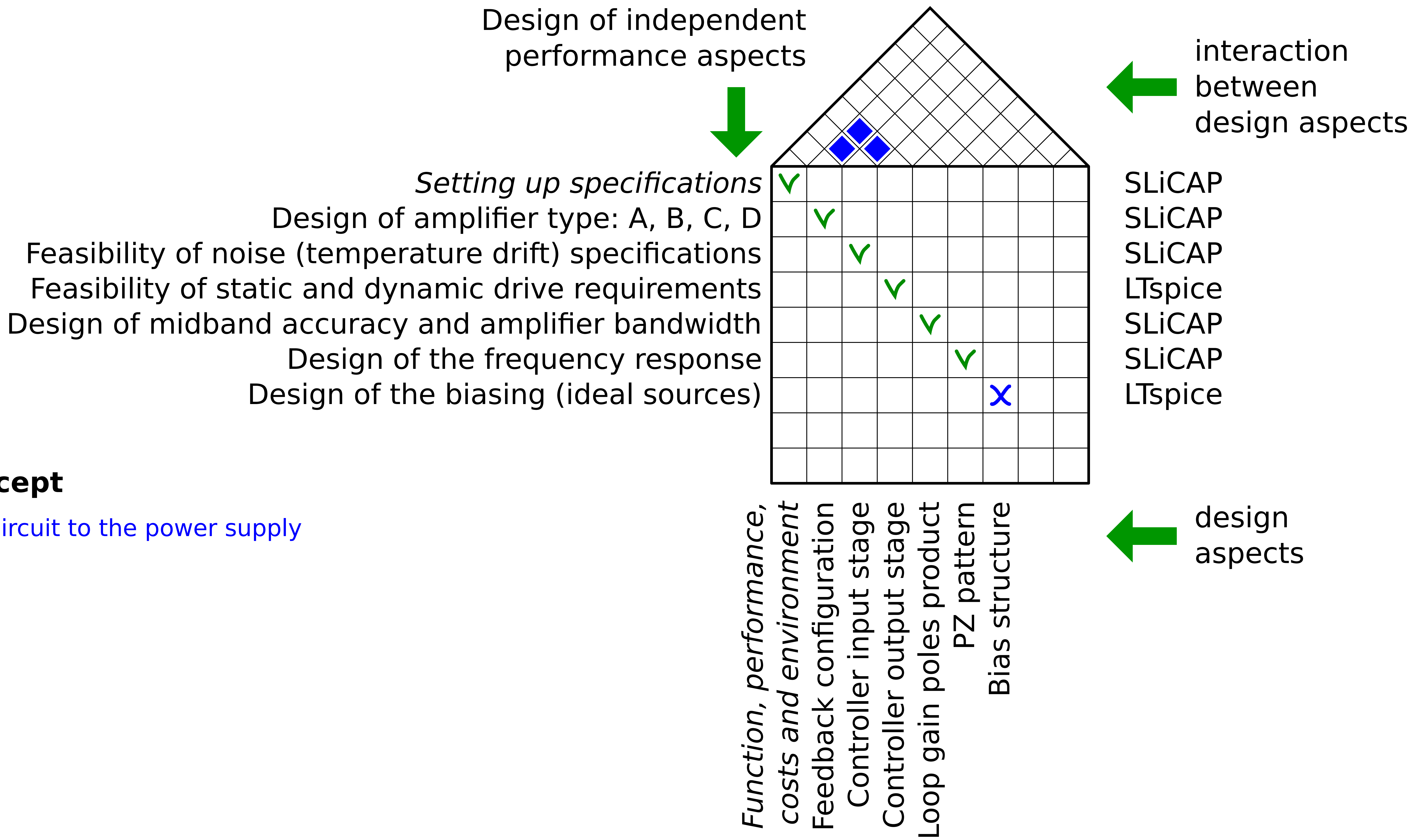
Design of independent performance aspects
interaction between design aspects
Setting up specifications
Design of amplifier type: A, B, C, D
Feasibility of noise (temperature drift) specifications
Feasibility of static and dynamic drive requirements
Design of midband accuracy and amplifier bandwidth
Design of the frequency response
Design of the biasing (ideal sources)
SLiCAP
SLiCAP
SLiCAP
LTspice
SLiCAP
SLiCAP
LTspice
Function, performance, costs and environment
Feedback configuration
Controller input stage
Controller output stage
Loop gain poles product
PZ pattern
Bias structure
design aspects

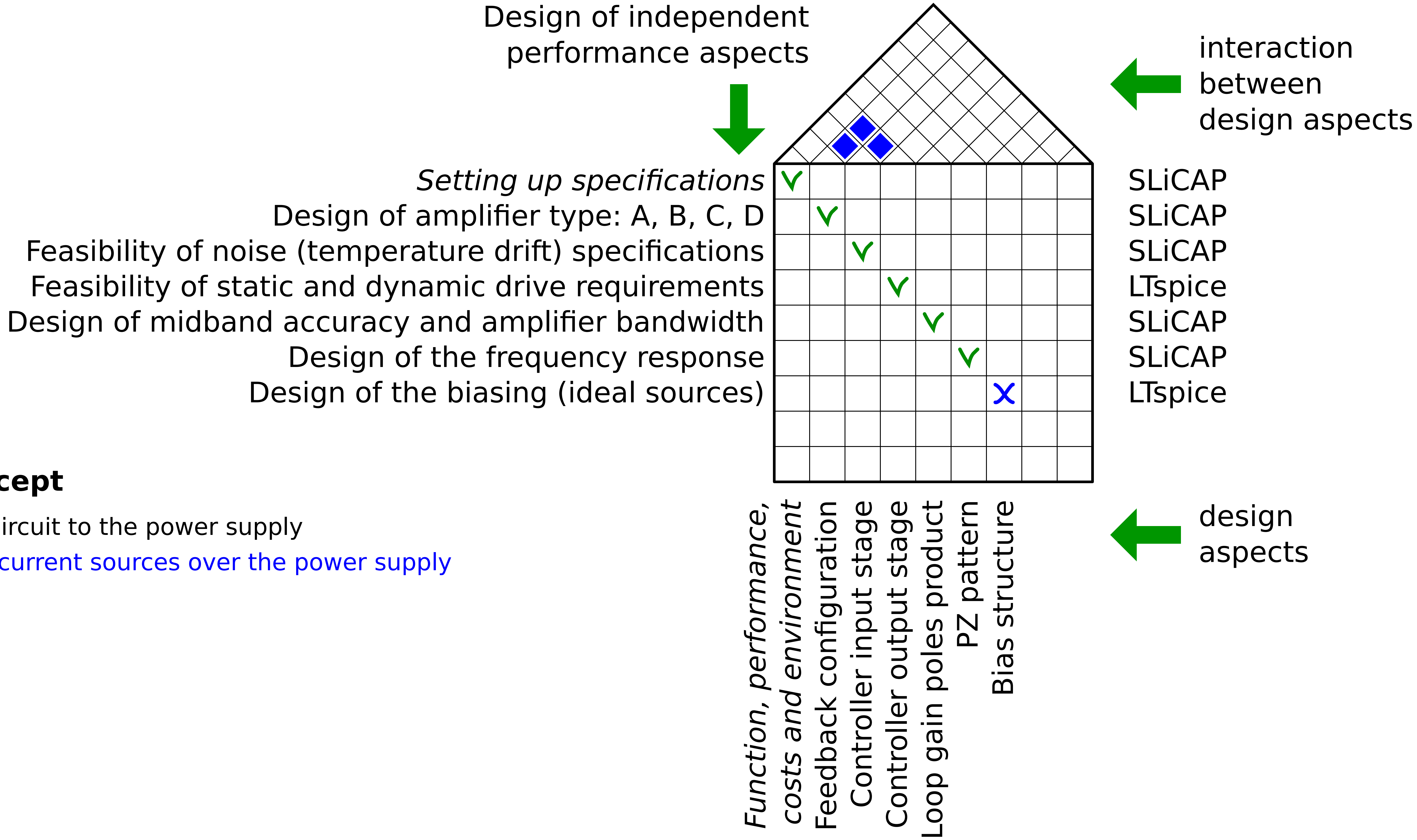


Biasing concept

Biasing concept

Connect the circuit to the power supply





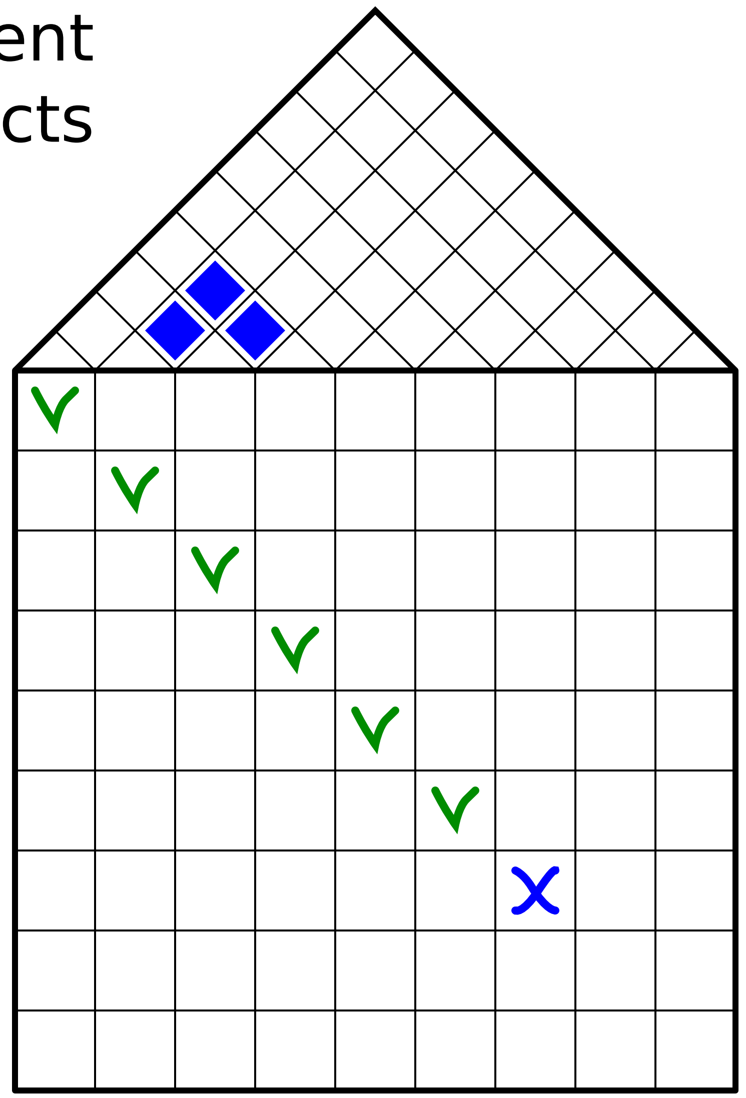
Biasing concept

Connect the circuit to the power supply

Redirect bias current sources over the power supply

Design of independent performance aspects

interaction between design aspects



Design aspect step	Tool
Setting up specifications	SLiCAP
Design of amplifier type: A, B, C, D	SLiCAP
Feasibility of noise (temperature drift) specifications	SLiCAP
Feasibility of static and dynamic drive requirements	LTspice
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Function, performance, costs and environment
Feedback configuration
Controller input stage
Controller output stage
Loop gain poles product
PZ pattern
Bias structure

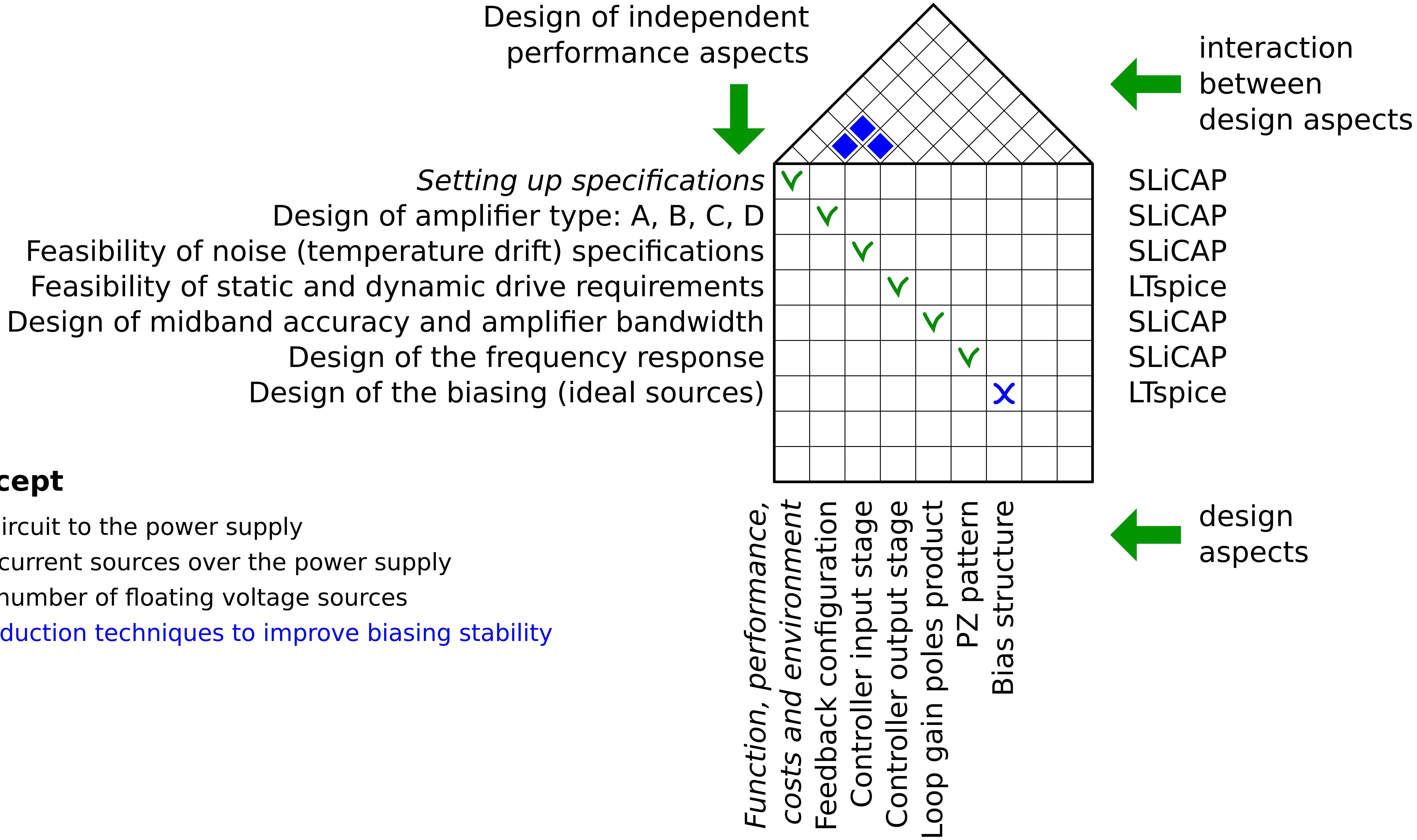
design aspects

Biasing concept

Connect the circuit to the power supply

Redirect bias current sources over the power supply

Minimize the number of floating voltage sources



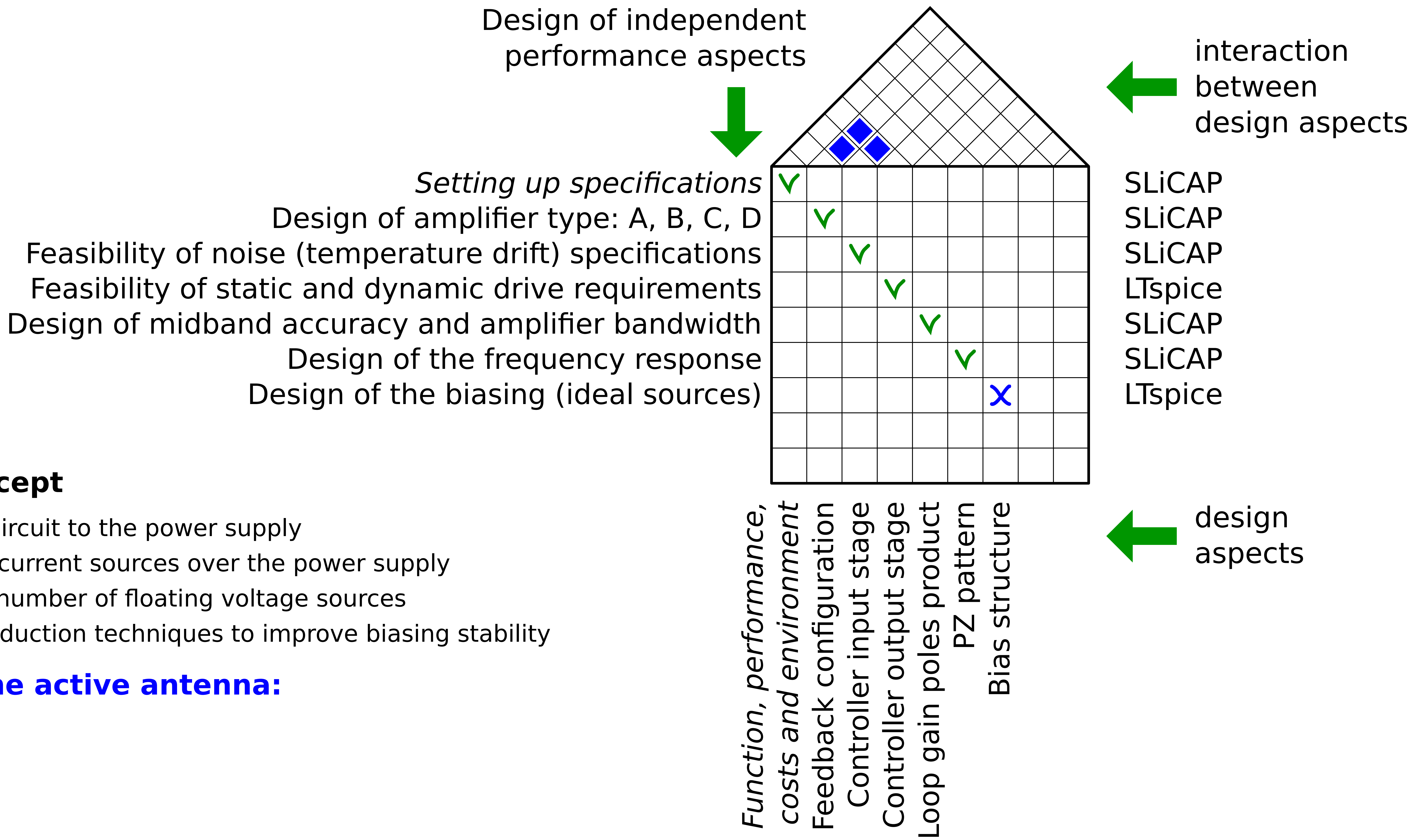
Biasing concept

Connect the circuit to the power supply

Redirect bias current sources over the power supply

Minimize the number of floating voltage sources

Apply error reduction techniques to improve biasing stability



Biasing concept

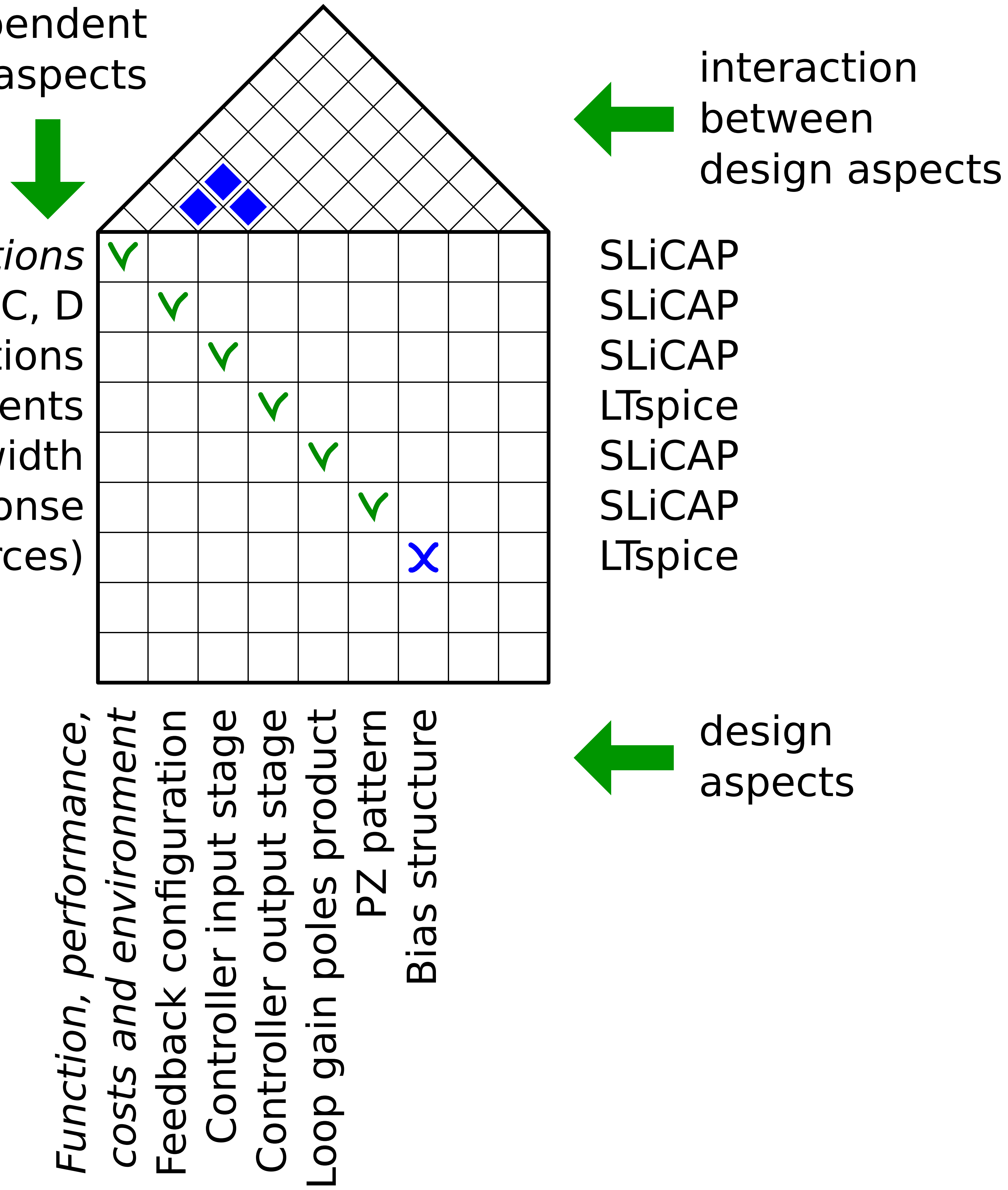
Connect the circuit to the power supply

Redirect bias current sources over the power supply

Minimize the number of floating voltage sources

Apply error reduction techniques to improve biasing stability

Design of the active antenna:



Biasing concept

Connect the circuit to the power supply

Redirect bias current sources over the power supply

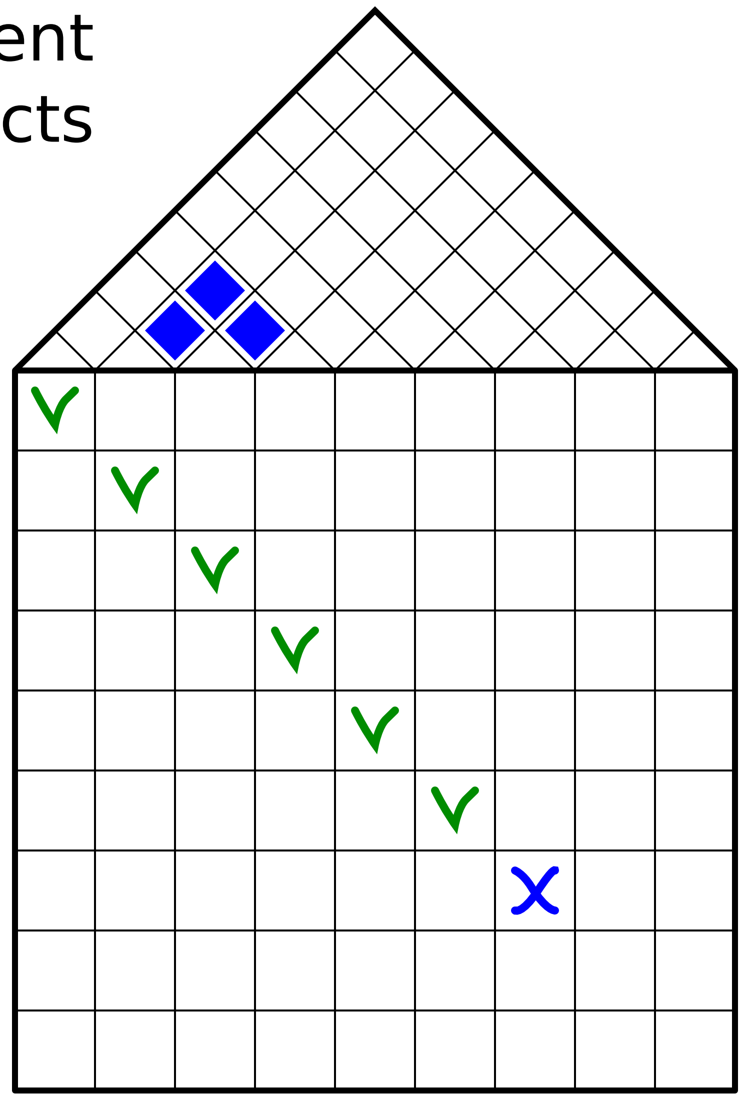
Minimize the number of floating voltage sources

Apply error reduction techniques to improve biasing stability

Design of the active antenna:

1.8V supply

Design of independent performance aspects

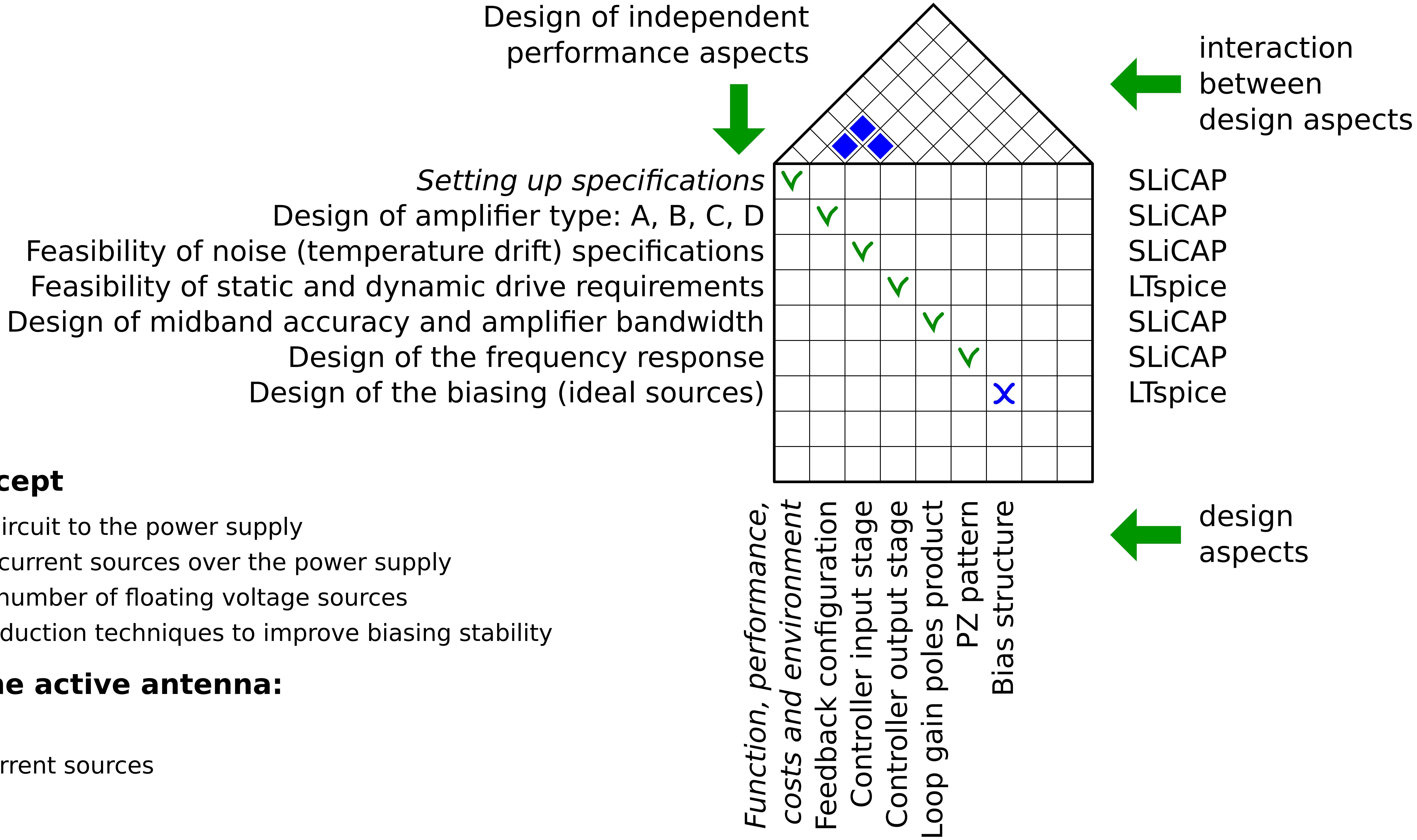


Biasing concept

- Connect the circuit to the power supply
- Redirect bias current sources over the power supply
- Minimize the number of floating voltage sources
- Apply error reduction techniques to improve biasing stability

Design of the active antenna:

- 1.8V supply
- Redirected current sources



Biasing concept

- Connect the circuit to the power supply
- Redirect bias current sources over the power supply
- Minimize the number of floating voltage sources
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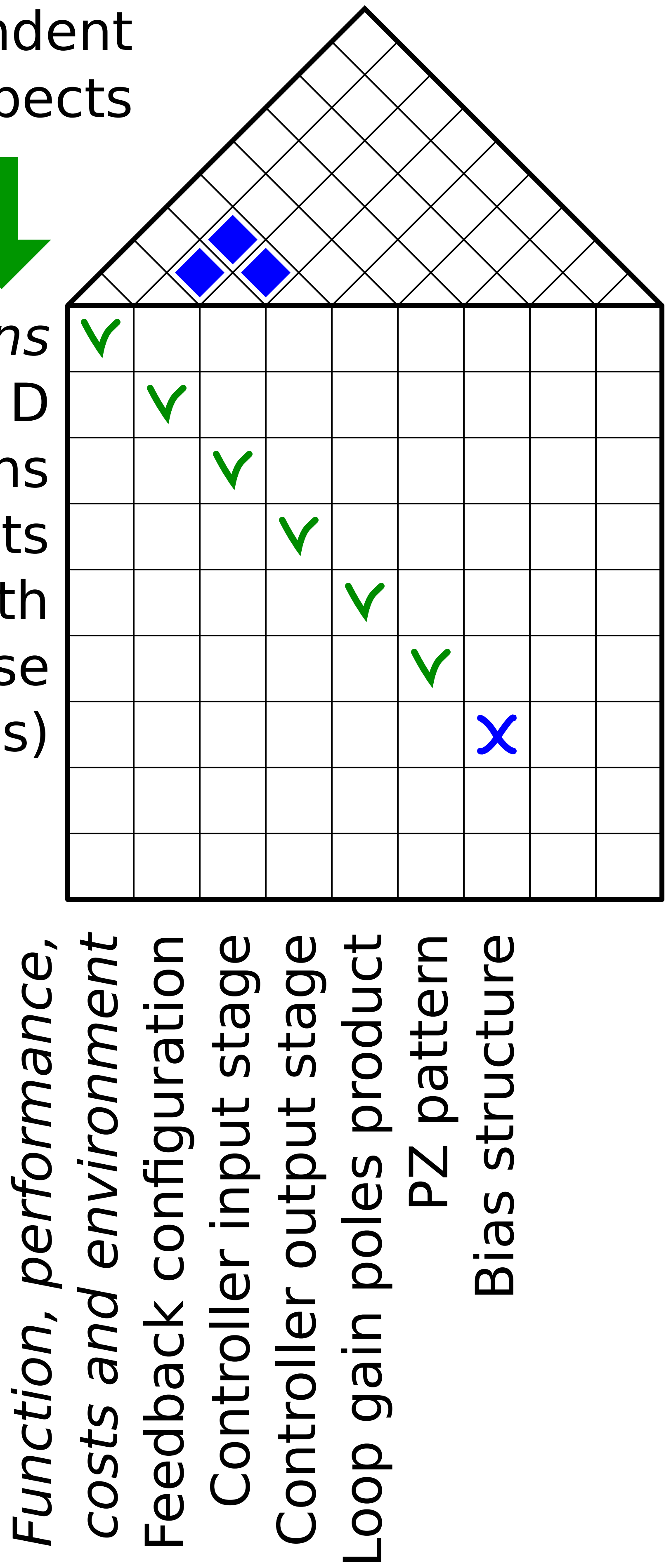
Design of the active antenna:

- 1.8V supply
- Redirected current sources
- AC coupling

Design of independent performance aspects

interaction between design aspects



Setting up specifications	SLiCAP
Design of amplifier type: A, B, C, D	SLiCAP
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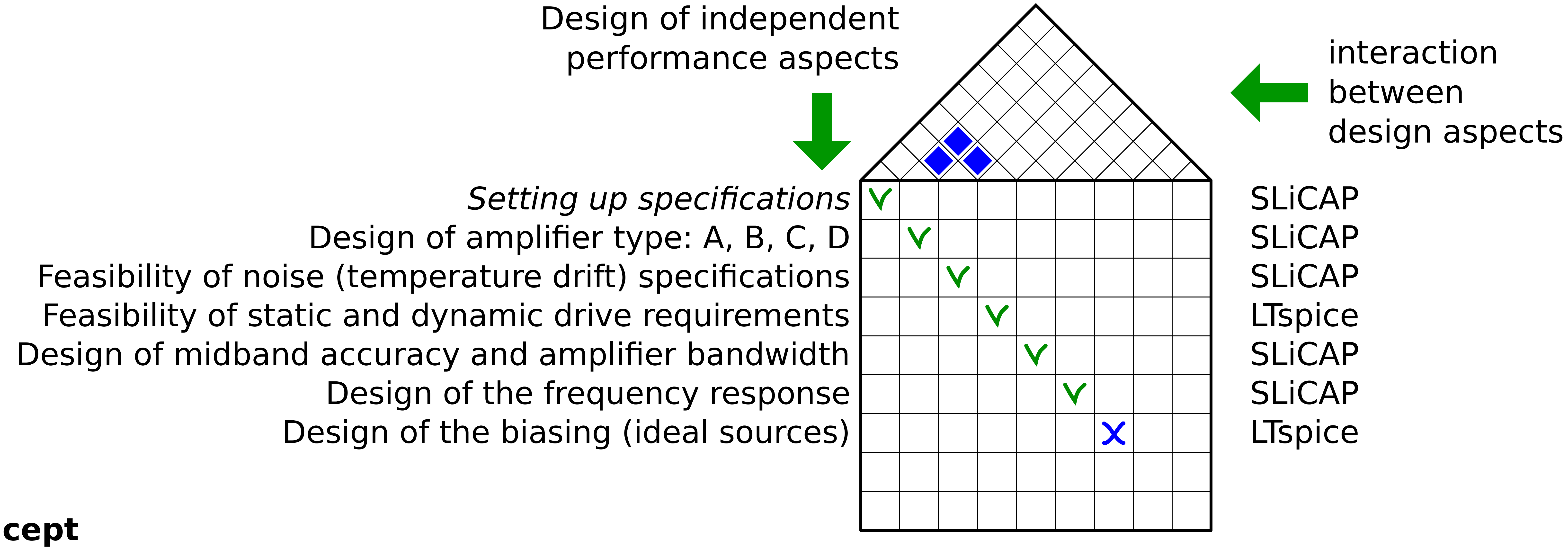
design aspects

Biasing concept

- Connect the circuit to the power supply
- Redirect bias current sources over the power supply
- Minimize the number of floating voltage sources
- Apply error reduction techniques to improve biasing stability

Design of the active antenna:

- 1.8V supply
- Redirected current sources
- AC coupling
- Over-all negative-feedback biasing



Biasing concept

Connect the circuit to the power supply

Redirect bias current sources over the power supply

Minimize the number of floating voltage sources

Apply error reduction techniques to improve biasing stability

Design of the active antenna:

1.8V supply

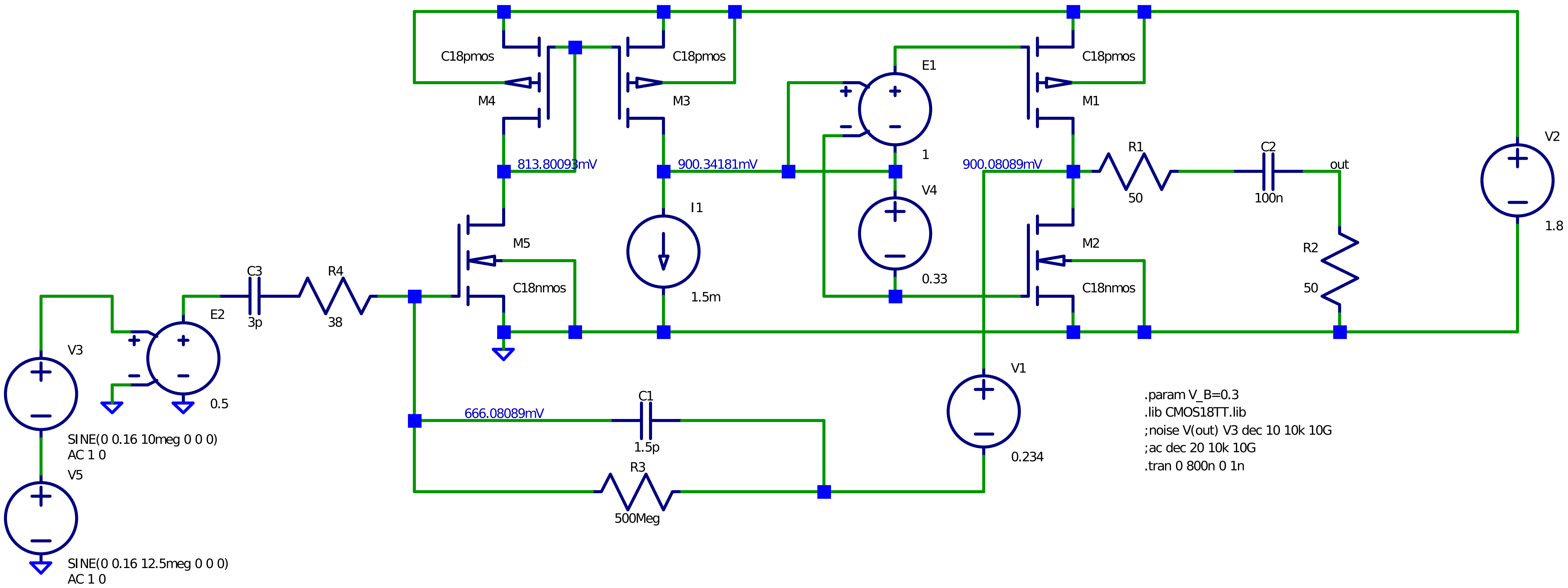
Redirected current sources

AC coupling

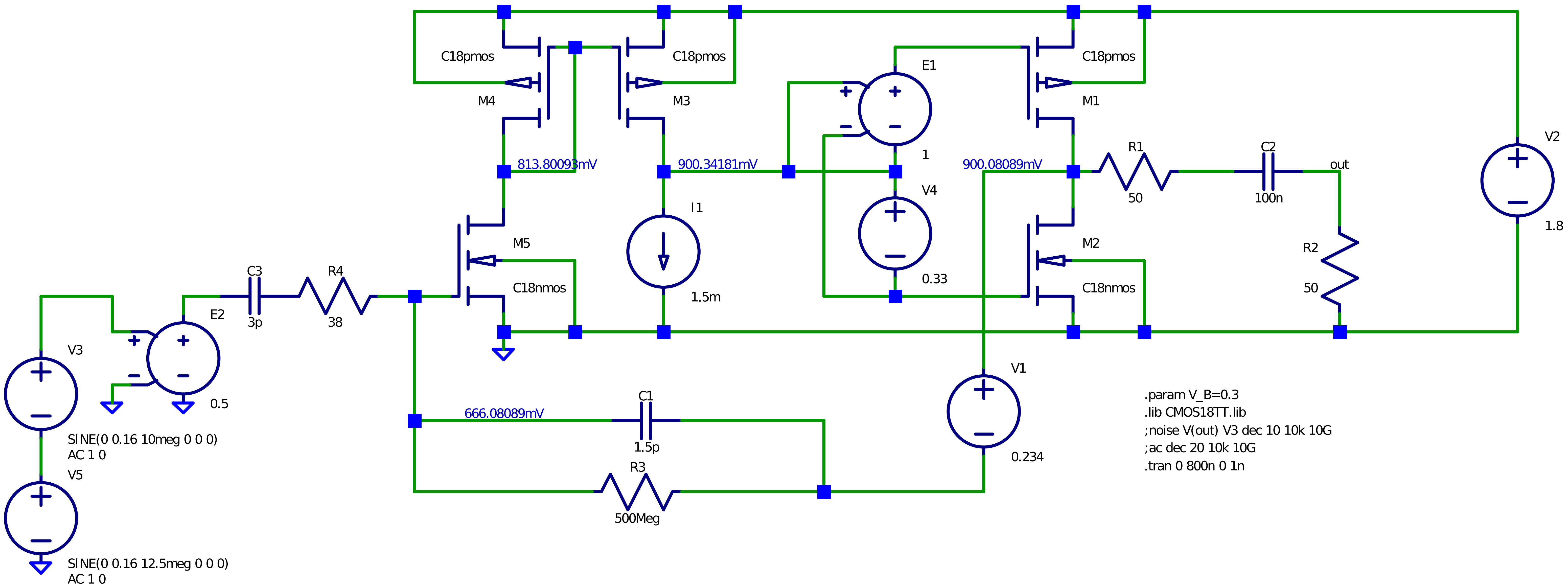
Over-all negative-feedback biasing

Biasing concept

Biasing concept

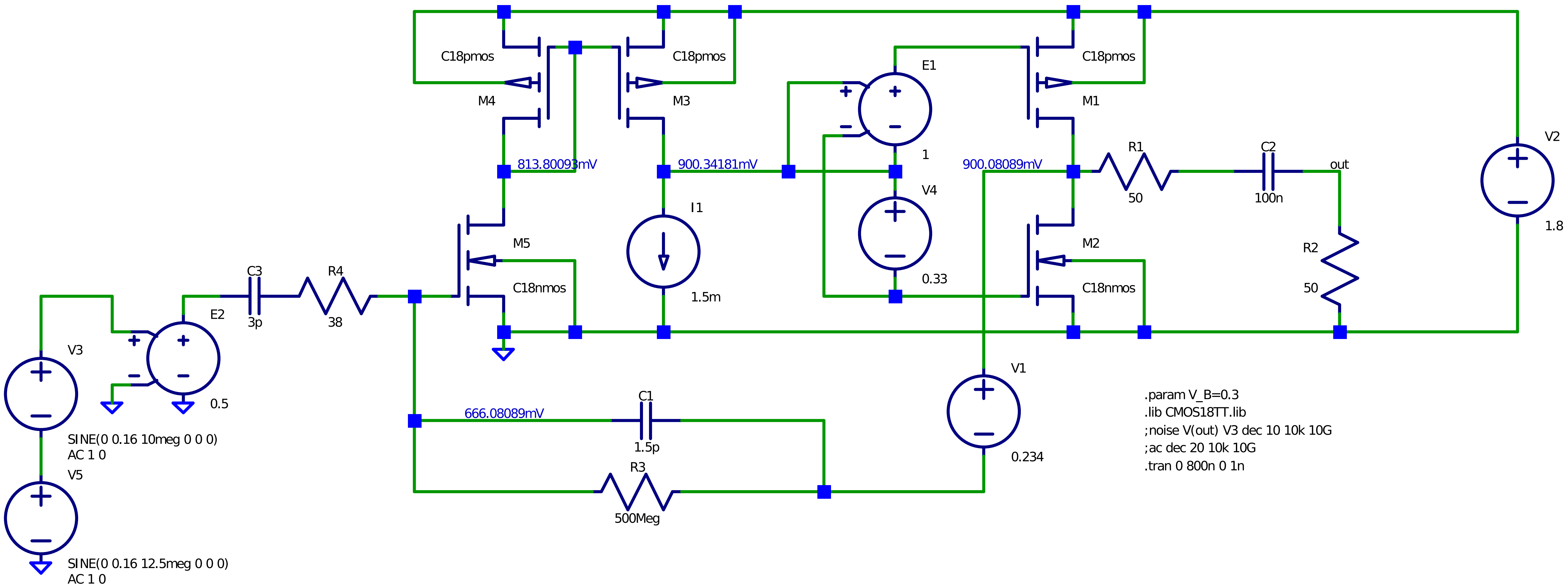


Biasing concept



Single supply

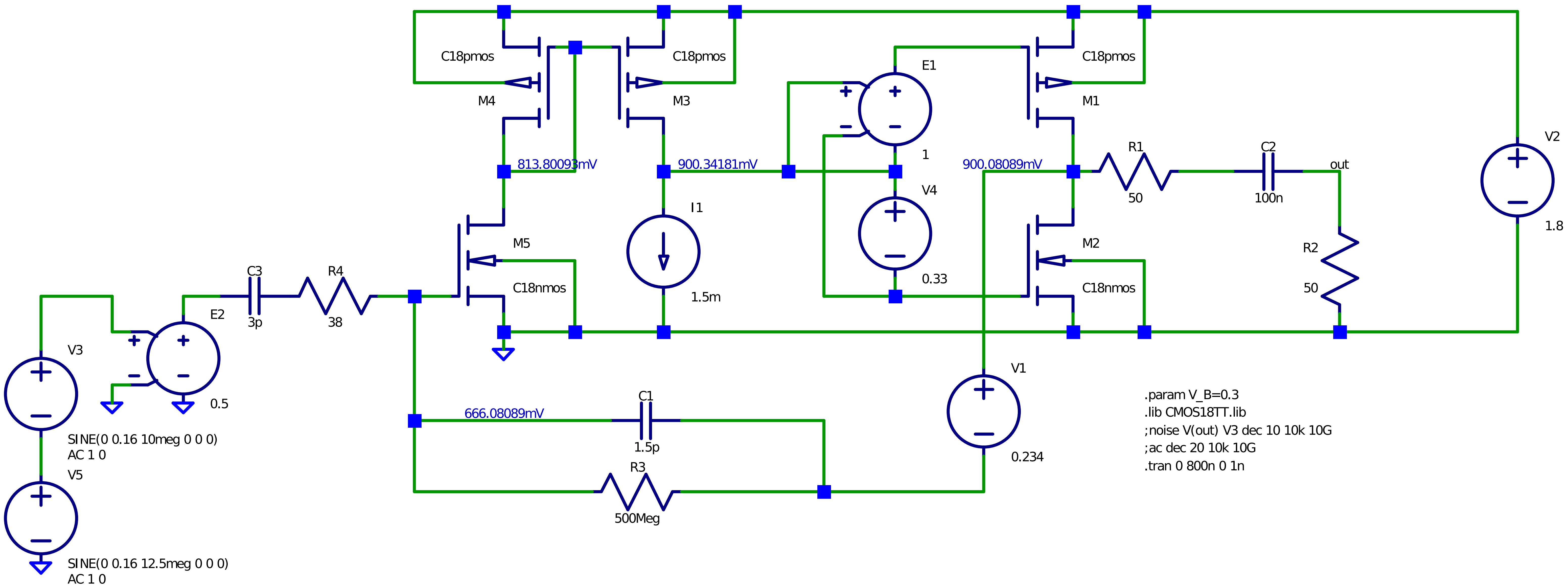
Biasing concept



Single supply

Bias current sources redirected via supply and combined

Biasing concept

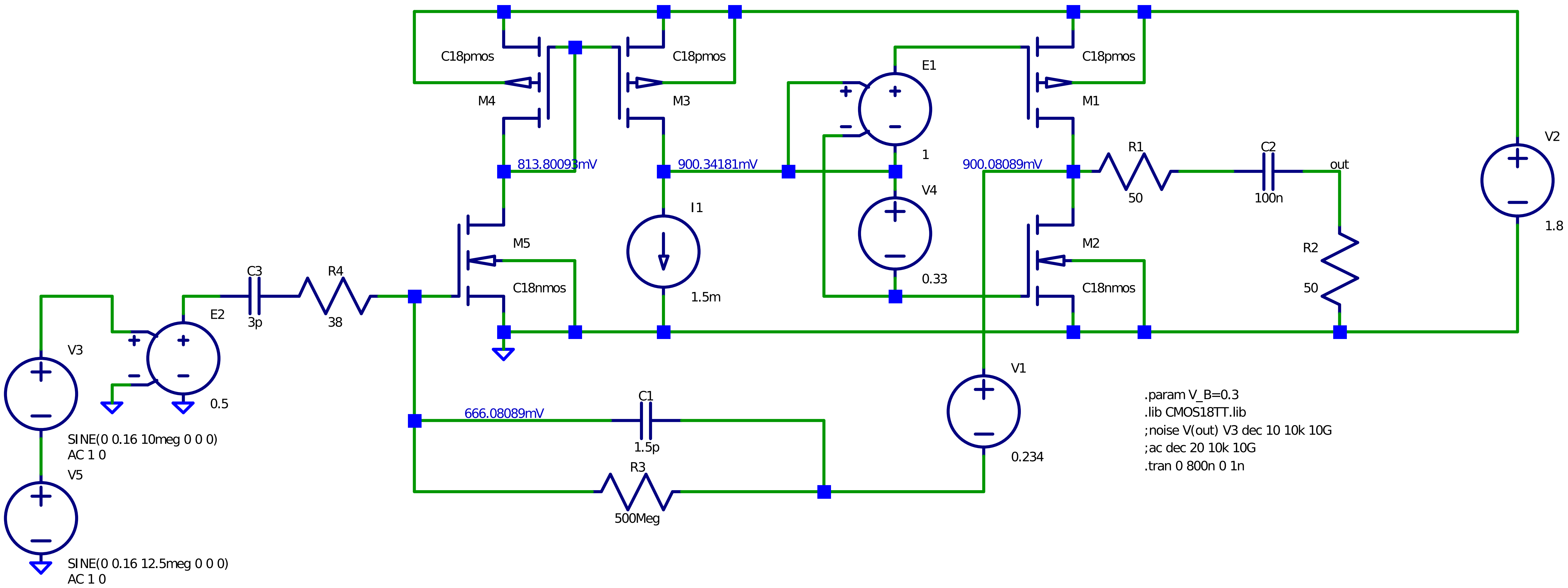


Single supply

Bias current sources redirected via supply and combined

AC coupling and over-all negative feedback biasing

Biasing concept



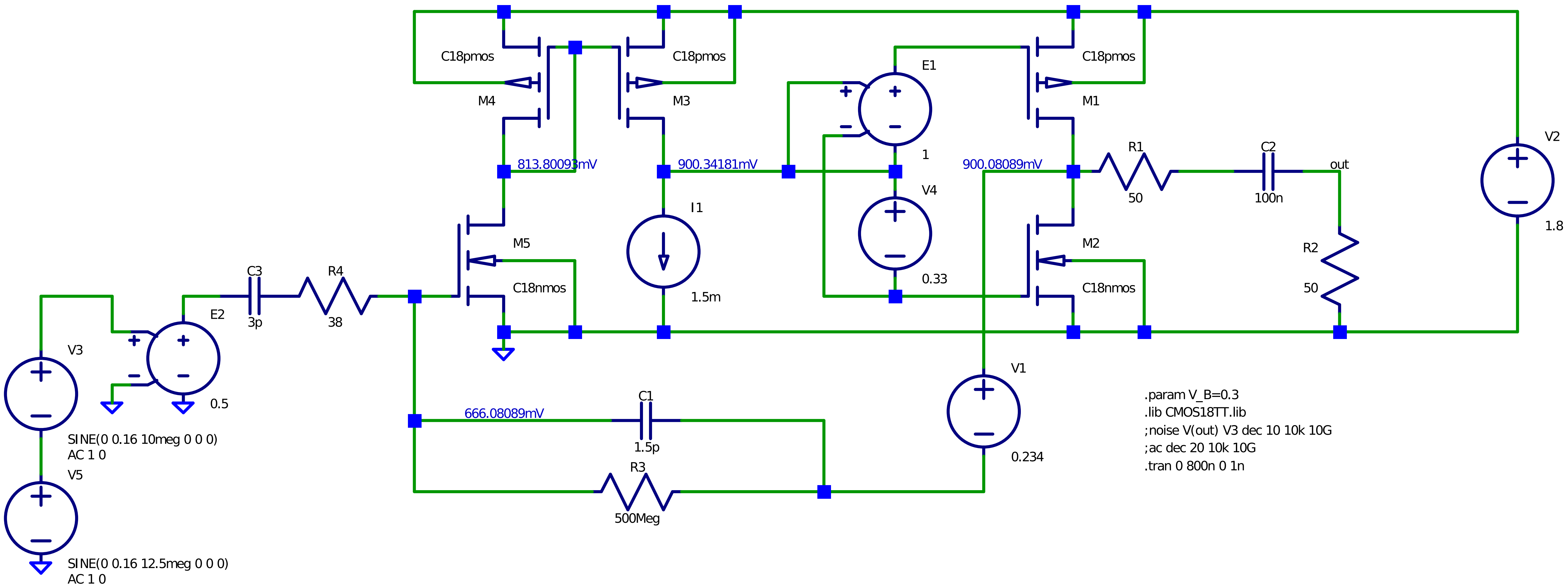
Single supply

Bias current sources redirected via supply and combined

AC coupling and over-all negative feedback biasing

Two or three remaining floating voltage sources

Biasing concept



Single supply

Bias current sources redirected via supply and combined

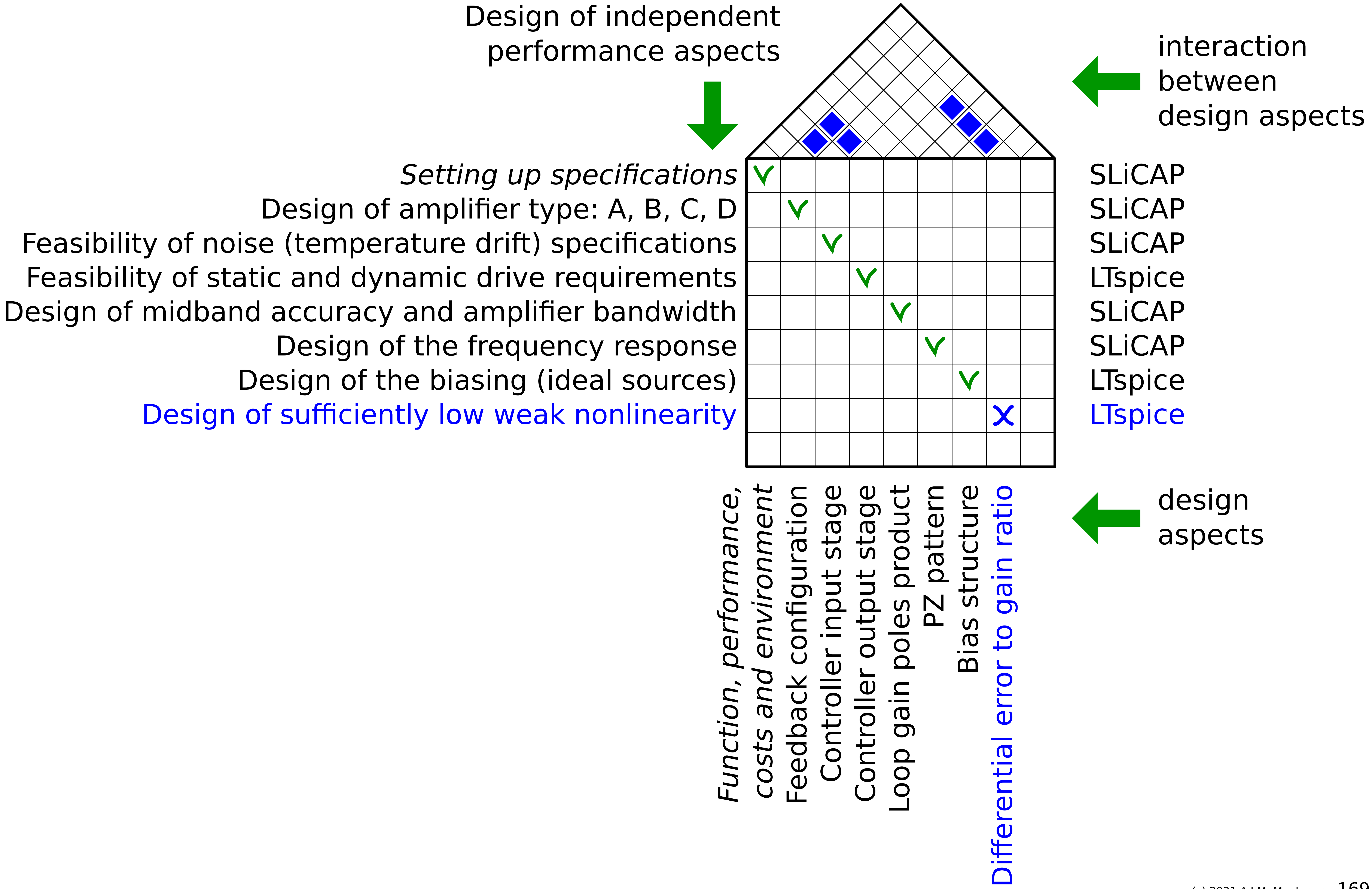
AC coupling and over-all negative feedback biasing

Two or three remaining floating voltage sources

Structured Electronic Design

Step 8
Design of the sufficiently low weak nonlinearity
(ideal bias sources)

Anton J.M. Montagne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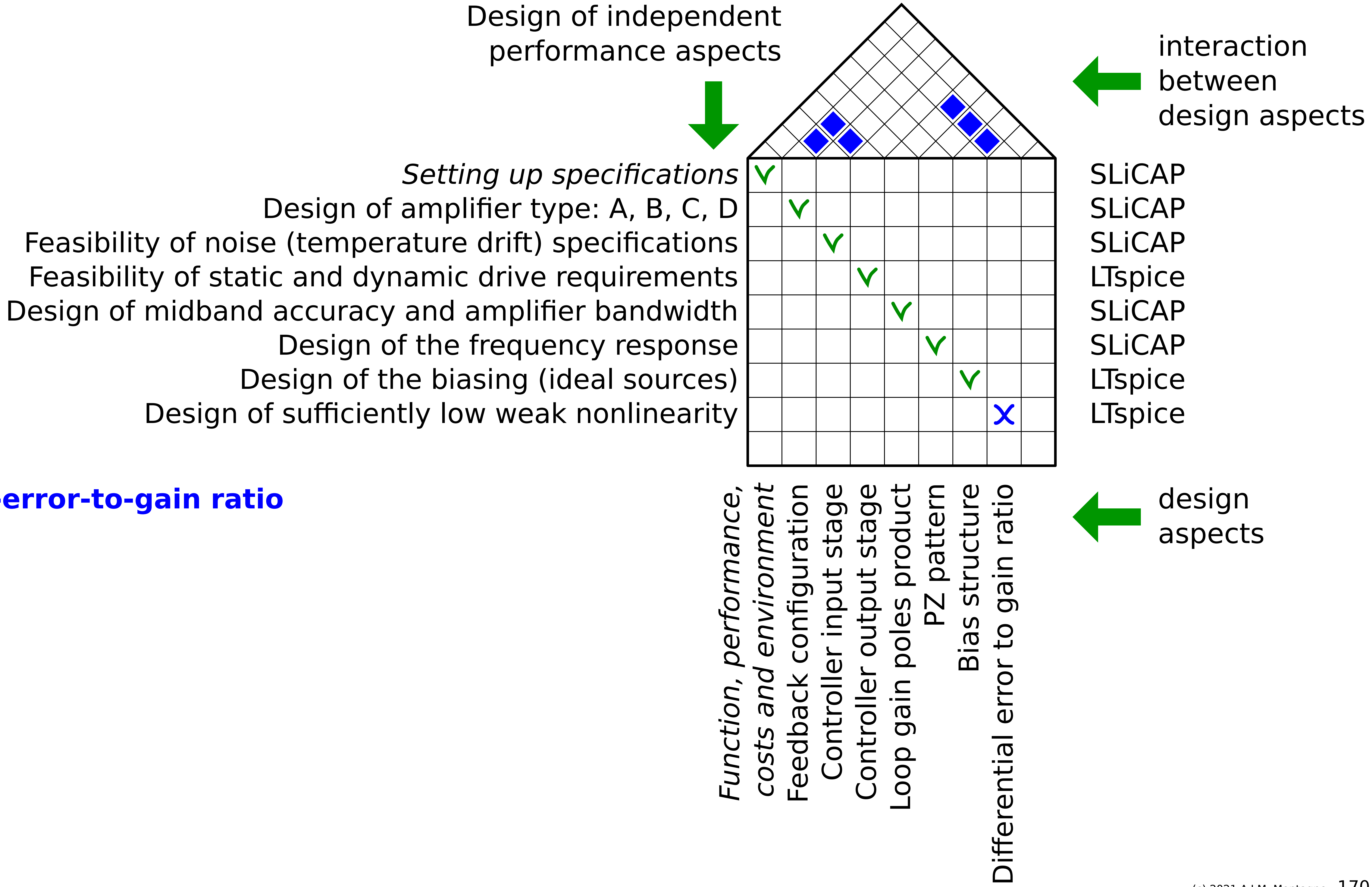
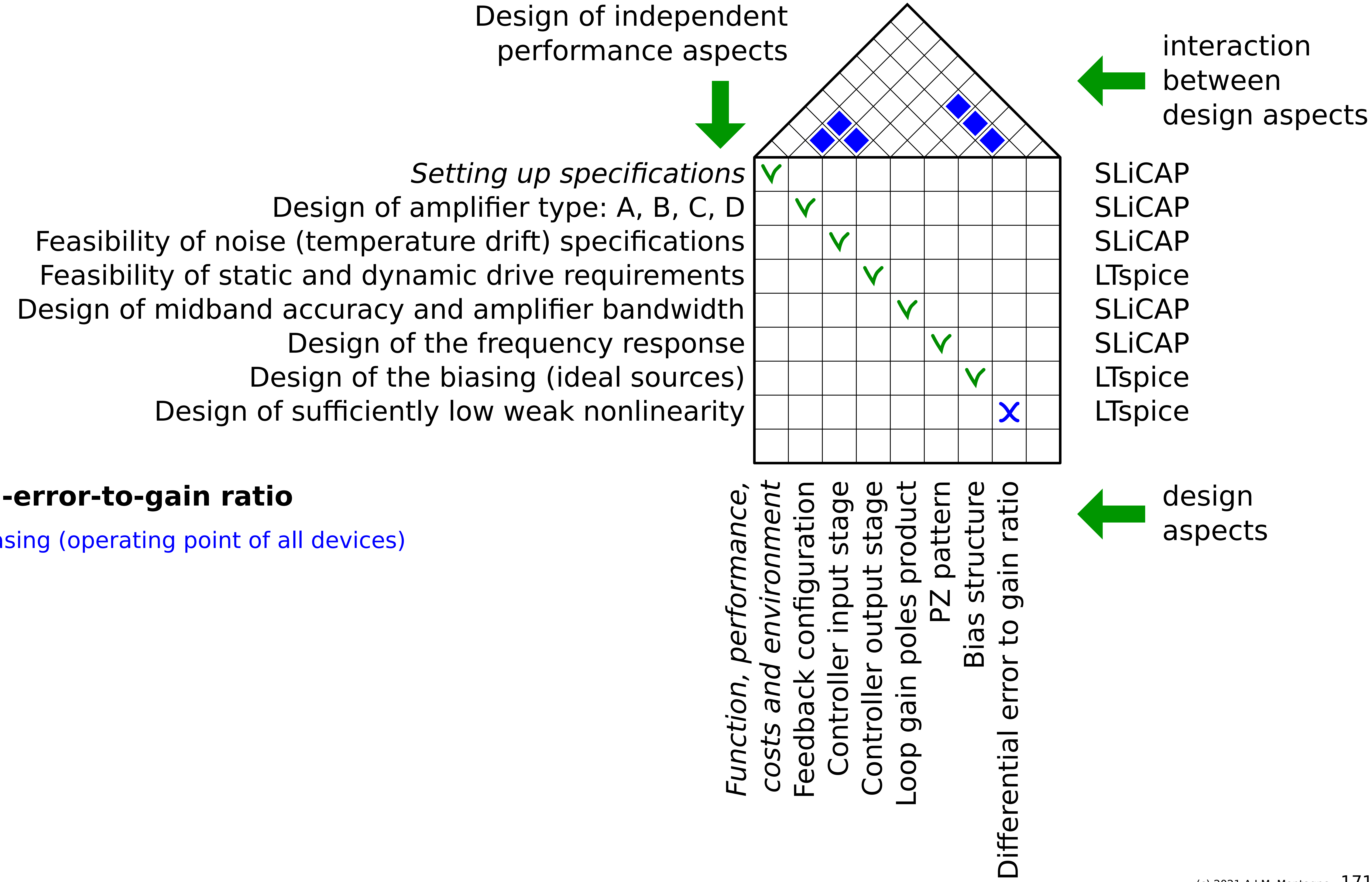
PZ pattern
Bias structure
Differential error to gain ratio
design
aspects

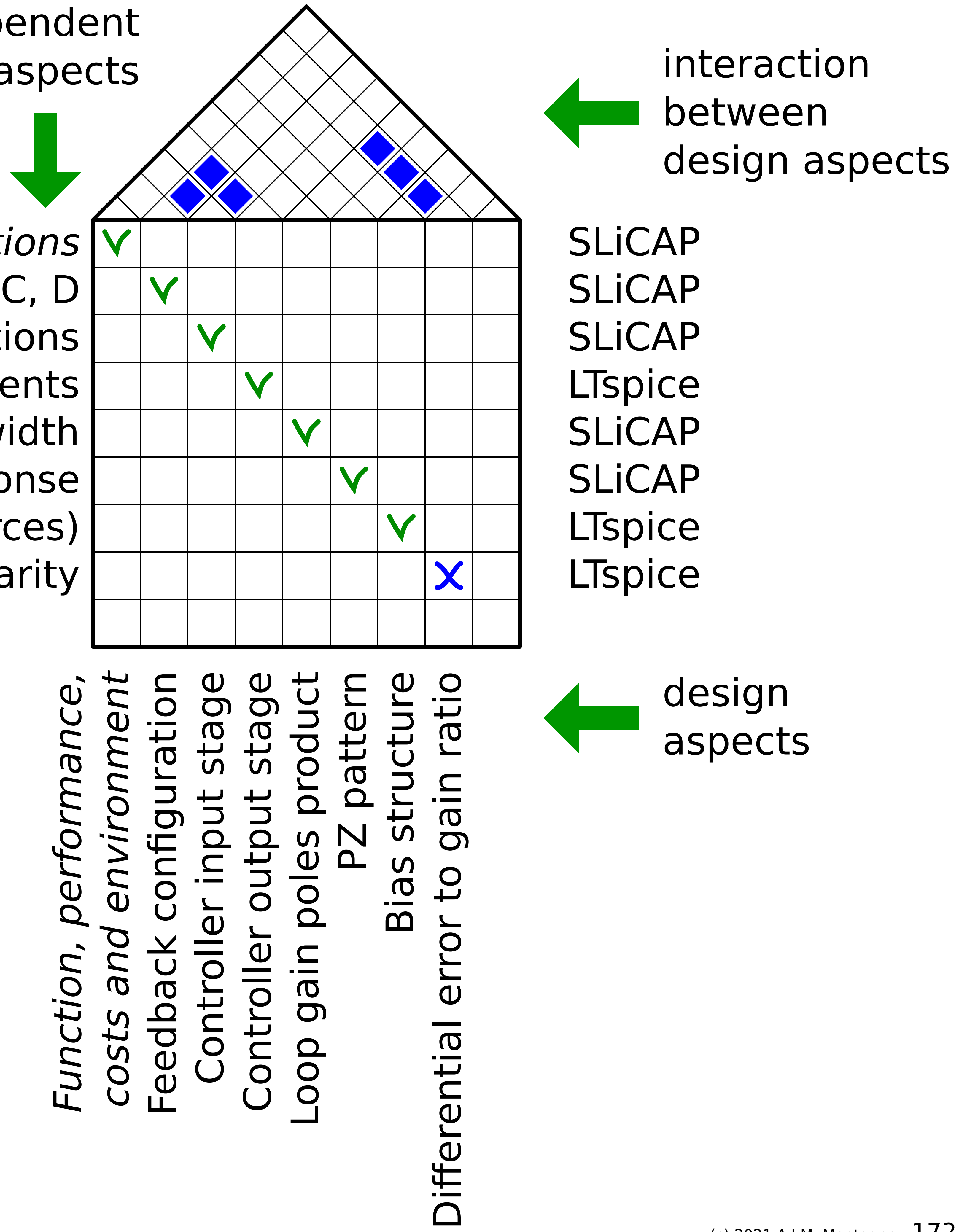
Differential-error-to-gain ratio





Differential-error-to-gain ratio

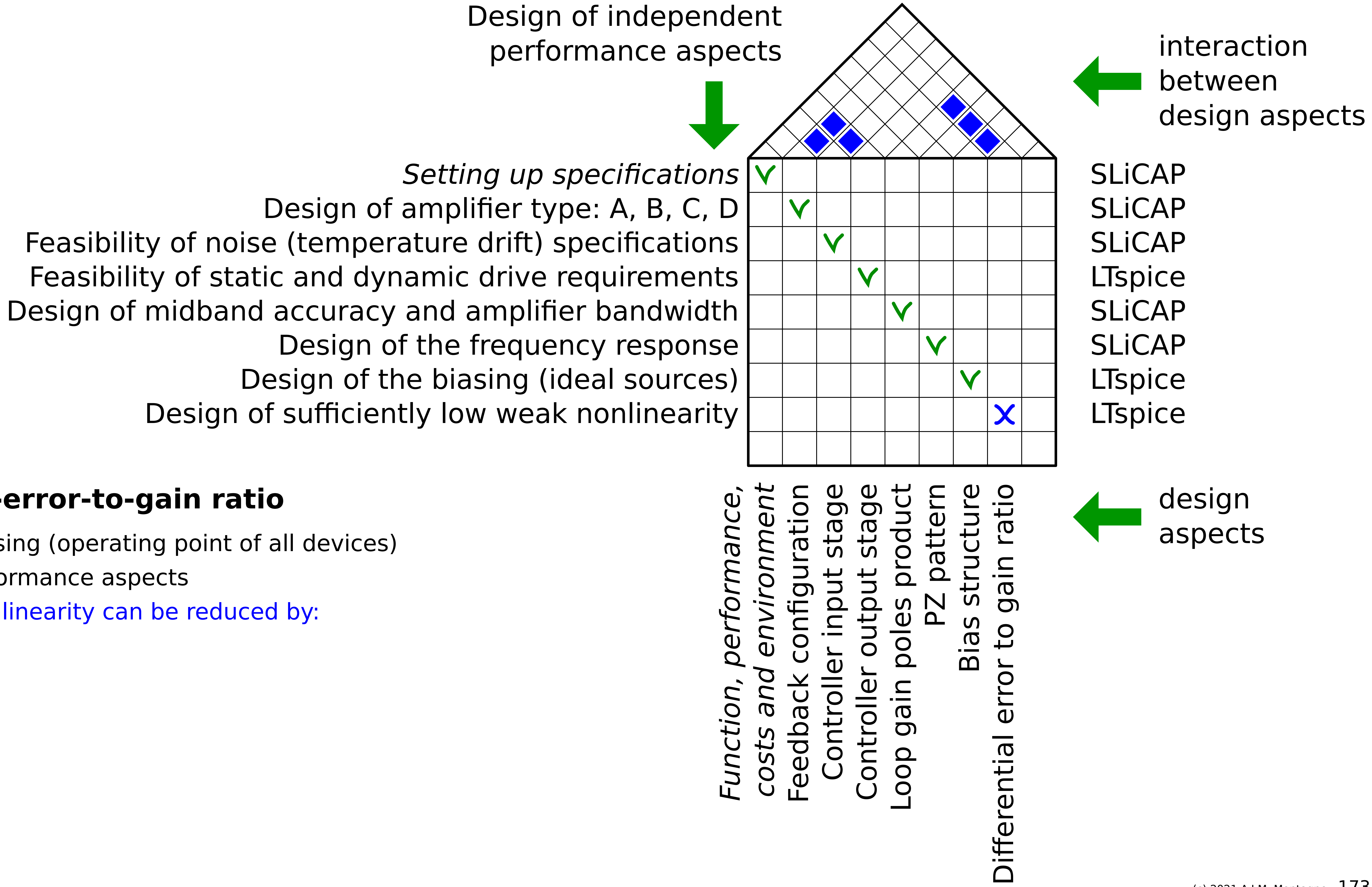
Verify the biasing (operating point of all devices)



Differential-error-to-gain ratio

Verify the biasing (operating point of all devices)

Verify all performance aspects

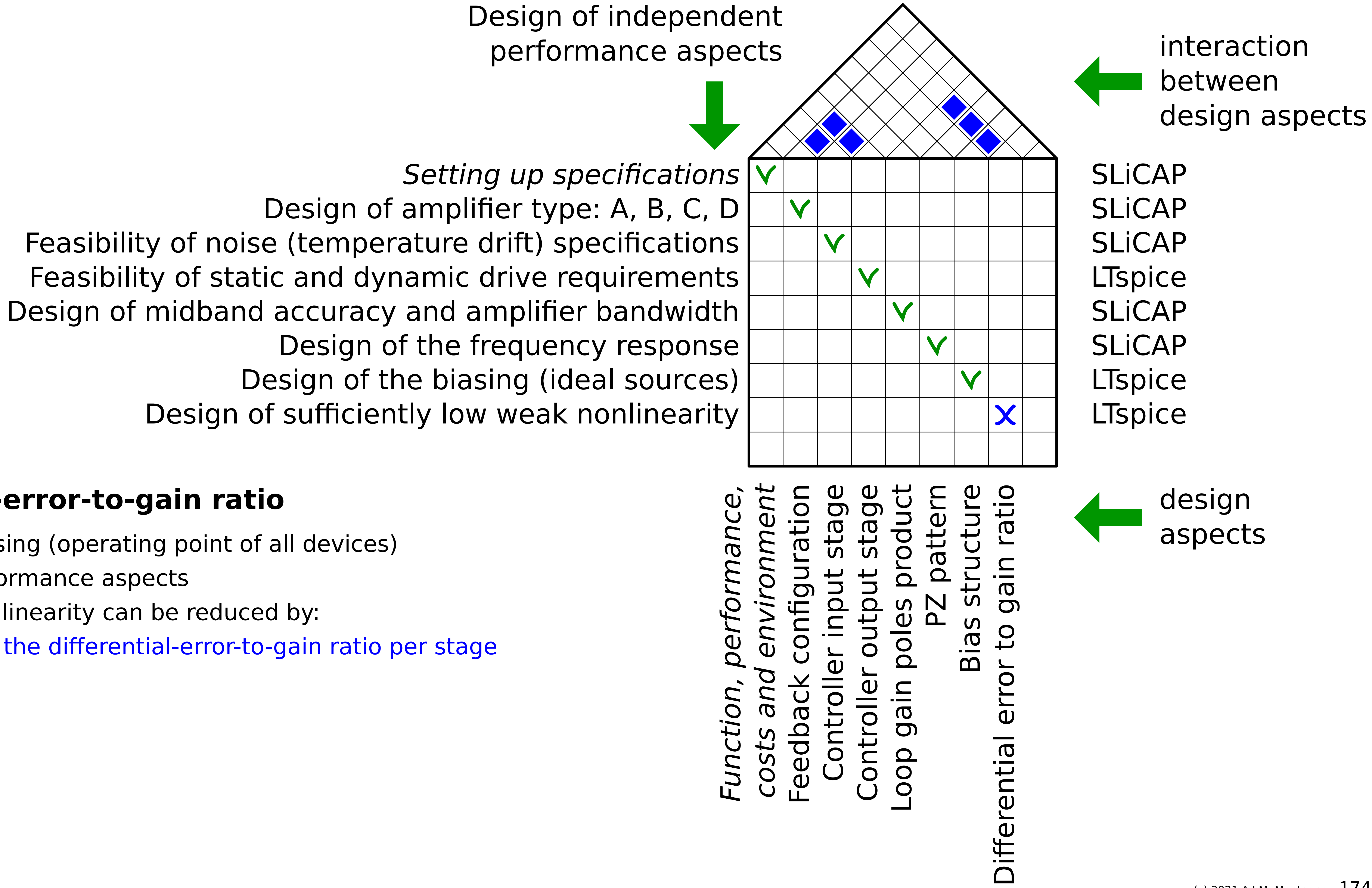


Differential-error-to-gain ratio

Verify the biasing (operating point of all devices)

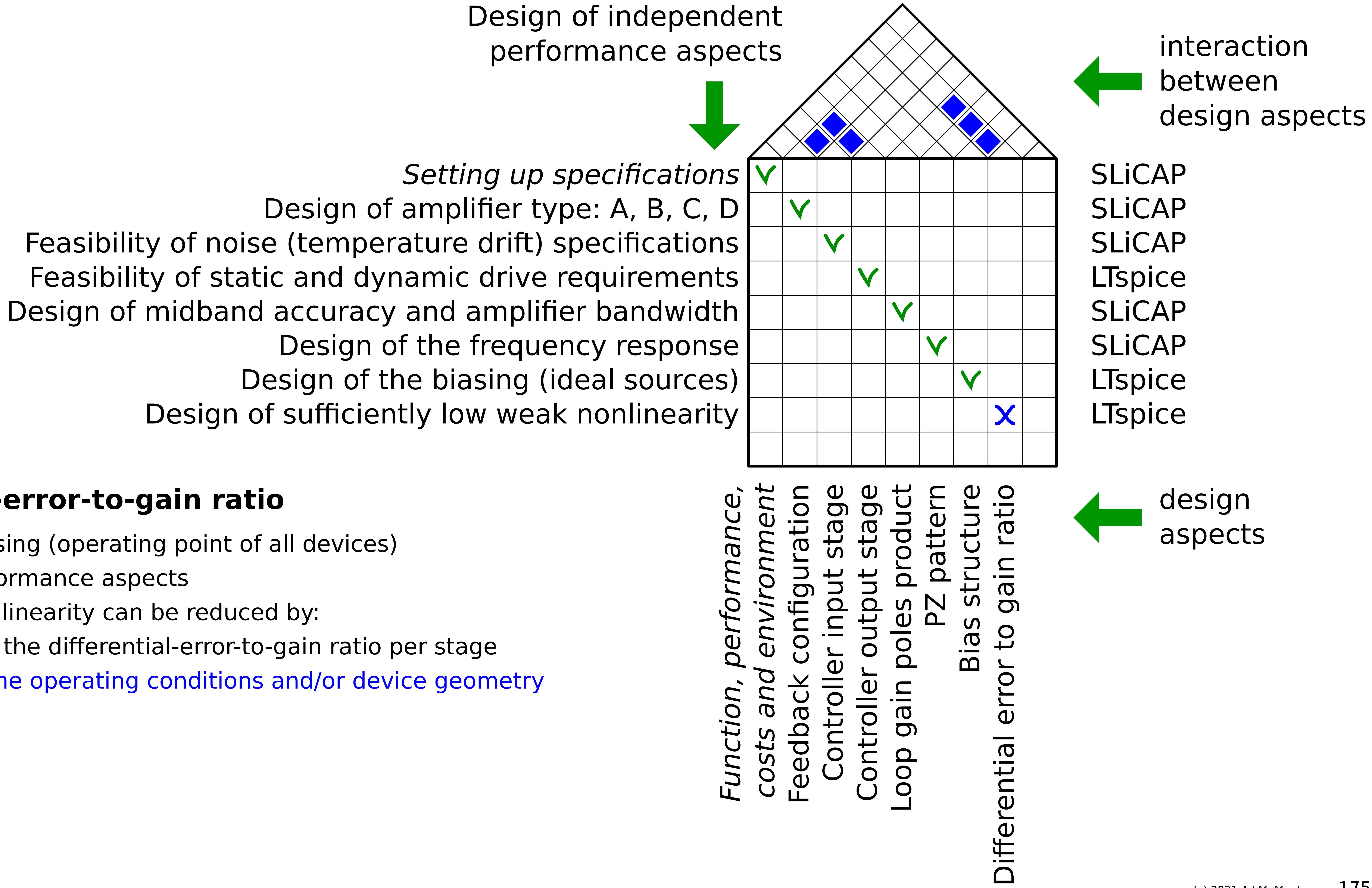
Verify all performance aspects

The weak nonlinearity can be reduced by:



Differential-error-to-gain ratio

- Verify the biasing (operating point of all devices)
- Verify all performance aspects
- The weak nonlinearity can be reduced by:
  - Decreasing the differential-error-to-gain ratio per stage



Differential-error-to-gain ratio

- Verify the biasing (operating point of all devices)
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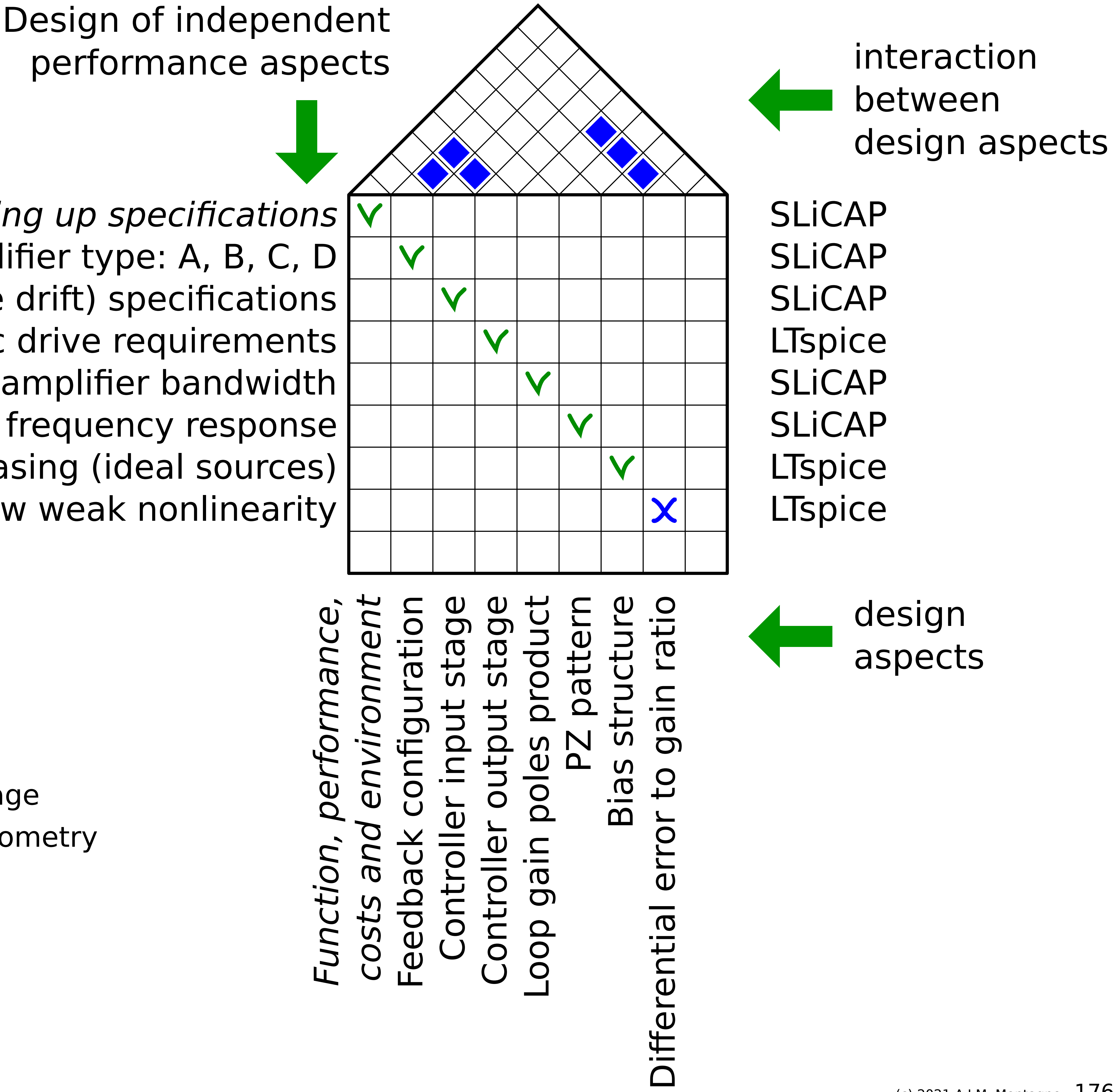
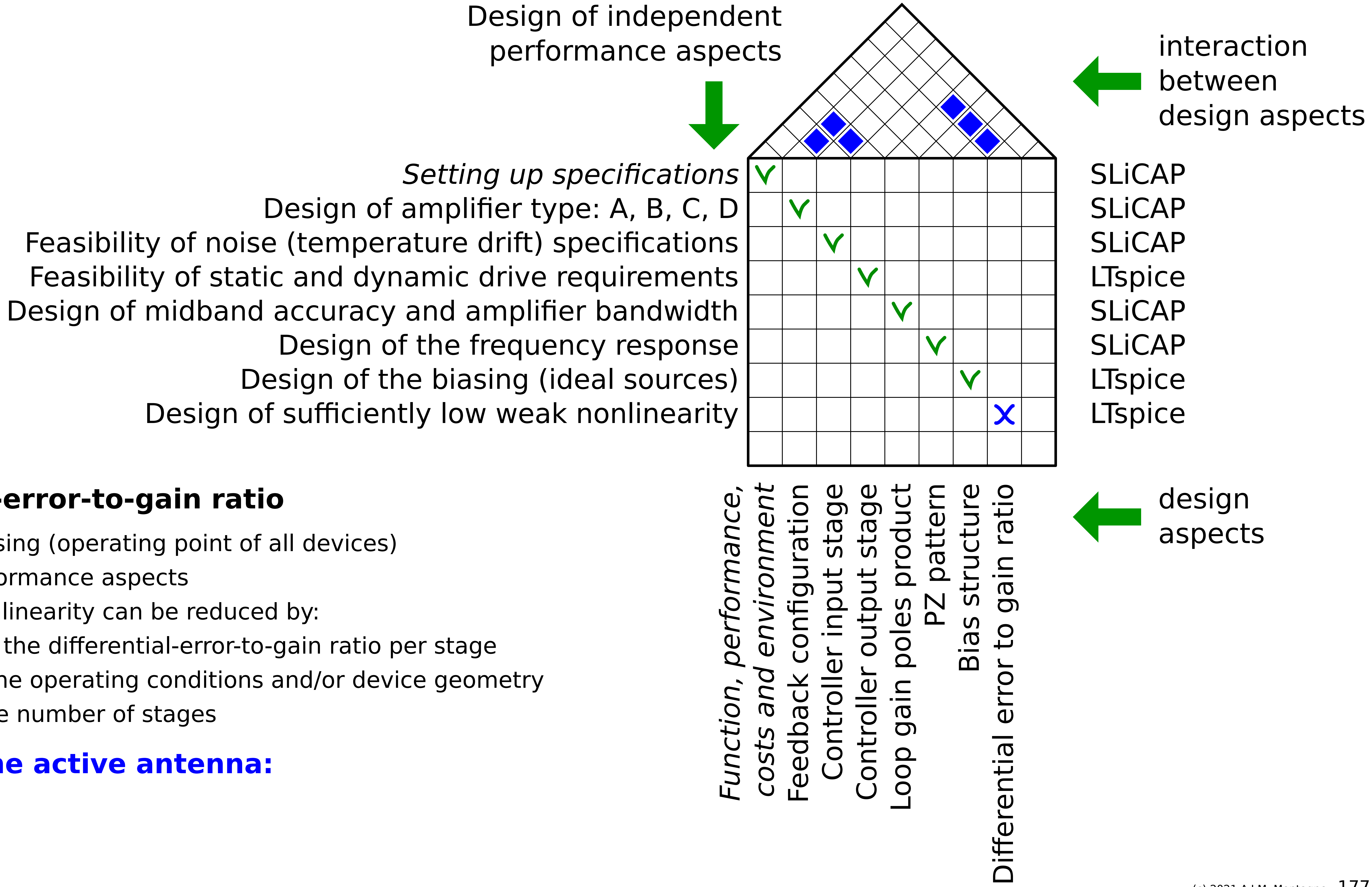
  - Increase the number of stages





Differential-error-to-gain ratio

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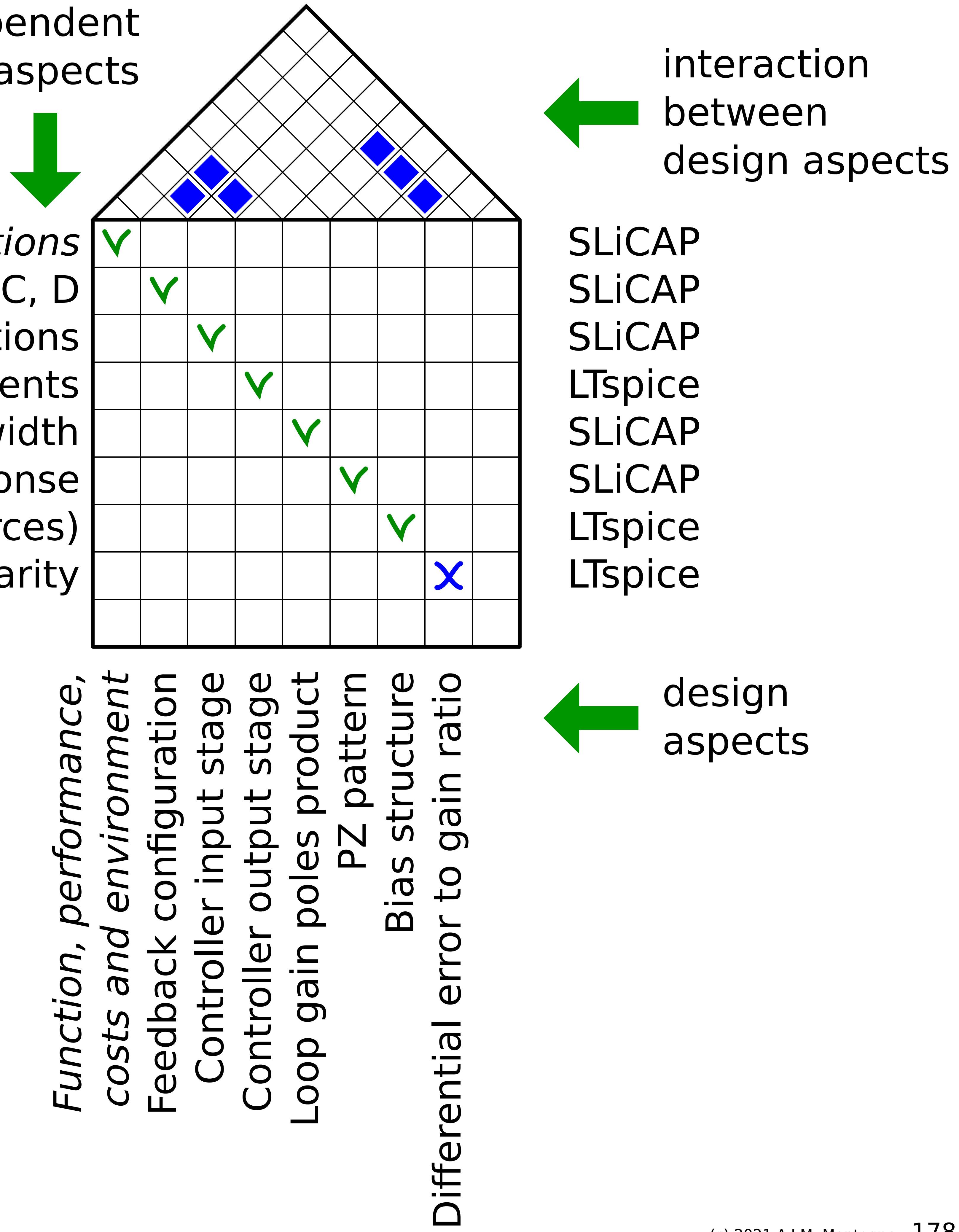
Design of the active antenna:



Differential-error-to-gain ratio

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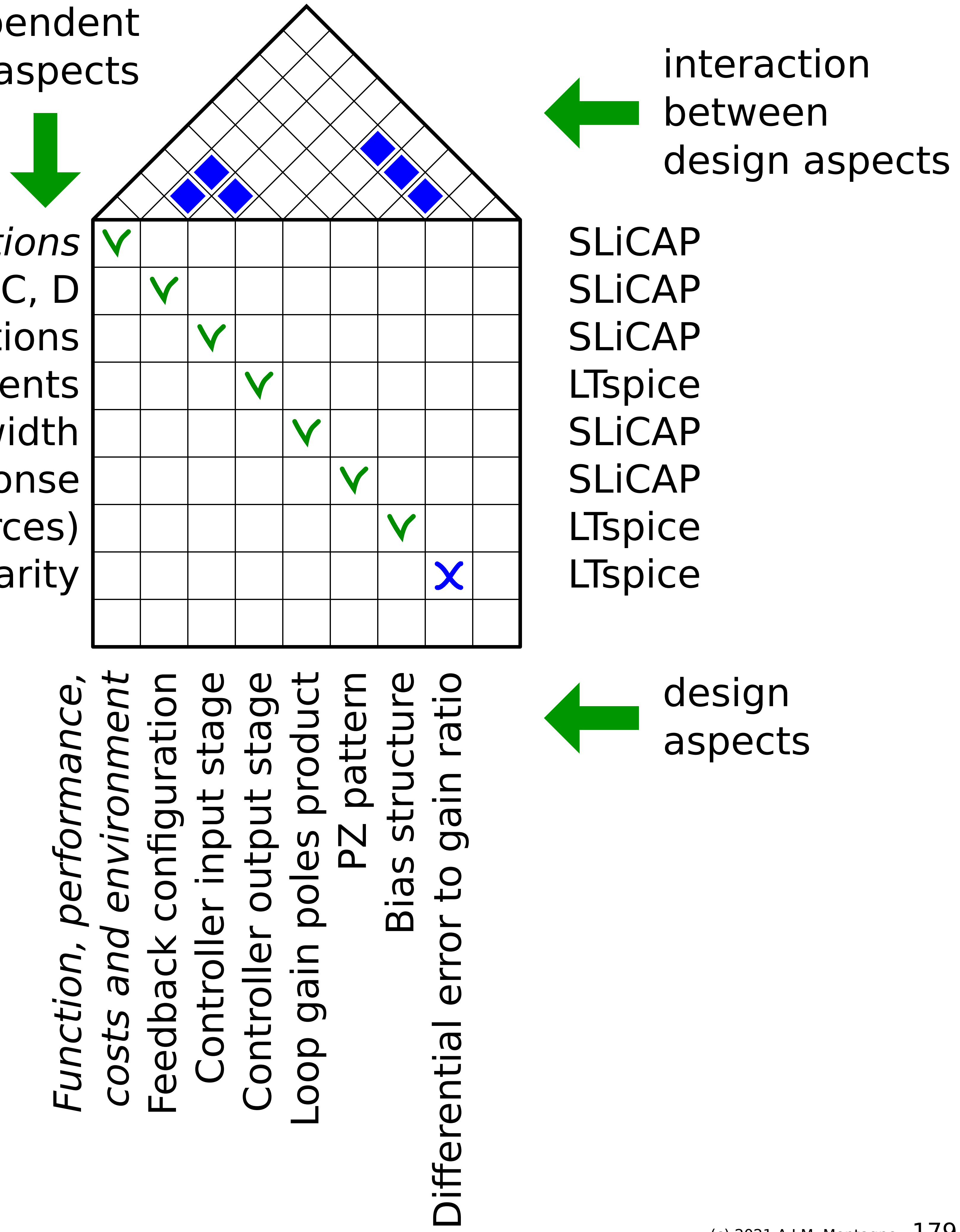
  - Increase the number of stages

Design of the active antenna:

- Verification showed sufficiently low distortion



Differential-error-to-gain ratio

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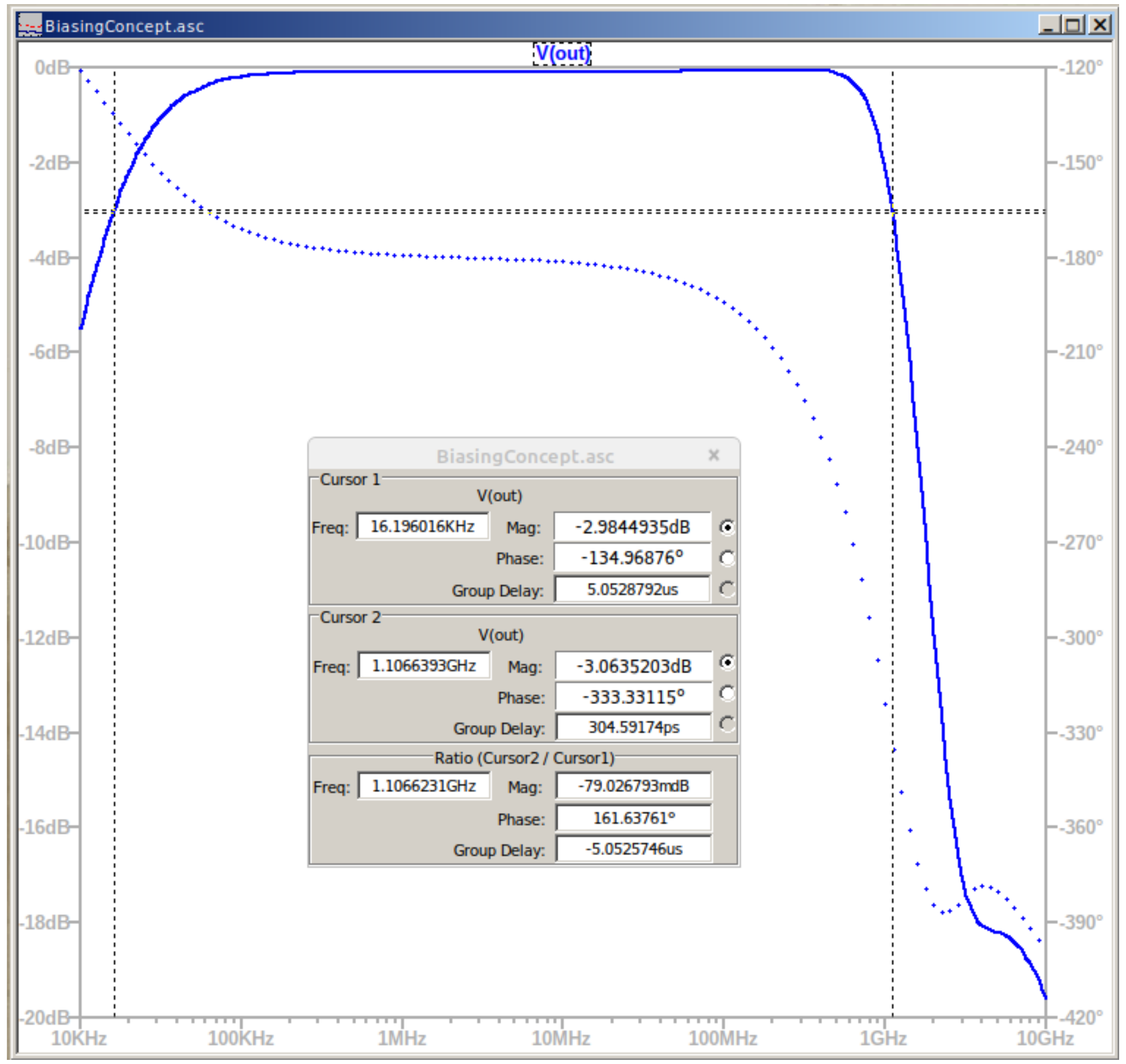
Design of the active antenna:

- Verification showed sufficiently low distortion

Check performance

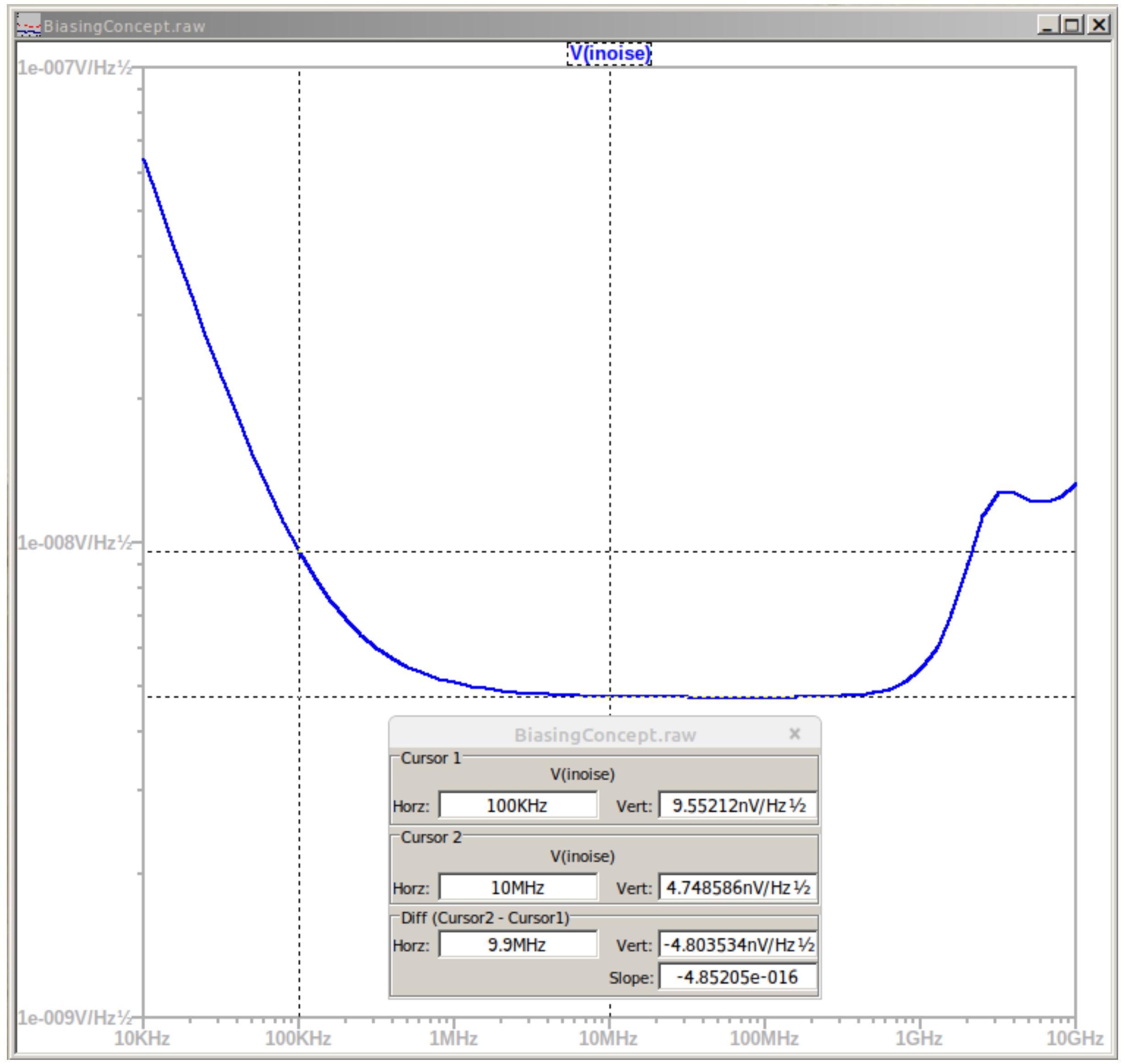
Check performance

Frequency response



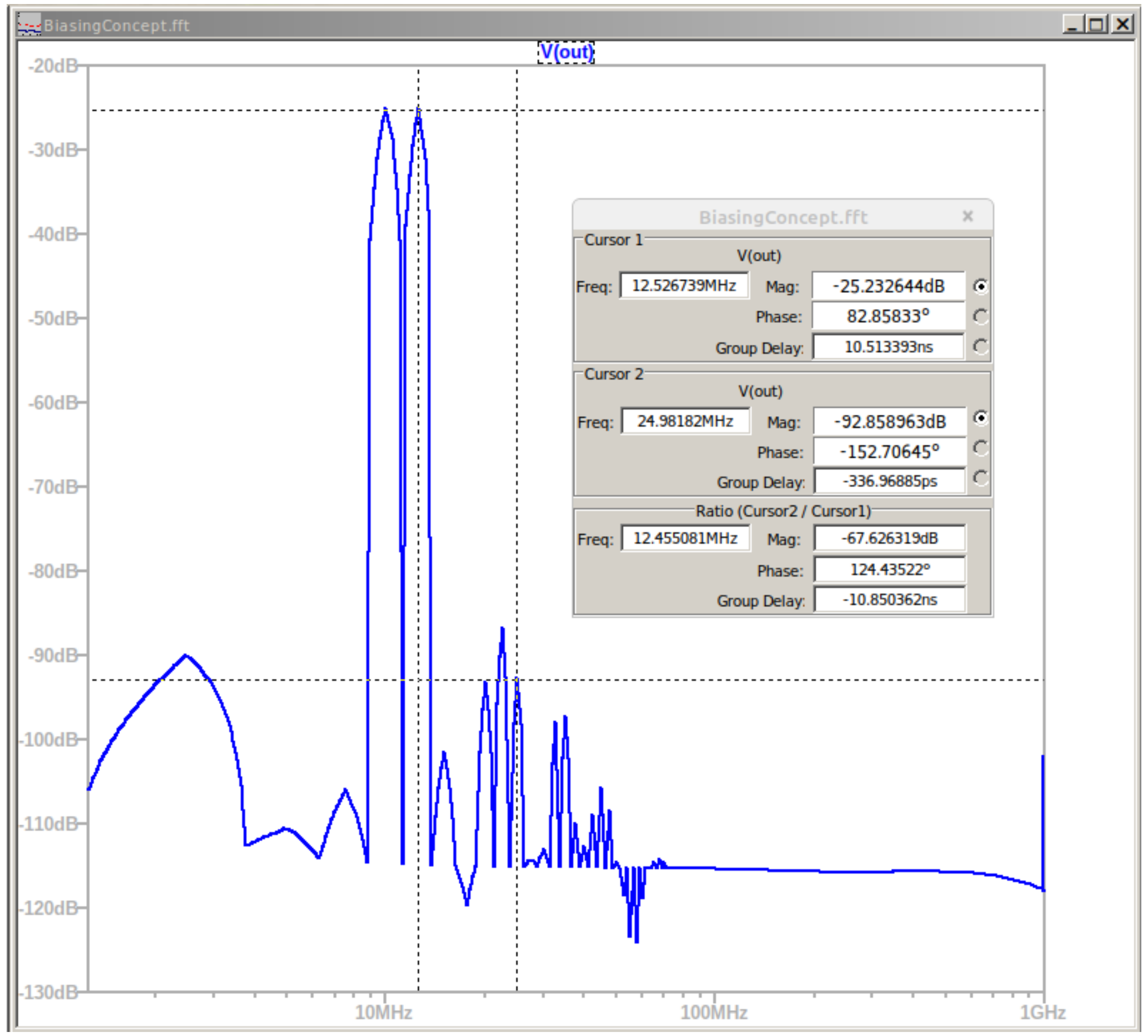
Check performance

Antenna referred noise



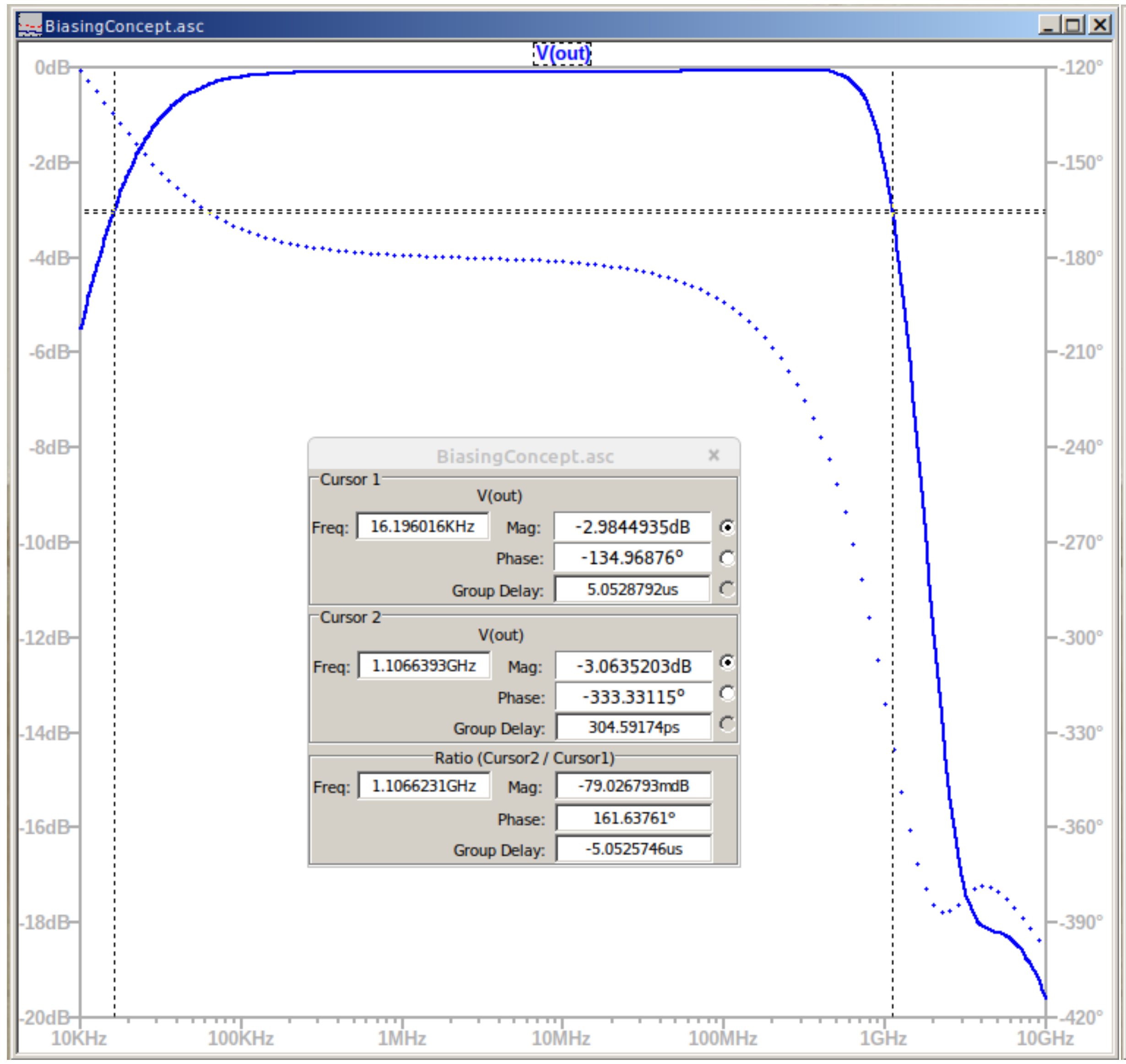
Check performance

IMD

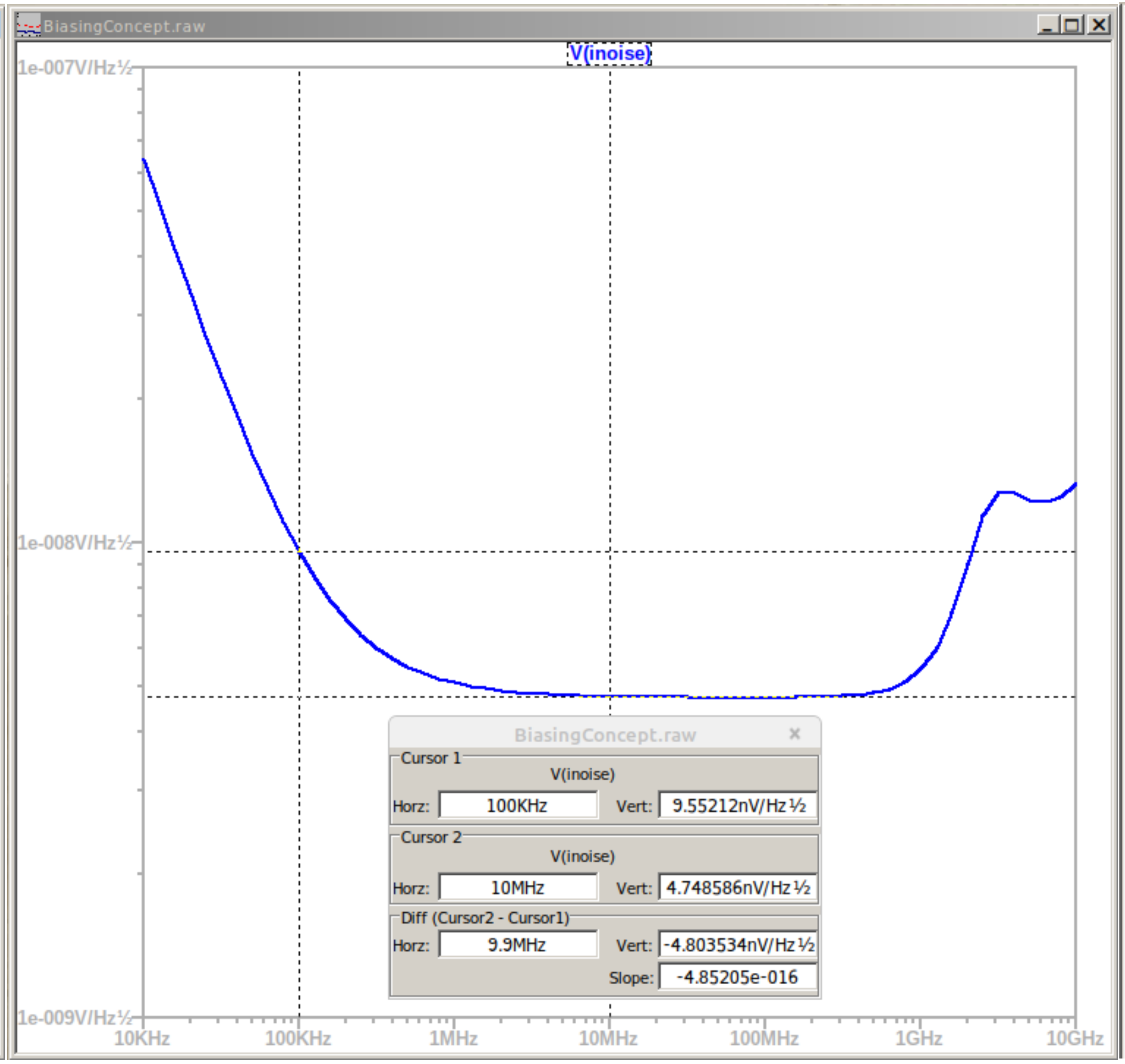


Check performance

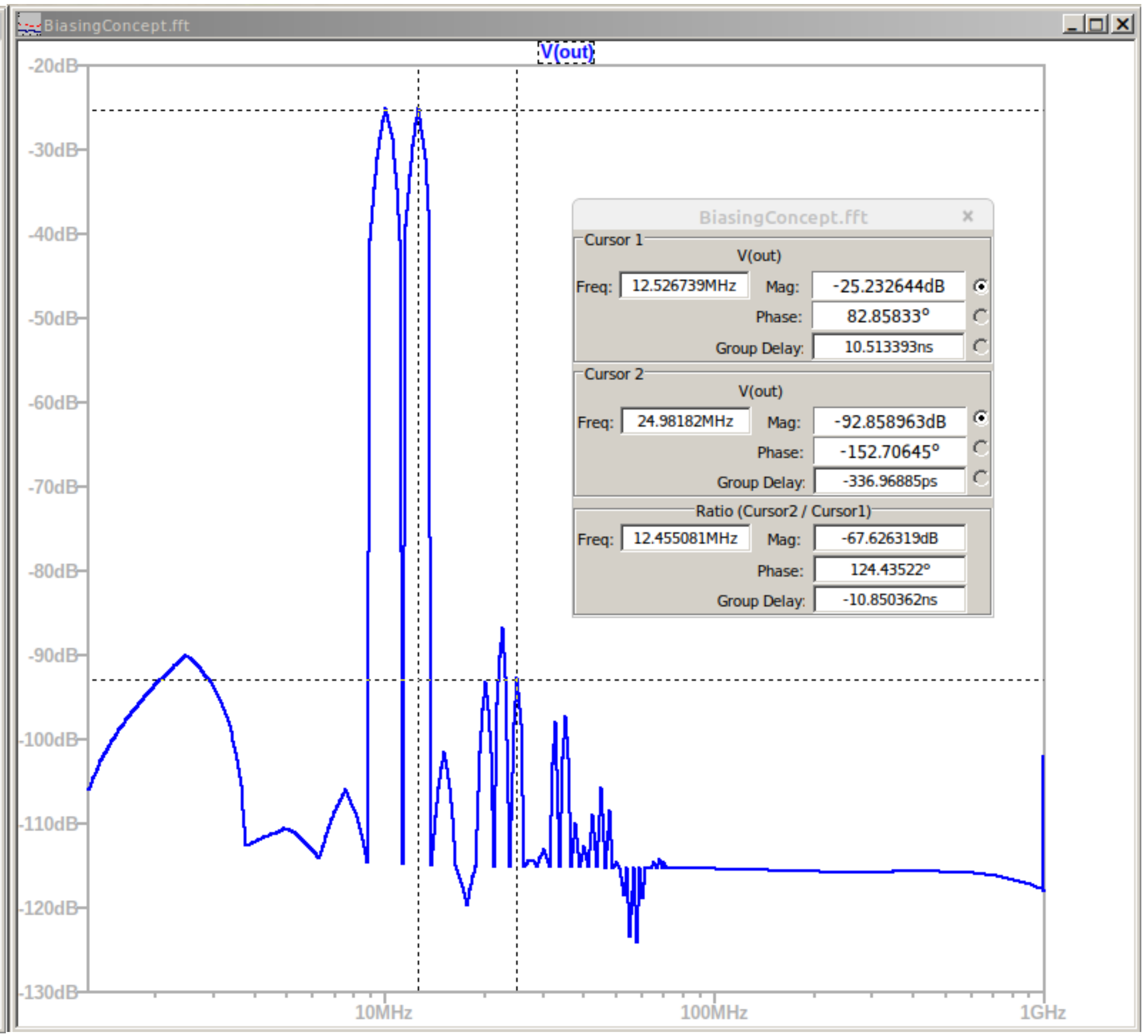
Frequency response



Antenna referred noise



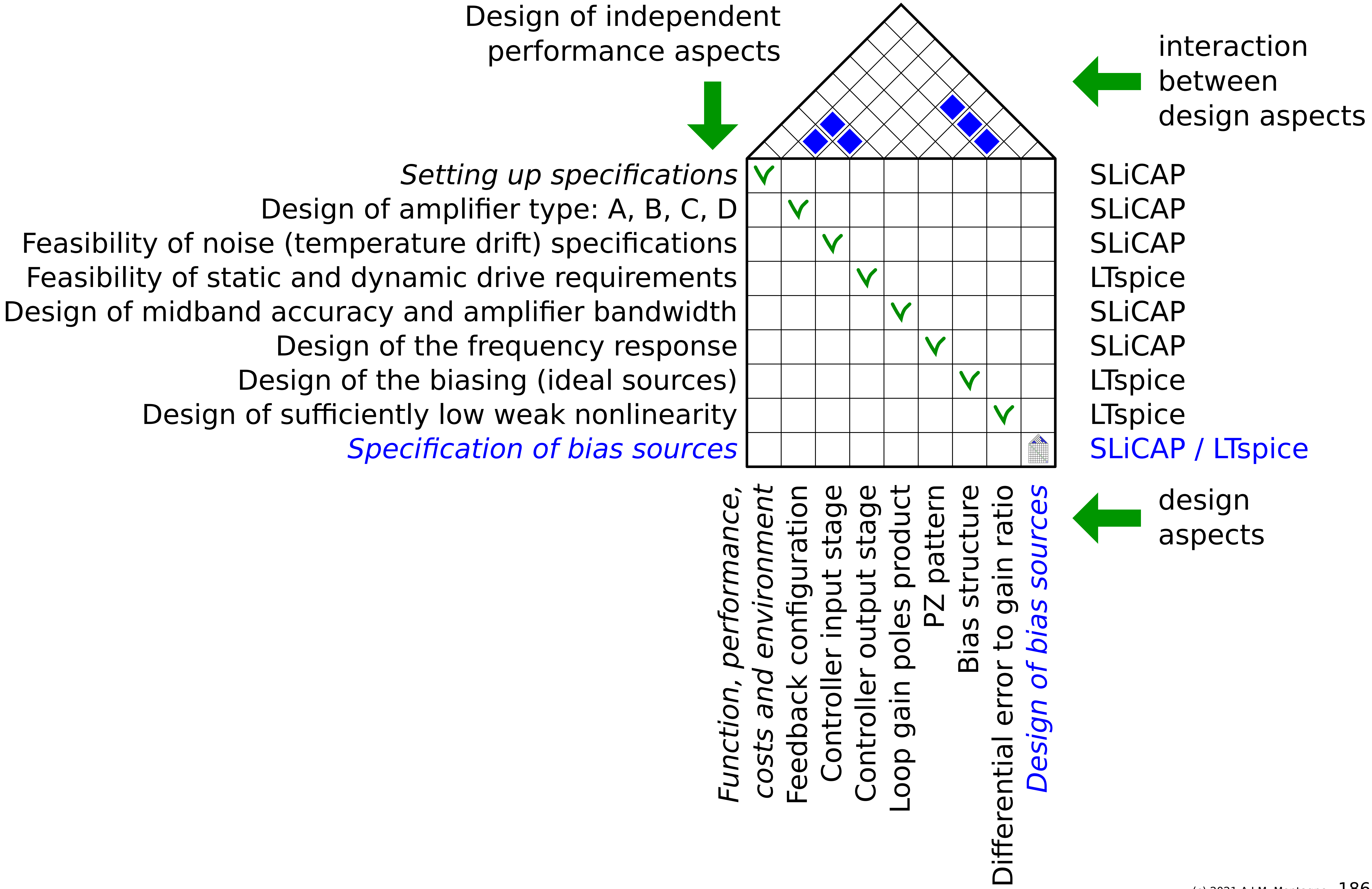
IMD

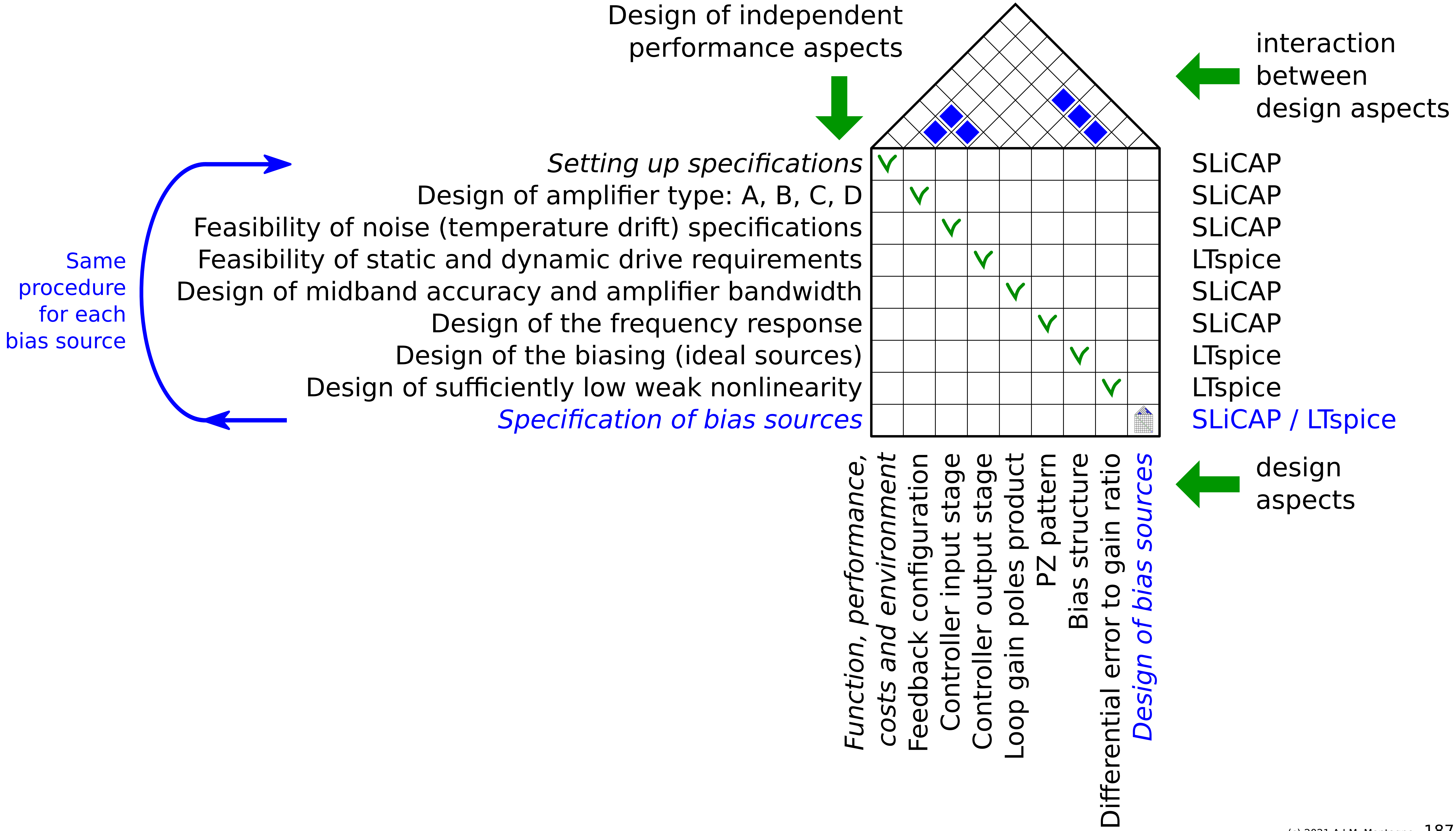


Structured Electronic Design

Step 9
Design of the bias sources

Anton J.M. Montagne


Design of independent performance aspects
interaction between design aspects
Setting up specifications
Design of amplifier type: A, B, C, D
Feasibility of noise (temperature drift) specifications
Feasibility of static and dynamic drive requirements
Design of midband accuracy and amplifier bandwidth
Design of the frequency response
Design of the biasing (ideal sources)
Design of sufficiently low weak nonlinearity
Specification of bias sources
SLiCAP
SLiCAP
SLiCAP
LTspice
SLiCAP
SLiCAP
LTspice
LTspice
SLiCAP / LTspice
Function, performance, costs and environment
Feedback configuration
Controller input stage
Controller output stage
Loop gain poles product
PZ pattern
Bias structure
Differential error to gain ratio
Design of bias sources
design aspects



Design of independent
performance aspects
interaction
between
design aspects
Same
procedure
for each
bias source
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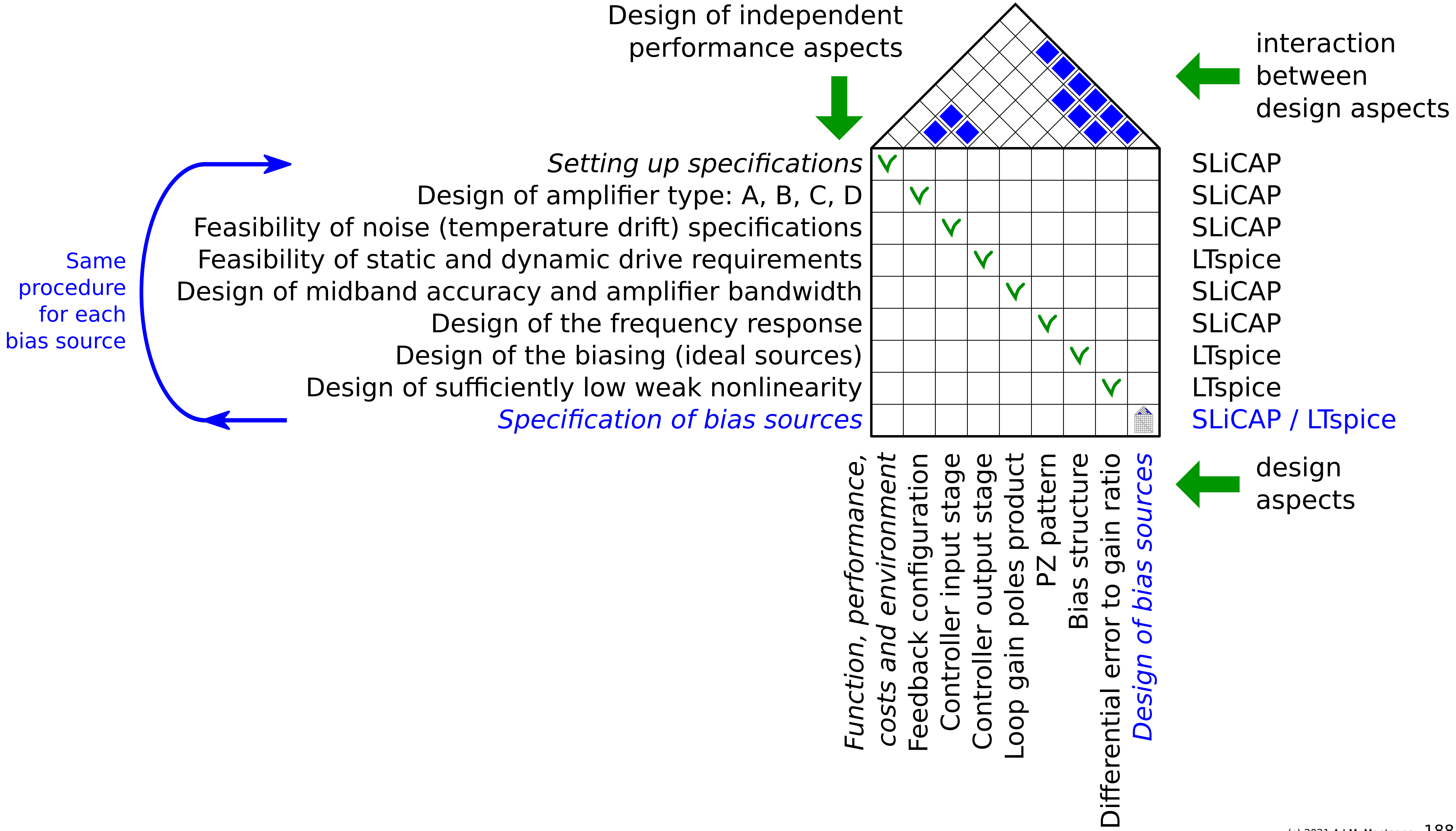
Bias structure
Differential error to gain ratio
Design of bias sources
design
aspects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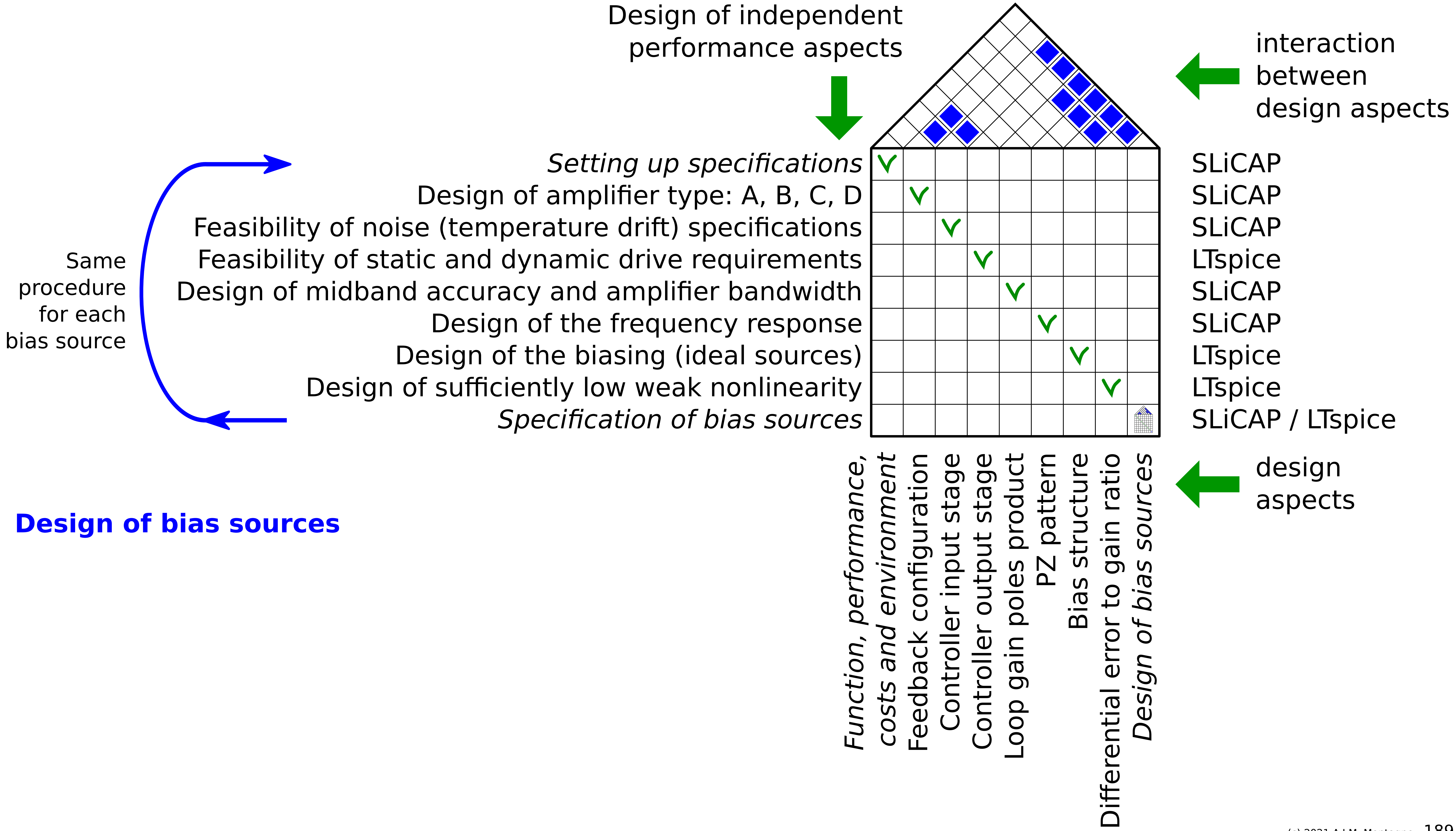
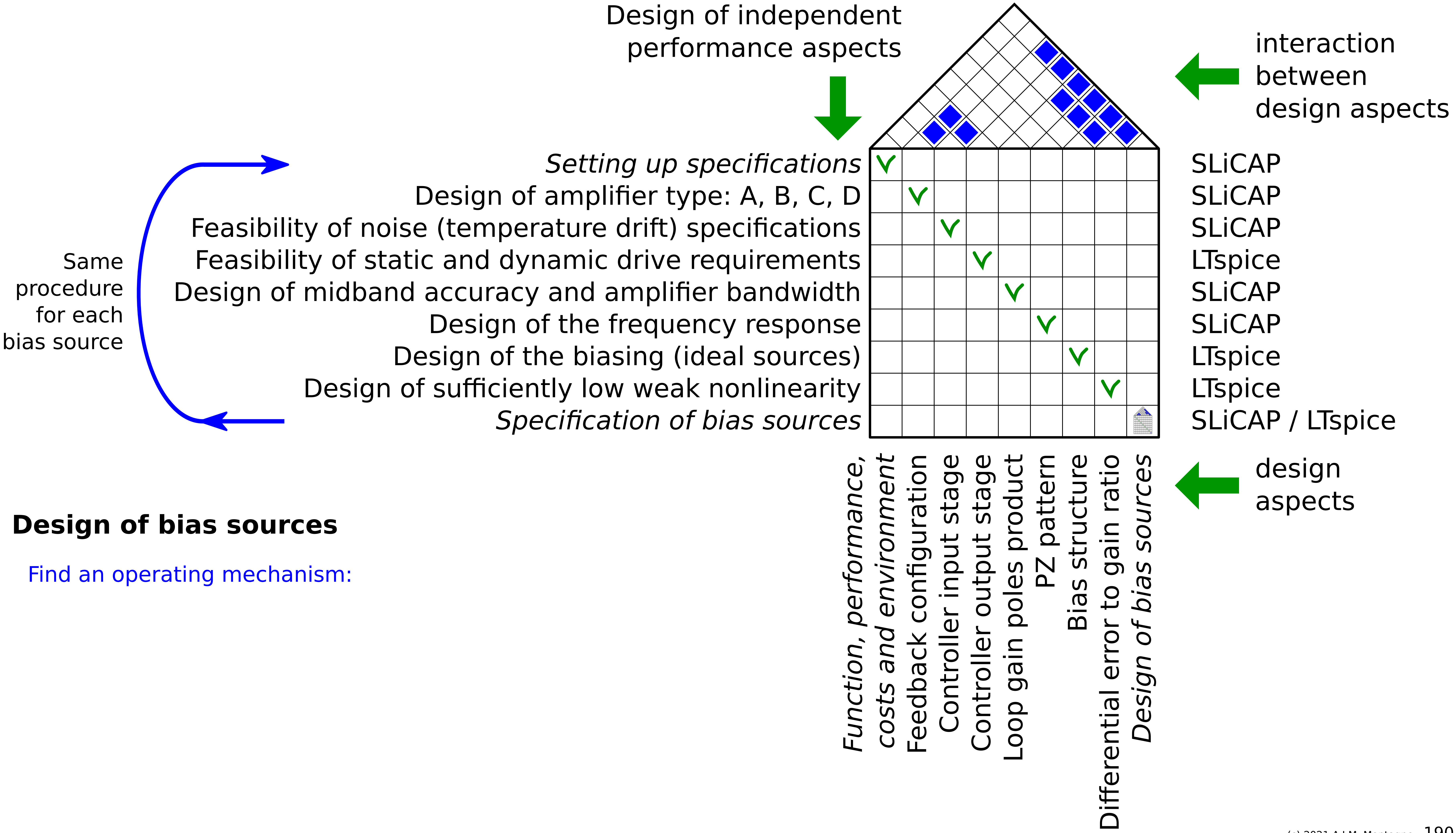
Design of bias sources
design aspects

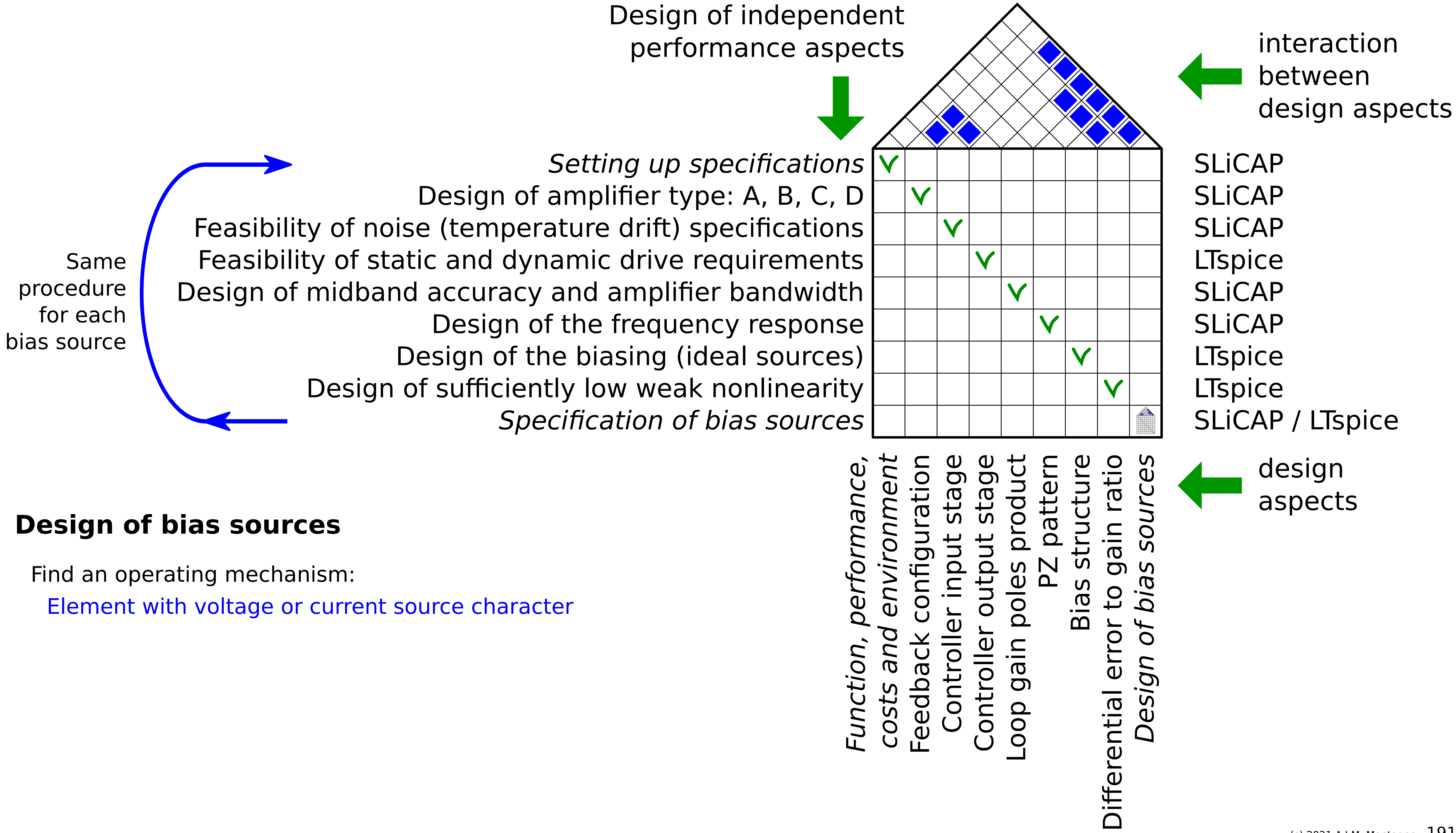


Design of bias sources



Design of bias sources

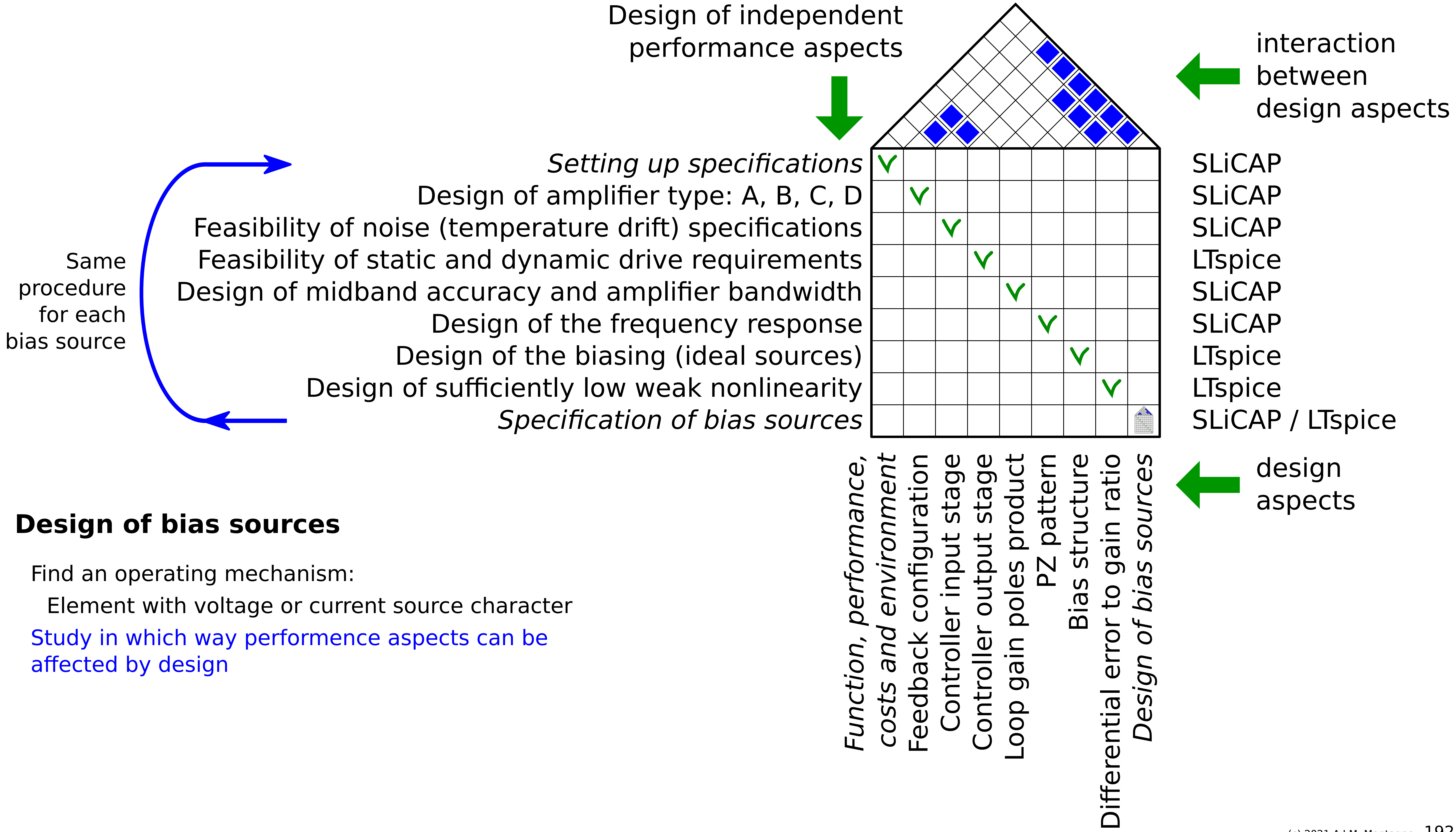
Find an operating mechanism:



Design of bias sources

Find an operating mechanism:

Element with voltage or current source character



Design of bias sources

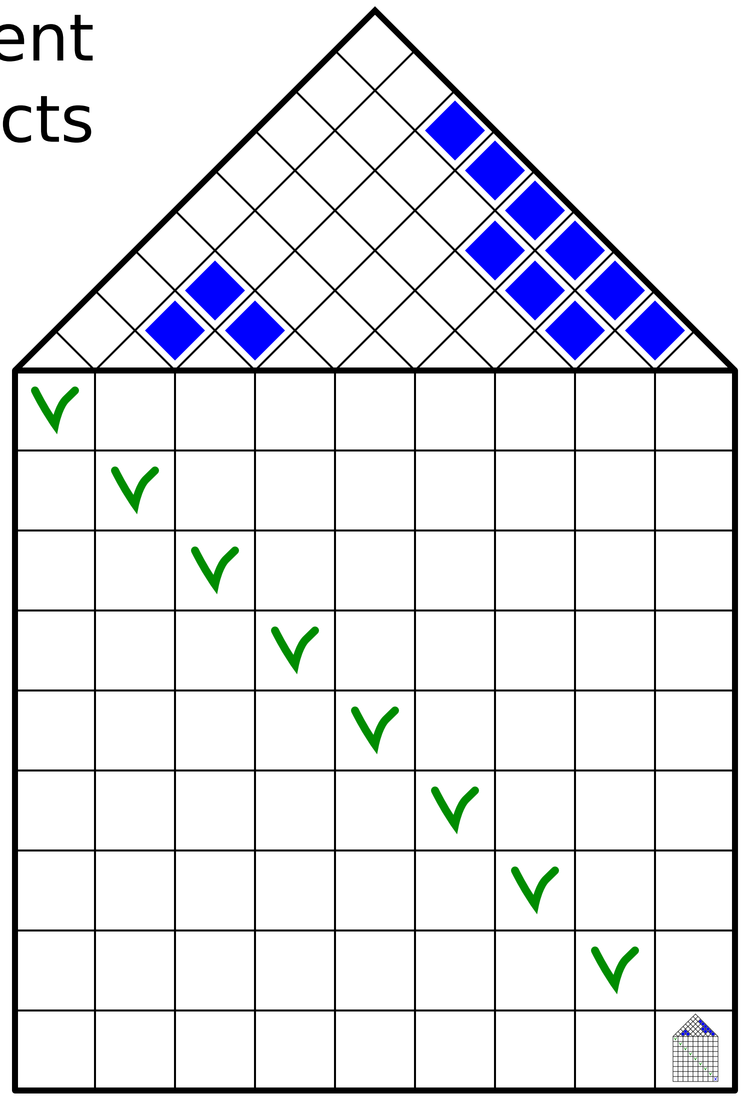
Find an operating mechanism:

Element with voltage or current source character

Study in which way performence aspects can be affected by design

Design of independent performance aspects

interaction between design aspects



Same procedure for each bias source

design aspects

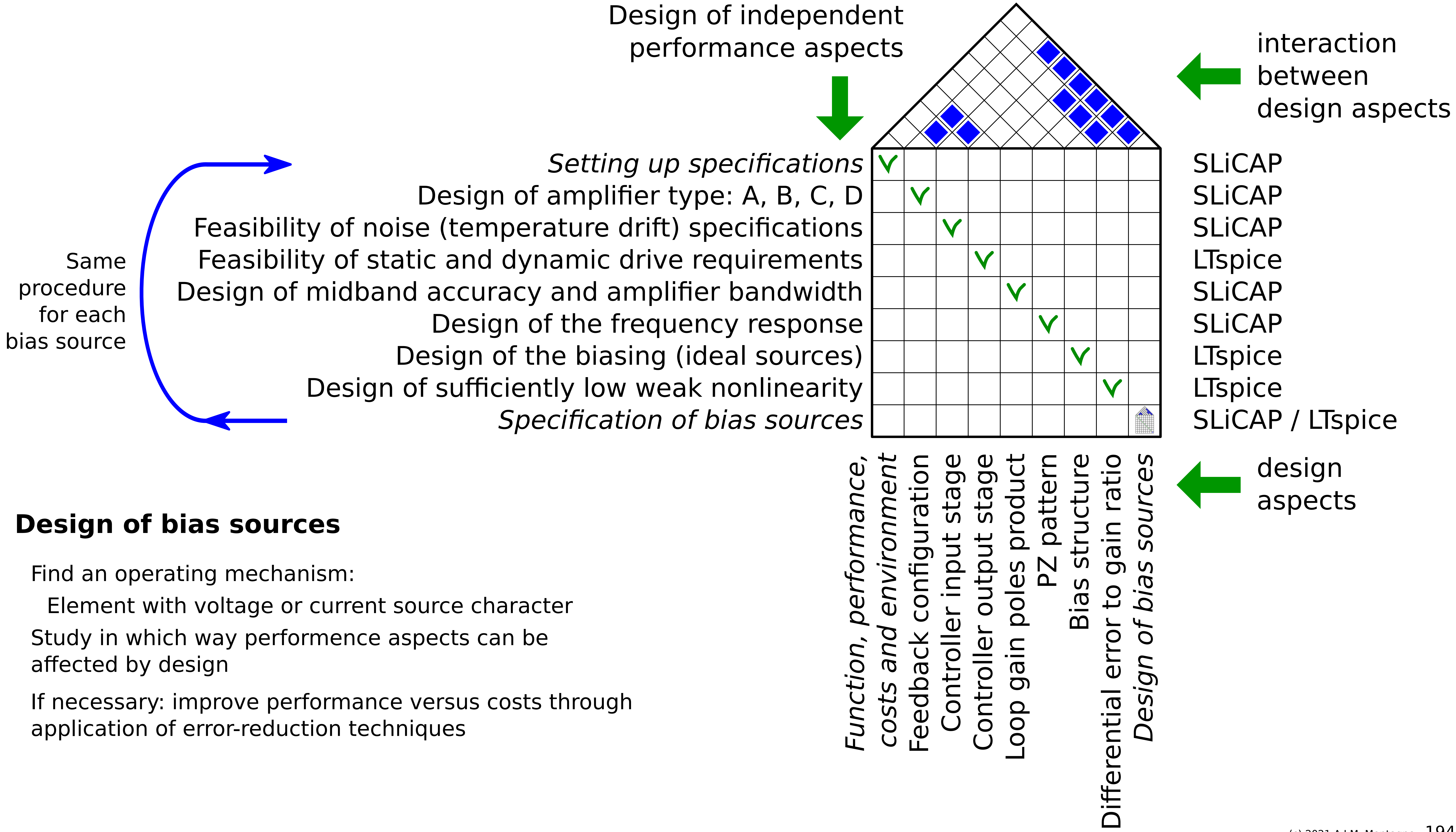
Design of bias sources

Find an operating mechanism:

Element with voltage or current source character

Study in which way performence aspects can be affected by design

If necessary: improve performance versus costs through application of error-reduction techniques



Design of bias sources

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